SGS-THOMSON
MICROELECTRONICS

TEA5170

SWITCH MODE POWER SUPPLY SECONDARY CIRCUIT

- POWER SUPPLY WIDE RANGE 4.5V – 14.5V
- SOFT START
- REFERENCE VOLTAGE 2V ± 5%
- WIDE FREQUENCY RANGE 250KHz
- MINIMUM OUTPUT PULSE WIDTH 500nS
- MAXIMUM PRESET DUTY CYCLE
- SYNCHRONIZATION WINDOW
- OUTPUT SWITCH
- UNDERVOLTAGE LOCKOUT
- FREQUENCY RANGE WITH SYNCHRONIZATION 64KHz

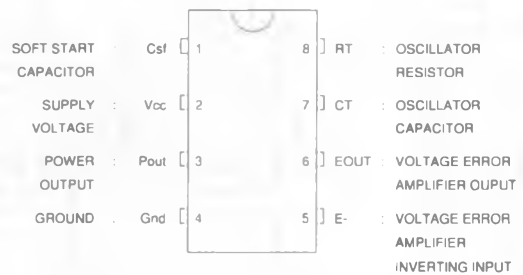
DIP8
(Plastic Package)

ORDER CODE : TEA5170

DESCRIPTION

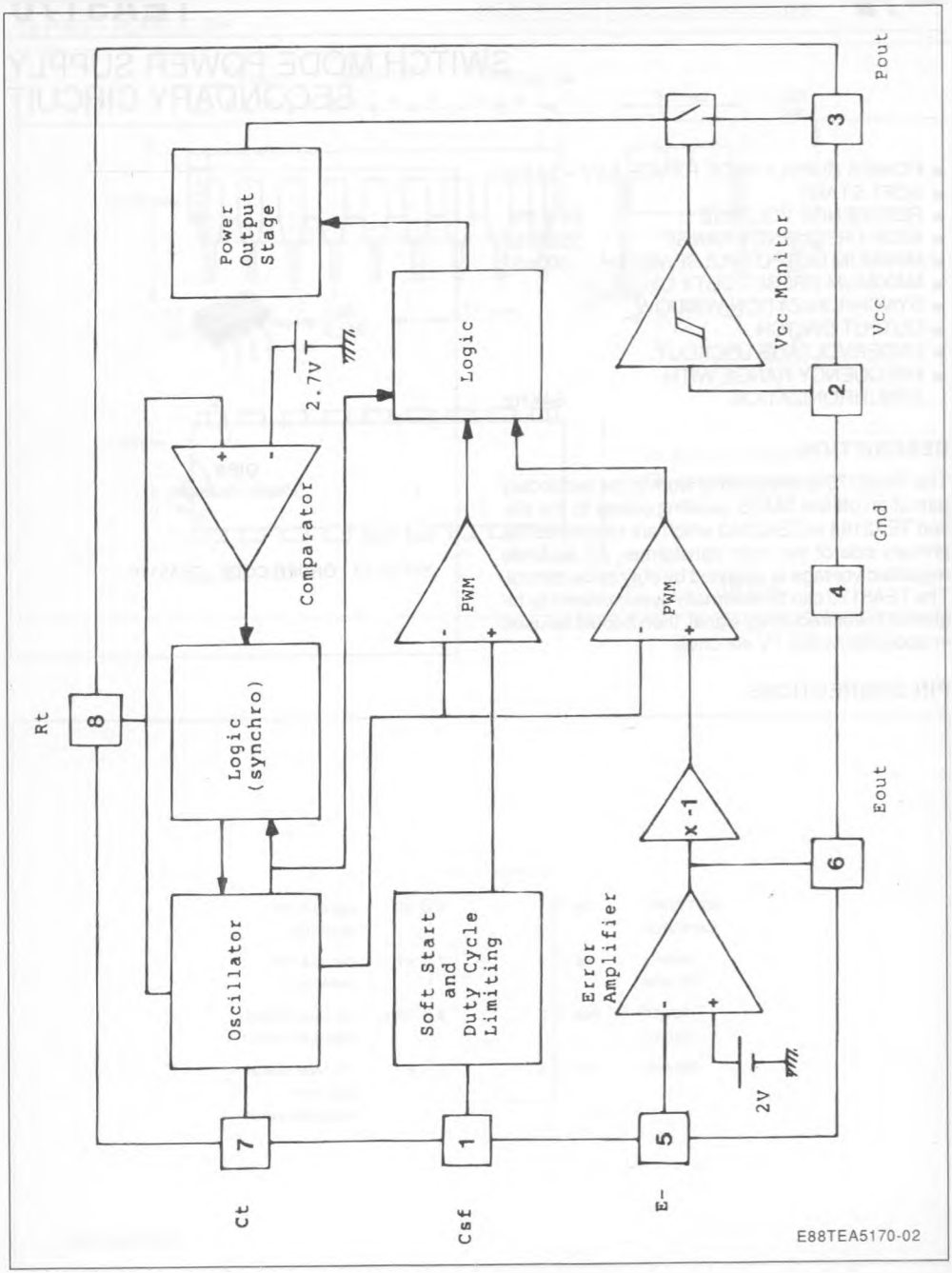
The TEA5170 is designed to work in the secondary part of an off-line SMPS, sending pulses to the slaved TEA2164 or TEA2260 which are located on the primary side of the main transformer. An accurate regulated vol-tage is obtained by duty cycle control. The TEA5170 can be externally synchronized by higher or lower frequency signal, then it could be used in applications like TV set ones.

PIN CONNECTIONS



E88TEA5170-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	15	V
T_j	Operating Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	– 40 to 150	°C

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	90	°C/W

RECOMMANDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	5		14	V
RT	Timing Resistor	47		180	KΩ
CT	Timing Capacitor	0.12		1.8	nF
Fosc	Oscillator Frequency	12		250	KHz
Fsy	Synchro Frequency	12		64	KHz
T_{amb}	Operating Ambient Temperature	– 20		70	°C
VRT	Voltage on Pin RT (8)			7	Volt
VCT	Current on Pin CT (1)			100	µA
ISOURCE	Output Current		30	60	mA

ELECTRICAL CHARACTERISTICS (TA = 25°C)

T_A = 25°C ; V_{CC} = 12V (unless otherwise specified)

OSCILLATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TA	Free Period	RT = 100KΩ ± 0% CT = 1.2nF ± 0% Vcc = 12V	60.40	65.60	70.80	µS
TB		RT = 100KΩ ± 0% CT = 560pF ± 0% Vcc = 12V	29.18	31.70	34.22	µS
ΔFosc (T)	Frequency drift due to ambient temperature variation from 0C to 70C $\frac{Fosc\ (70°C) - Fosc\ (0°C)}{70°C \times Fosc\ (25°C)}$	RT = 100KΩ ± 0% CT = 1.2nF ± 0% Vcc = 12V		0.01		%/°C
ΔFosc (Vcc)	Frequency drift due to Vcc variation from 5V to 12V $\frac{Fosc\ (12V) - Fosc\ (5V)}{7V \times Fosc\ (12V)}$	RT = 100KΩ ± 0% CT = 1.2nF ± 0%		0.07		%/V

ELECTRICAL CHARACTERISTICS (continued)
T_A = 25°C ; V_{CC} = 12V (unless otherwise specified)

ERROR VOLTAGE AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Ibias	Input Bias Current	Ein = 2V	0	0.2	1	µA
Gvol	Voltage Gain			80		dB
GB	Gain Bandwidth			2		MHz
	Slew Rate			2		V/µs

INTERNAL VOLTAGE REFERENCE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	Voltage Reference	Using the voltage error amp. as a follower	1.9	2	2.1	V
ΔVREF (Vcc)	Line Regulation $\frac{VREF(12V) - VREF(5V)}{7V}$	Vcc = 5V to 12V	– 3	0.4	3	mV/V
ΔVREF (T)	VREF drift with temperature $\frac{VREF(70°C) - VREF(0°C)}{70}$	TA = 0°C to 70°C		0.2		mV/°

TON MIN

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TONMIN A	Minimum Duty Cycle	Ct = 1.2nF ± 0% Rt = 100KΩ ± 0%	1.77	2.53	3.29	µs
TONMIN B	Minimum Duty Cycle	Ct = 560pf ± 0% Rt = 100KΩ ± 0%	1.04	1.49	1.94	µs

POWER OUTPUT STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VPOUTH	Output High Level	Iload = 1mA	6.3	6.9	7.5	V
VPOUTL	Output Low Level	Iload = – 1mA	0.5	0.8	1.1	V
ISINK	Sink Current	VPOUT = 3V	30	60	190	mA
ISOURCE	Source Current	VPOUT = 3V	30	110	190	mA

ELECTRICAL CHARACTERISTICS (continued)
$T_A = 25°C$; $V_{CC} = 12V$ (unless otherwise specified)

SYNCHRONISATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Ftrig Max	Maximum Synchro Frequency		64			KHz
Vtrig	Synchro Triggering Threshold			2.7	3	V
Ttrigp	Synchro Triggering Pulse Width	at VRT = 2.7Volt (fig 5)	800			nS
Wtrig +	Positive Triggering Window $\frac{Ttrig + - To}{To}$	CT = 1.2nF ± 0% RT = 100KΩ ± 0%	25	35	40	%
Wtrig –	Negative Triggering Window $\frac{To - Ttrig -}{To}$	CT = 1.2nF ± 0% RT = 100kΩ ± 0%	9	29	42	%

SOFT START

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Icsf	*Csf Load Current	Vcsf = 1V	2.5	3.7	6	µA
Donmax	Maximum Duty Cycle *Csf is a high impedance capacitor	Vcs > 2.5V Vcc = 12V CT = 1.2nf ± 0% RT = 100KΩ ± 0%	60	78	95	%

VCC MONITOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VSTART	Turn-on Threshold		3.60	4	4.40	V
VHYST	Hysteresis Voltage		100			mV
VSTOP	Turn-off Threshold		3.50			V

TOTAL DEVICE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Icc	Supply Current	RT = 100KΩ ± 0% CT = 1.2nf ± 0% No Load on Pin 3 Vcc = 12V	7	12	25	mA

GENERAL DESCRIPTION

The TEA5170 takes place in the secondary part of an isolated off-line SMPS. During normal mode operation, it sends pulses to the slave circuit (TEA2164 or TEA2260) through a pulse transformer to achieve a very precisely regulated voltage by duty cycle control.

The main blocs of the circuit are :

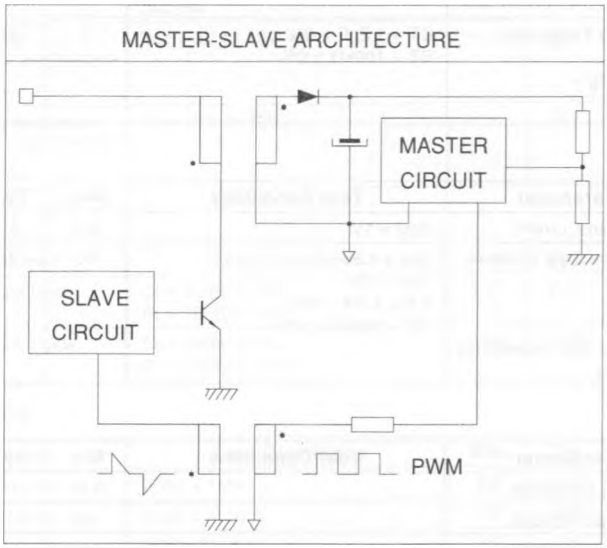
- an error voltage amplifier
- an RC oscillator
- an output stage
- a V_{CC} monitor
- a voltage reference bloc
- a pulse width modulator
- two logic blocs
- a soft start and Duty cycle limiting bloc

PRINCIPLE OF OPERATION

The TEA5170 sends pulses continuously to the slave circuit in order to insure a proper behaviour of the primary side.

- According to this, the output duty cycle is varying between Donmin (0.05) and Donmax (0.75) : then even in case of open load, pulses are still sent to the slave circuit.

Figure 1 : Basic Concept.

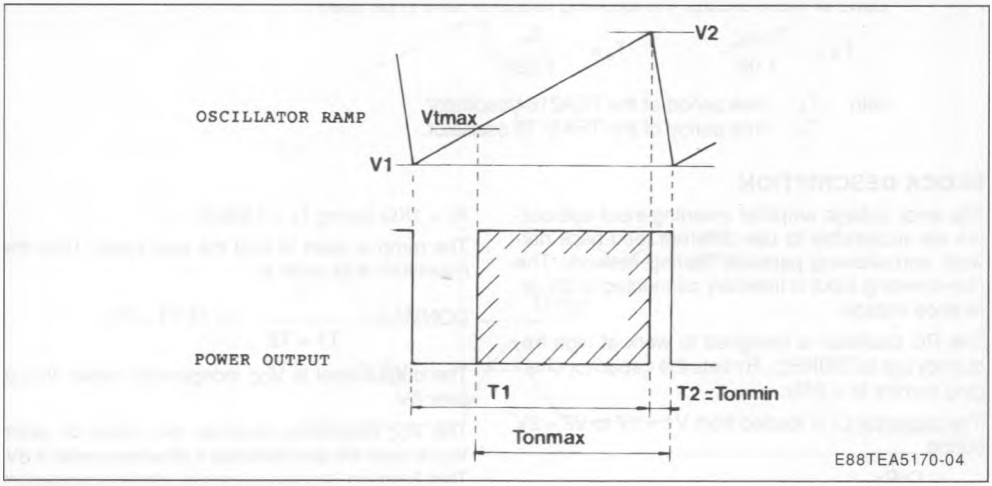


ASYNCHRONIZED MODE

The regulated voltage image is compared to 2V voltage reference. The error voltage amplifier output and the RC oscillator voltage ramp are applied to the internal Pulse Width Modulator Inputs.

The PWM logic Output is connected to a logic bloc which behaves like a RS latch, sets by the PWM output and resets when Ct downloading occurs. Finally, the push-pull output bloc delivers square wave signal whom output leading edge occurs during Ct uploading time, and output trailing edge at Ct downloading time end. The duty cycle is limited to 75% of oscillator period as maximum value and to Ct downloading time/oscillator period as minimum value (Figure 2).

Figure 2 : Asynchronized Mode.



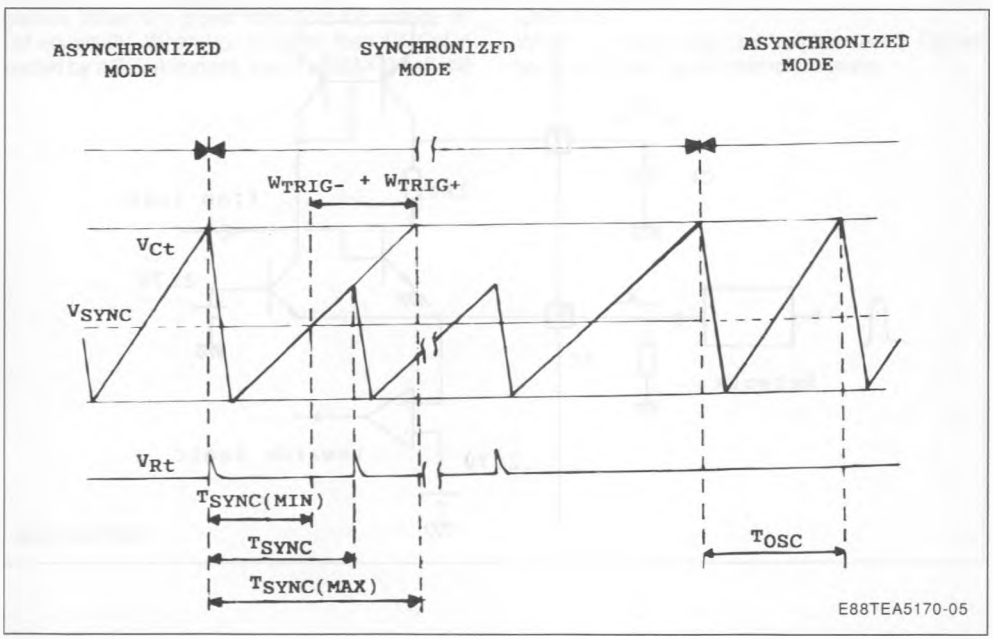
SYNCHRONIZED MODE (figures 3, 4, 5)

The TEA5170 will enter the Synchronized Mode when it receives one pulse through Rt during Ct discharge.

At that time Ct charging current will be multiplied by 0.75 and period will increase up to To x 1.33.

A pulse occuring during the synchro window, commands the Ct downloading. If none, the TEA5170 will return to normal mode at the end of the period.

Figure 3 : Synchronized Mode.



Remark : In case of an application between TEA5170 and TEA2164, to optimize the synchronization windows of these circuits, the following relations have to be used :

$$T_m = \frac{T_{SYNC}}{1.06} \qquad T_e = \frac{T_m}{1.223}$$

with - T_e : Free period of the TEA2164 oscillator.
- T_m : Free period of the TEA5170 oscillator.

BLOCK DESCRIPTION

The error voltage amplifier inverting-input and output are accessible to use different feed-back network and allowing parasitic filtering network. The non-inverting input is internaly connected to 2V reference voltage.

The RC oscillator is designed to work at high frequency (up to 250KHz). R_T sets the capacitor charging current $Io = 2/R_T$.

The capacitor C_T is loaded from $V1 \approx 1V$ to $V2 \approx 2V$ during

$T1 = \frac{C_T R_T}{1.985}$ and then down loaded through an integrated resistor

$R_2 \approx 1K\Omega$ during $T_2 = 1300\ C_T$

The ramp is used to limit the duty cycle. Then the maximum duty cycle is

$$DONMAX = \frac{1}{T1 + T2} \quad (0.73\ T1 + T2)$$

The output level is V_{CC} independant when V_{CC} is over 8V.

The V_{CC} monitoring switches the circuit on when V_{CC} is over 4V and switches it off when under 3.8V. This function insures a proper starting procedure (made by the primary side circuit).

SYNCHRONIZATION

Figure 4 : Triggering Schematic.

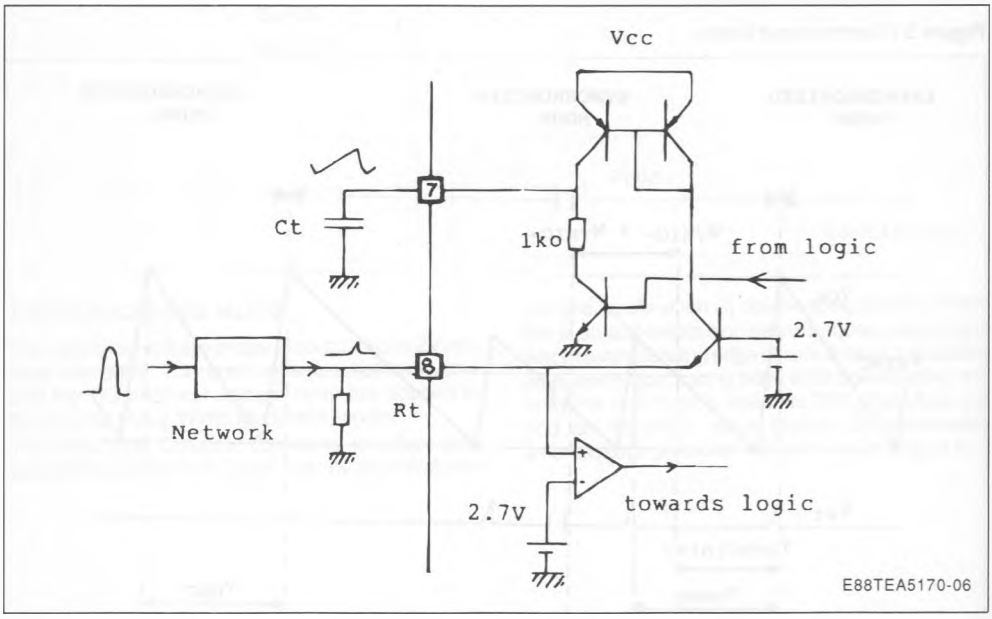
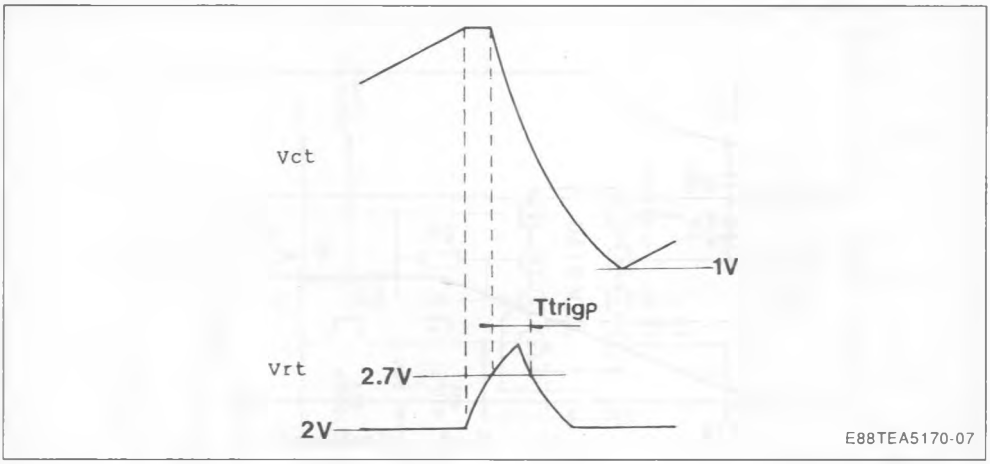


Figure 5 : Typical Wave Forms.



STARTING

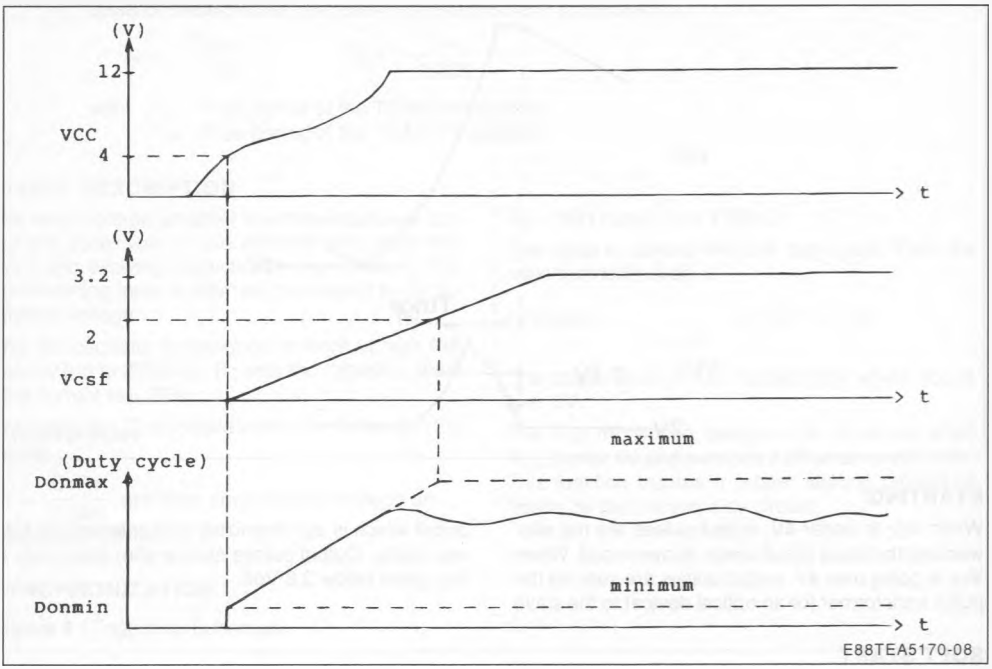
When V_{CC} is under 4V, output pulses are not allowed and the slave circuit keeps its own mode. When V_{CC} is going over 4V, output pulses are sent via the pulse transformer (or an optical device) to the slave circuit which is synchronizing and entering the slaved mode. Output pulses can be shut down only if V_{CC} goes below 3.8 Volt.

SOFT START

Using Csf, it is possible to make a soft start sequence. When V_{CC} grows from 0V to 4V, voltage on Csf equals 0V. When V_{CC} is higher than 4V, Csf is loaded by a 3.7µA current, then TonMAX (Vcsf) will vary linearly from Tonmin to Tonmax according to Csfst bias.

When V_{CC} will go low (3.8 Volt threshold), Csf will be downloaded by an internal transistor.

Figure 6 : Soft Start Sequence.



POWER OUTPUT STAGE

Figure 7 : Electrical Schematic.

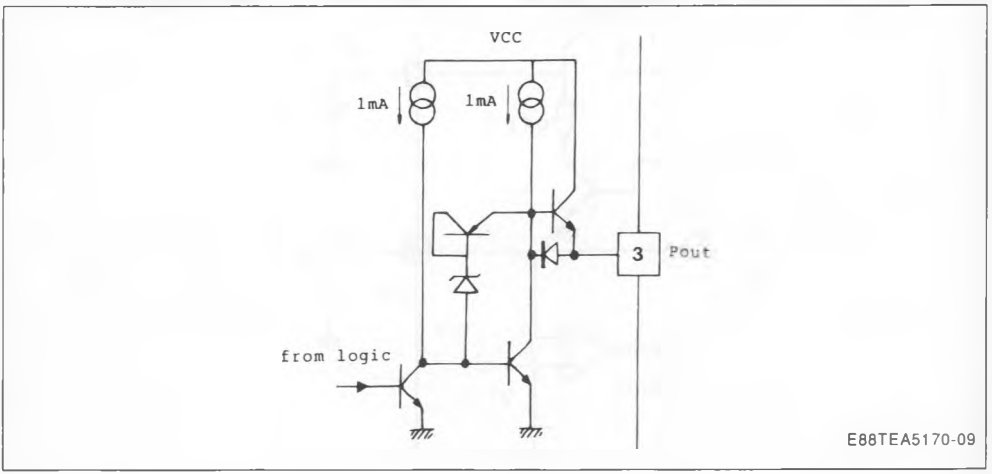


Figure 8.

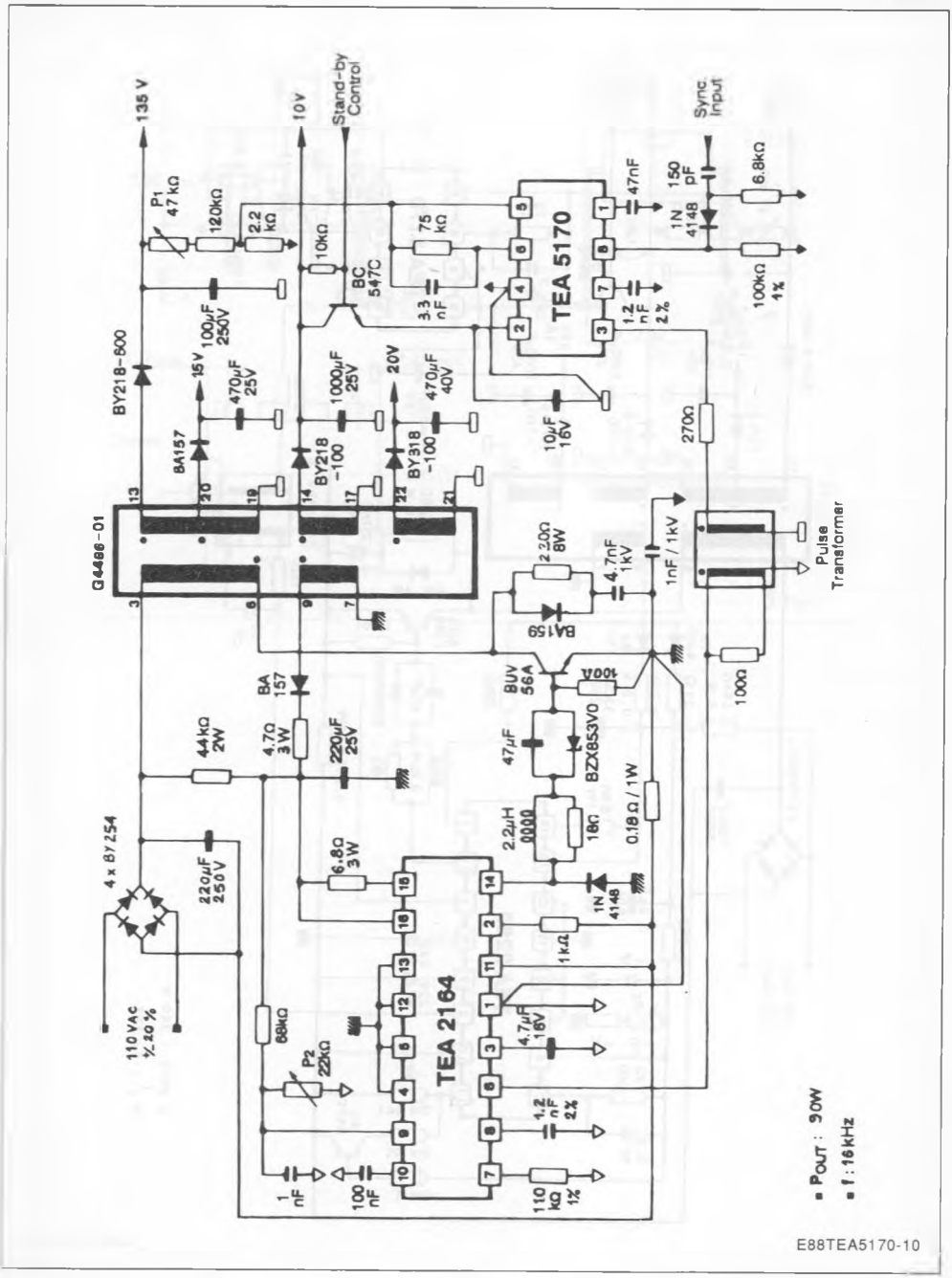
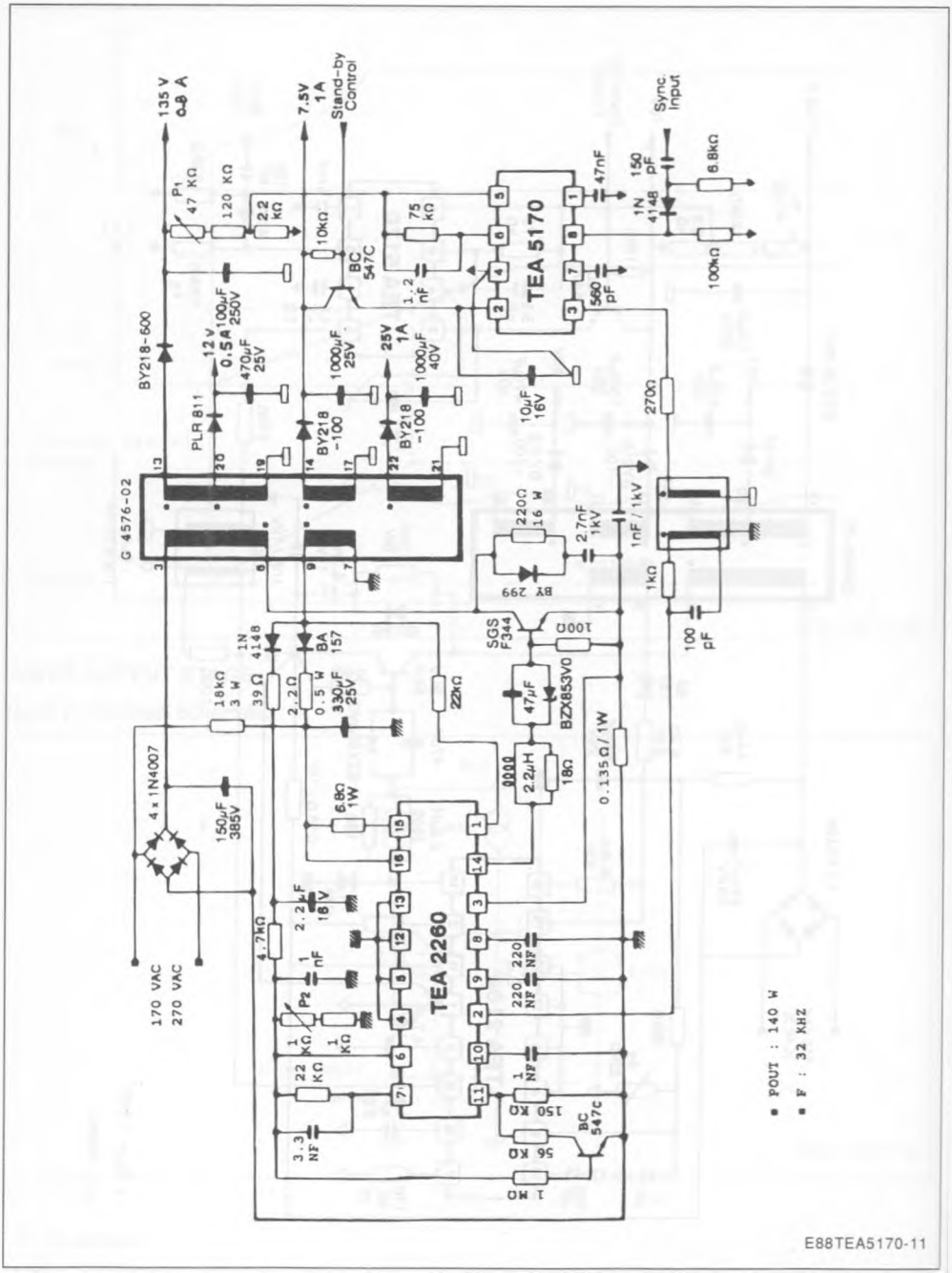

135 V
10V
Stand-by Control
Sync Input
P1 47 kΩ
120kΩ
2.2 kΩ
10kΩ
75 kΩ
BC 547C
3.3 nF
TEA 5170
47nF
150 pF
1N 4148
6.8kΩ
100kΩ 1%
1.2 nF 2%
BY218-600
15 V
100µF 250V
470µF 25V
BA157
BY218 -100
1000µF 25V
20V
BY318 -100
470µF 40V
10µF 16V
270Ω
G4466-01
2.2Ω 8W
4.7nF 1kV
1nF / 1kV
Pulse Transformer
BA1159
BA 157
BUV 56A
500A
100Ω
44kΩ 2W
4.7Ω 3W
220µF 25V
47µF
BZX85C3V0
2.2µH
18Ω
0.18Ω / 1W
4 x BY254
220µF 250V
6.8Ω 3W
1N 4148
1kΩ
TEA 2164
4.7µF 16V
68kΩ
P2 22kΩ
1.2 nF 2%
110 VAC ±10 %
1 nF
100 nF
110 kΩ 1%
▪ POUT : 90W
▪ f : 16 kHz
E88TEA5170-10

Figure 9.


135 V 0.8 A
7.5V 1A Stand-by Control
Sync. Input
TEA 5170
TEA 2260
G 4576-02
BY218-600
PLR 811
BY218 -100
BC 547C
SGS F344
BZX853V0
BY 299
4 x 1N4007
170 VAC
270 VAC
• POUT : 140 W
• F : 32 KHZ
E88TEA5170-11

PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP