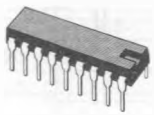
SGS-THOMSON MICROELECTRONICS

TEA5115

5 CHANNELS VIDEO SWITCH

- EACH CHANNEL EXCEPT FAST BLANKING HAS 6dB GAIN
- R, G, B AND VIDEO SIGNALS ARE CLAMPED TO THE SAME REFERENCE VOLTAGE IN ORDER TO HAVE NO OUTPUT DIFFERENTIAL VOLTAGE WHEN SWITCHING
- ALL INPUT LEVELS COMPATIBLE WITH NFC 92250 AND EN 50049 NORMS
- 30MHz BAND WIDTH FOR R, G, B SIGNALS
- INTERNAL 6.7V SHUNT REGULATOR FOR :
  - LOW IMPEDANCE LOADS,
  - POWER DISSIPATION LIMITATION
- INDEPENDANT VIDEO OR SYNCHRONIZING SIGNAL SELECTION
- SIMULTANEOUS SWITCHING OF R, G, B AND FB SIGNALS BY FB1 INPUT (internal)



DIL18
(Plastic Package)

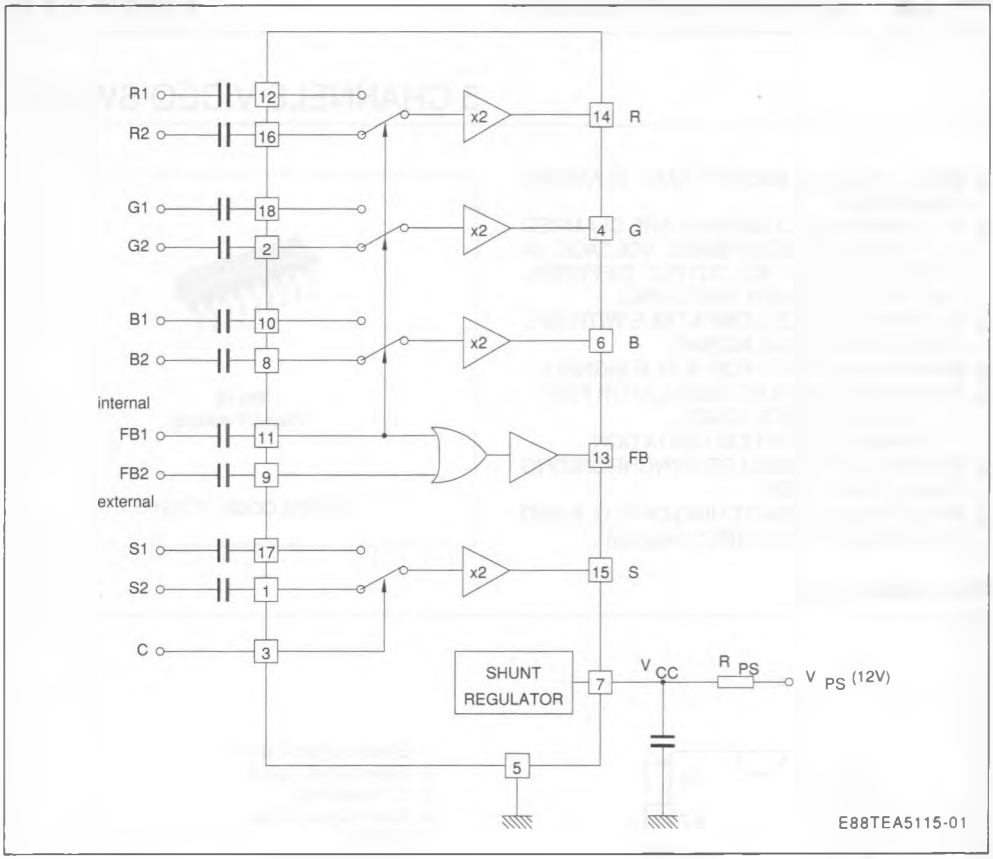
ORDER CODE : TEA5115

PIN CONNECTION

E88TEA5115-02

1 - Synchro signal input 2
2 - Green signal input 2
3 - "C" select input
4 - Green signal output
5 - Ground
6 - Blue signal output
7 - Shunt regulator supply input
8 - Blue signal input 2
9 - Fast blanking input 2 (external)
10 - Blue signal input 1
11 - Fast blanking input 1 (internal)
12 - Red signal input 1
13 - Fast blanking output
14 - Red signal output
15 - Synchro signal output
16 - Red signal input 2
17 - Synchro signal input 1
18 - Green signal input 1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_{CC}	Supply Current (see note)	150	mA
V_{in}	Input Voltage (all inputs)	− 0.5 to V_{CC} + 0.5	V
T_{oper}	Operating Temperature Range	0 to 70	°C
T_j	Junction Temperature	− 40 to + 150	°C
T_{stg}	Storage Temperature	− 40 to + 150	°C

Note : Minimum output load is 300 Ω in case of all outputs loaded.

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	70	°C/W

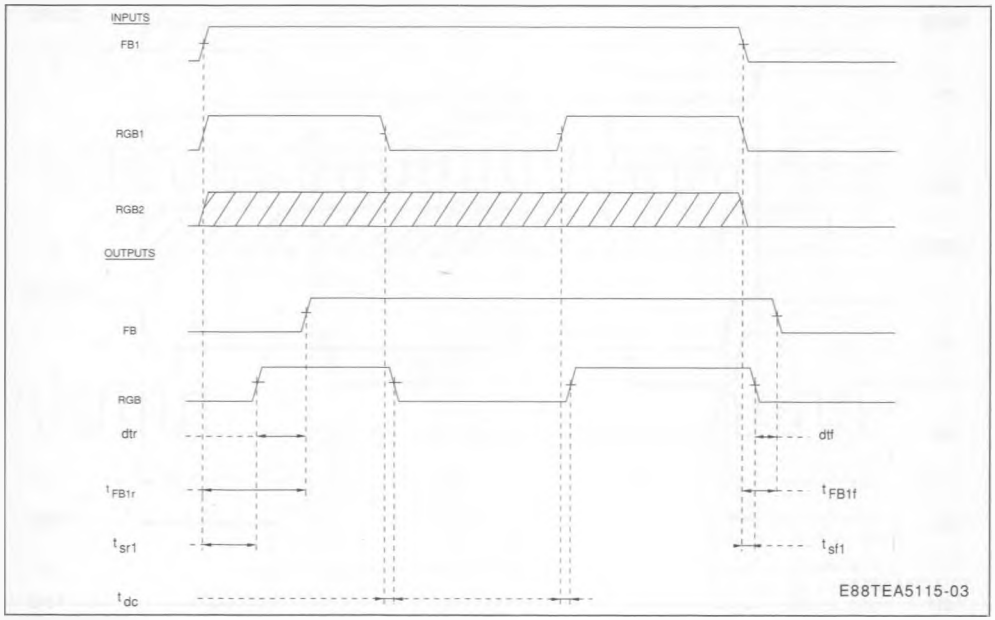
ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C, I_{CC} = 120 mA ; Load value = 150 Ω (sequentially switched) (unless otherwise specified, refer to test circuit page 7)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Internal Shunt Regulator	I_{CC} = 120 mA	6.3	6.7	7.2	V
		I_{CC} = 90 mA	6.2		7.3	V
		I_{CC} = 150 mA	6.2		7.3	V
R, G, B Switches (pins 4, 6, 14) (Time Measurement Conditions : Δ inputs RGB = 0.7 V_{pp} ; FB input pulse amplitude = 2 V)						
V_C	DC Output Voltage (no input voltage)	$T_{junction}$ = 25 °C		0.9	1.25	V
		$T_{junction}$ stabilized		1.2		
V_{AC}	Max Output Swing Voltage		2	4.0		V_{pp}
B	Bandwidth (– 3 dB) (input voltage 0.7 V_{pp})		20	30		MHz
A_v	Gain of Each Channel (input voltage 0.7 V_{pp} ; F = 1MHz)		5.5	6	6.5	dB
A_{dc}	Gain Difference Between any two R, G, B Channels (input voltage 0.7 V_{pp} ; F = 1 MHz)			0.1	0.5	dB
	Input Swing			0.7 V ± 3dB		
z_{ic}	DC Input Impedance			10		kΩ
z_{oc}	Dynamic Output Impedance (input voltage 0.7 V_{pp} ; F = 1MHz) with R_{load} = 300 Ω			10		Ω
	Crosstalk between any inputs (R1 and R2 or B1 and B2 or G1 and G2) (input voltage 0.7 V_{pp} ; F = 1 MHz).		45	55		dB
	Crosstalk between any outputs (input voltage 0.7 V_{pp} ; F = 1 MHz).		40	55		dB
t_{dc}	Delay time between R, G, B inputs and RGB outputs.			10		ns
t_{sr1}	Switching rise time between FB1 input signal and R, G, B output signal.			60	110	ns
t_{sf1}	Switching fall time between FB1 input signal and R, G, B output signal.			10	40	ns
t_{sr2}	Switching rise time between FB2 input signal and R, G, B output signal.			10		ns
t_{sf2}	Switching fall time between FB2 input signal and R, G, B output signal.			10		ns
t_{d11}	R1, G1, B1 Decay Time			30		ns
t_{d12}				60		ns
t_{d21}	R2, G2, B2 Decay Time			45		ns
t_{d22}				40		ns
Fast Blanking Switch (pin 13) (time measurement conditions : FB input pulse amplitude = 2 V)						
V_{IL}	Low Level Input Voltage FB1 and FB2		– 0.5		0.45	V
V_{IH}	High Level Input Voltage FB2 External		1		V_{CC}+0.5	V
V_{IH}	High Level Input Voltage FB1 Internal		1.2		V_{CC}+0.5	V
V_{OL}	Low Level Output Voltage				0.6	V
V_{OH}	High Level Output Voltage	$T_{junction}$ = 25 °C	1.4	1.7	3.5	V
		$T_{junction}$ stabilized	1.5	1.9		V
	Input Current (without load)			1.5		µA
	Dynamic Output Impedance : with R_{load} = 300 Ω			10		Ω
t_{FB1r}	Switching rise time between FB1 input and FB output.			120	160	ns
t_{FB1f}	Switching fall time between FB1 input and FB output.			25	60	ns

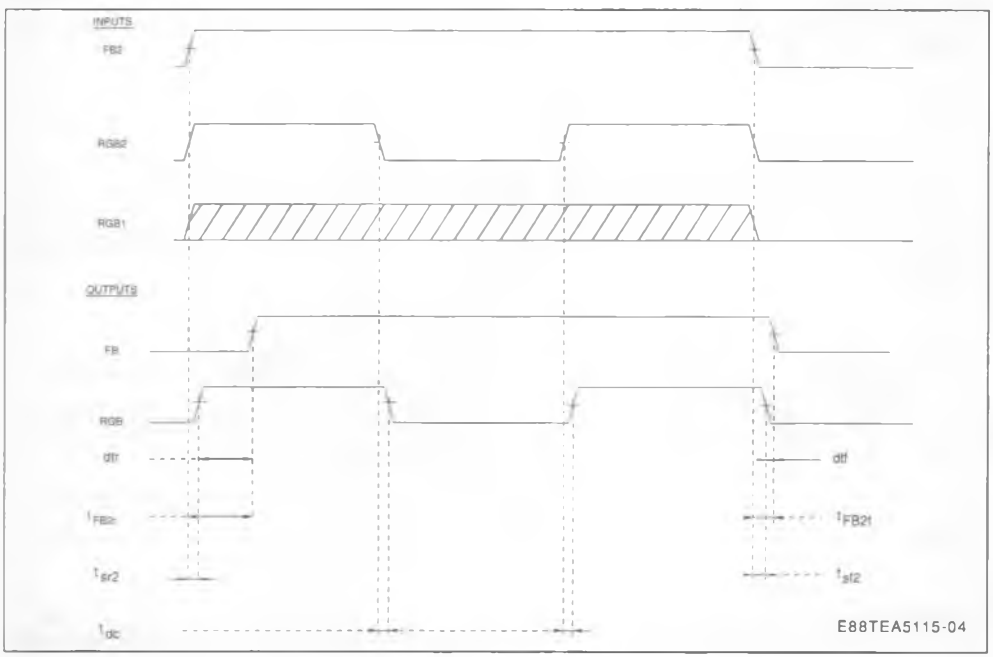
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{FB2r}	Switching rise time between FB2 input and FB output.		70		nsec
t_{FB2f}	Switching fall time between FB2 input and FB output.		35		nsec
d_{tr}	Delay Between RGB Output Signal and FB Output Signal (rise time)		50	100	
d_{tf}	Delay Between RGB Output Signal and FB Output Signal (fall time)		20	40	
Video (or synchro) **Signal Switch** (pin 15)					
V_S	DC Output Voltage (no input voltage)				
	$T_{junction}$ = 25 °C		0.9	1.25	V
	$T_{junction}$ stabilized		1.2		V
	Max Output Swing Voltage	2.6			V_{pp}
	DC Input Impedance		10		kΩ
	Dynamic Output Impedance (input voltage $1V_{pp}$; F = 1 MHz) with R_{load} = 300 Ω		10		Ω
	Gain (input voltage 1 V_{pp} ; F = 1 MHz)	5.5	6	6.5	dB
	Bandwidth (– 3 dB) (input voltage 1 V_{pp})	15	20		MHz
	Input Swing		1V ± 3 dB		
t_{cr}	Switching rise time between C input signal and S output signal (C pulse amplitude 3 V).		30		ns
t_{cf}	Switching fall time between C input signal and S output signal (C pulse amplitude 3 V).		10		ns
t_{dc}	Delay Time Between S Input and S Output (Δ input 0.7 V_{pp})		10		ns
Select Input "C" (pin 3)					
V_{IL}	Low Level Input Voltage	– 0.5		1	V
V_{IH}	High Level Input Voltage	2		V_{CC}+0.5	V
I_{IL}	Low Level Input Current (V_{IL} = 1 V)	– 0.6		– 0.1	mA
I_{IH}	High Level Input Current (V_{IH} = 3 V)			0.5	mA

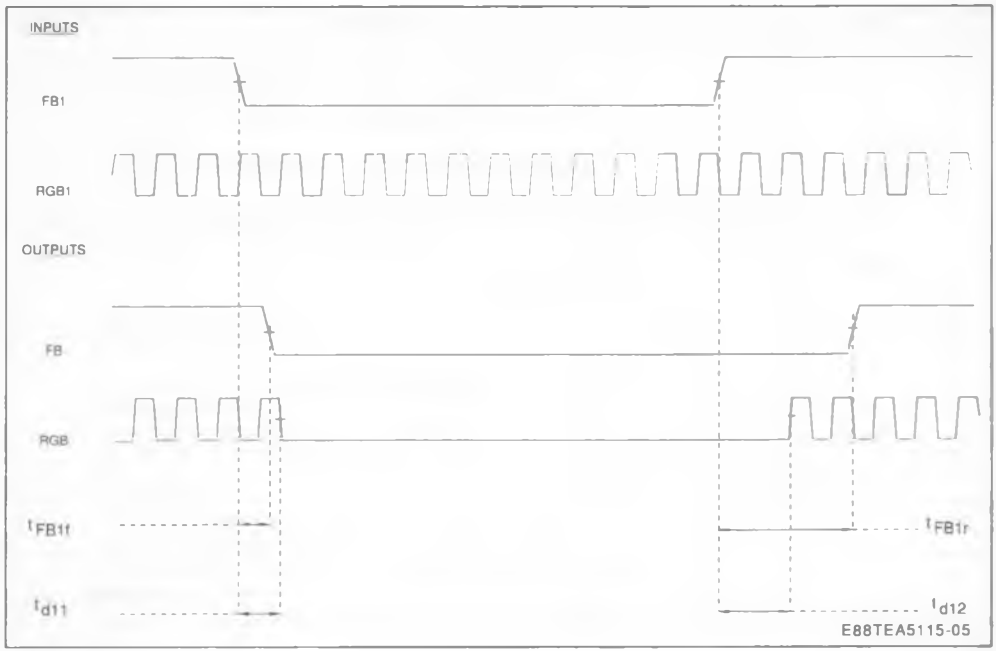
FB2 = 0


INPUTS
FB1
RGB1
RGB2
OUTPUTS
FB
RGB
dtr
dtf
tFB1r
tFB1f
tsr1
tsf1
tdc
E88TEA5115-03

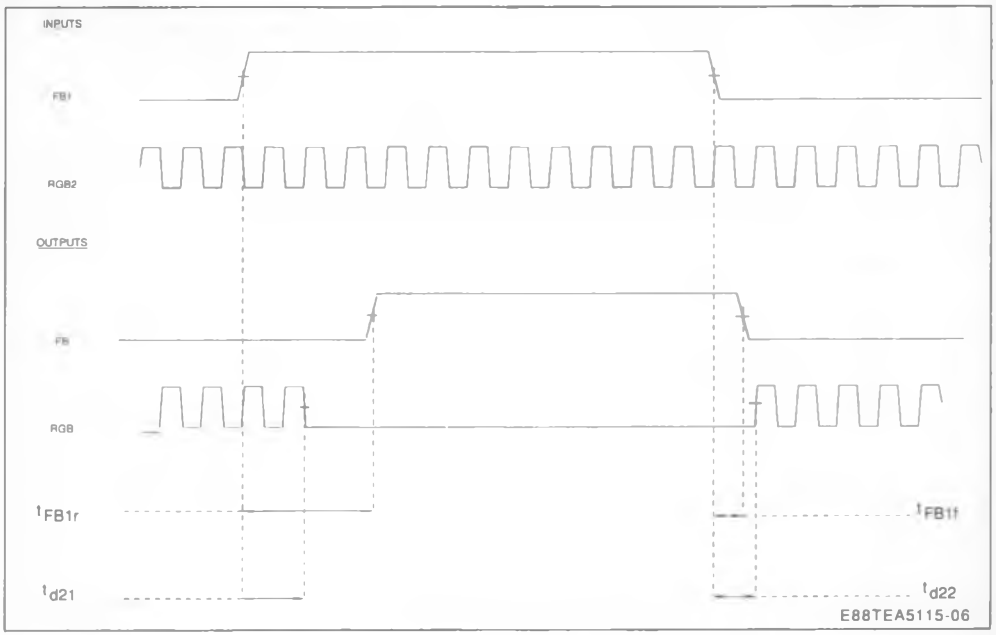
FB1 = 0

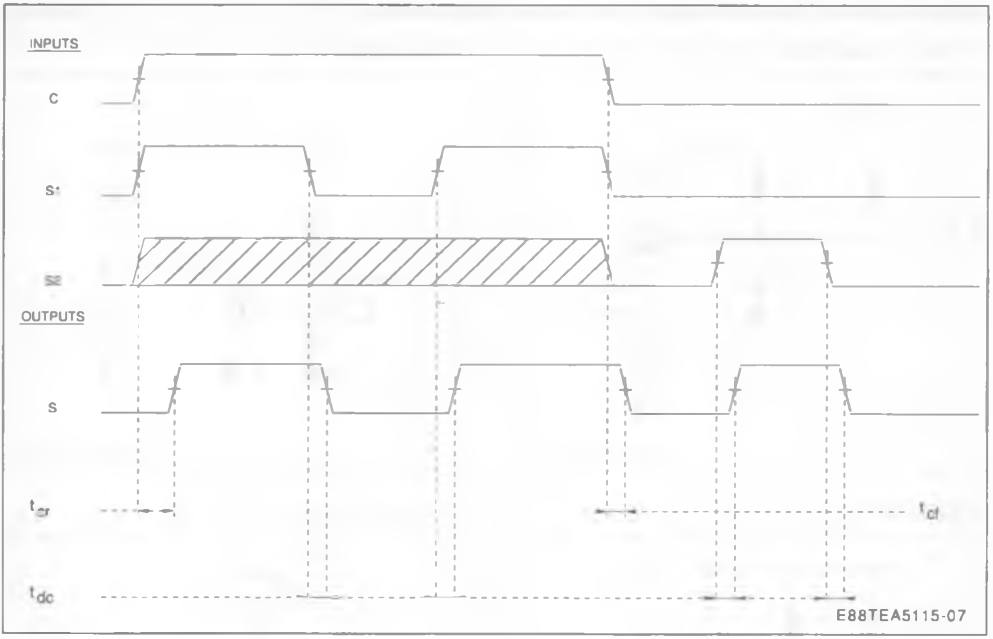

INPUTS
FB2
RGB2
RGB1
OUTPUTS
FB
RGB
dtr
dtf
tFB2r
tFB2f
tsr2
tsf2
tdc
E88TEA5115-04

RGB2 = 0, FB2 = 0

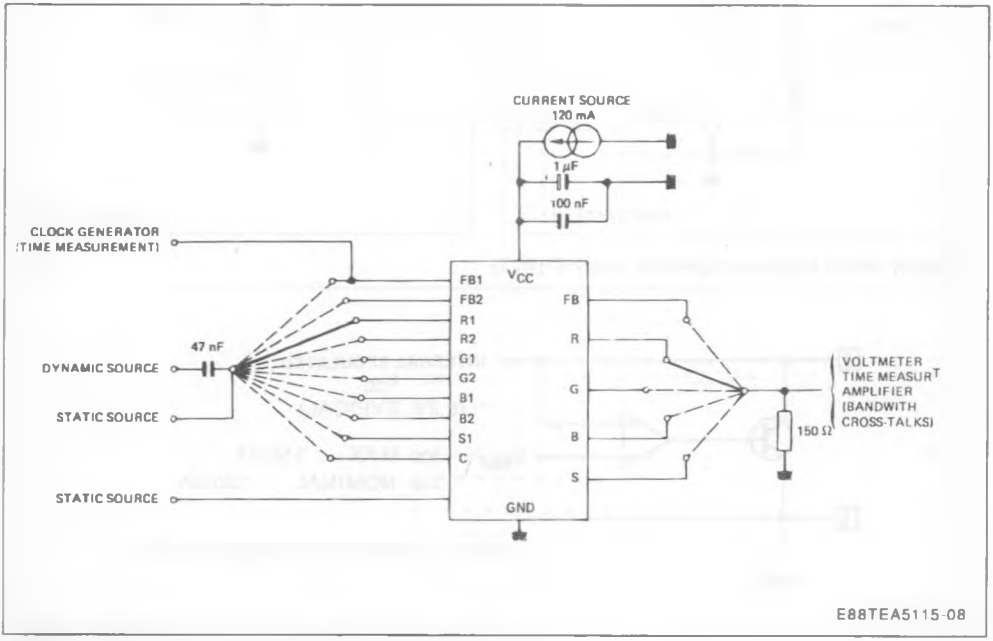


RGB1 = 0, FB2 = 0



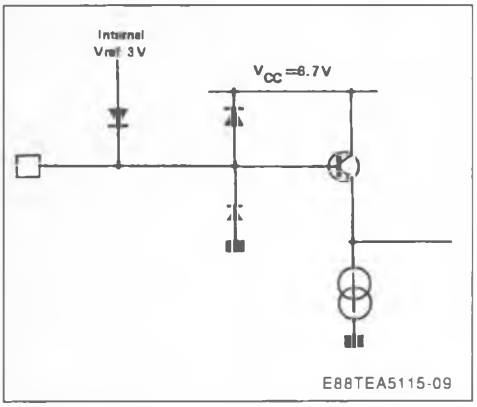


TEST CIRCUIT

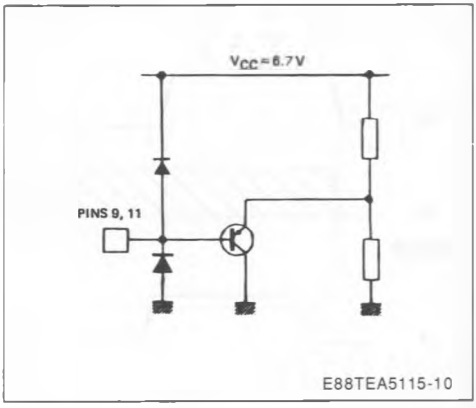


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

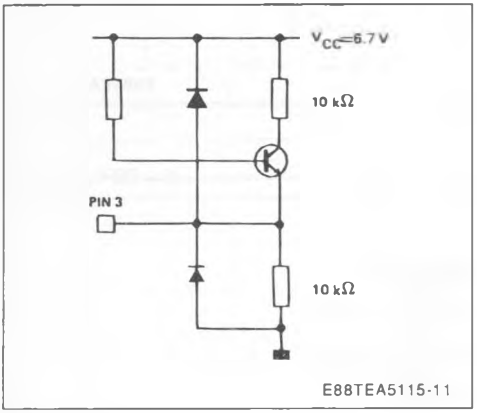
R, G, B, S inputs (pins 1, 2, 8, 10, 12, 16, 17, 18)



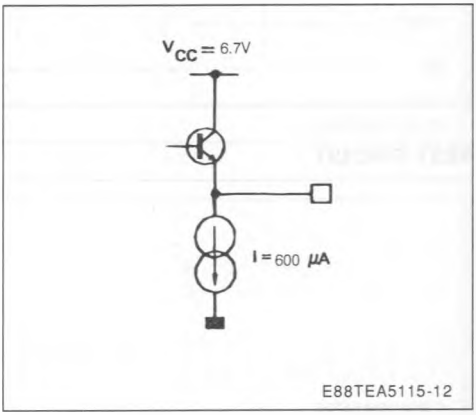
FB inputs (pins 9, 11)



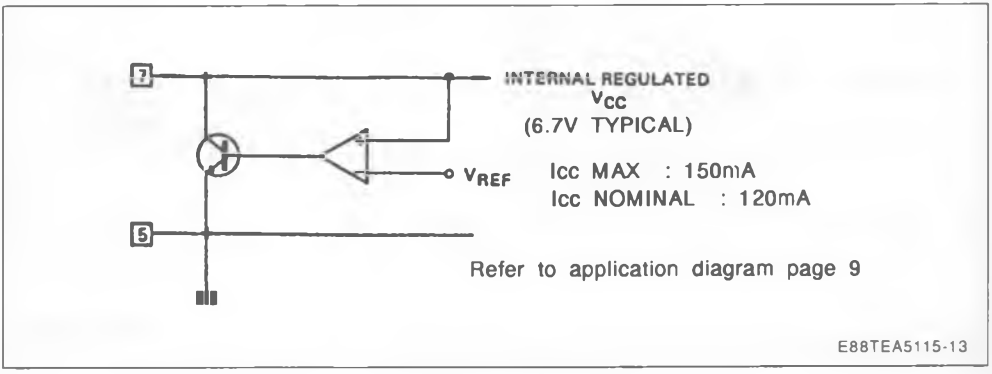
C input (pin 3)



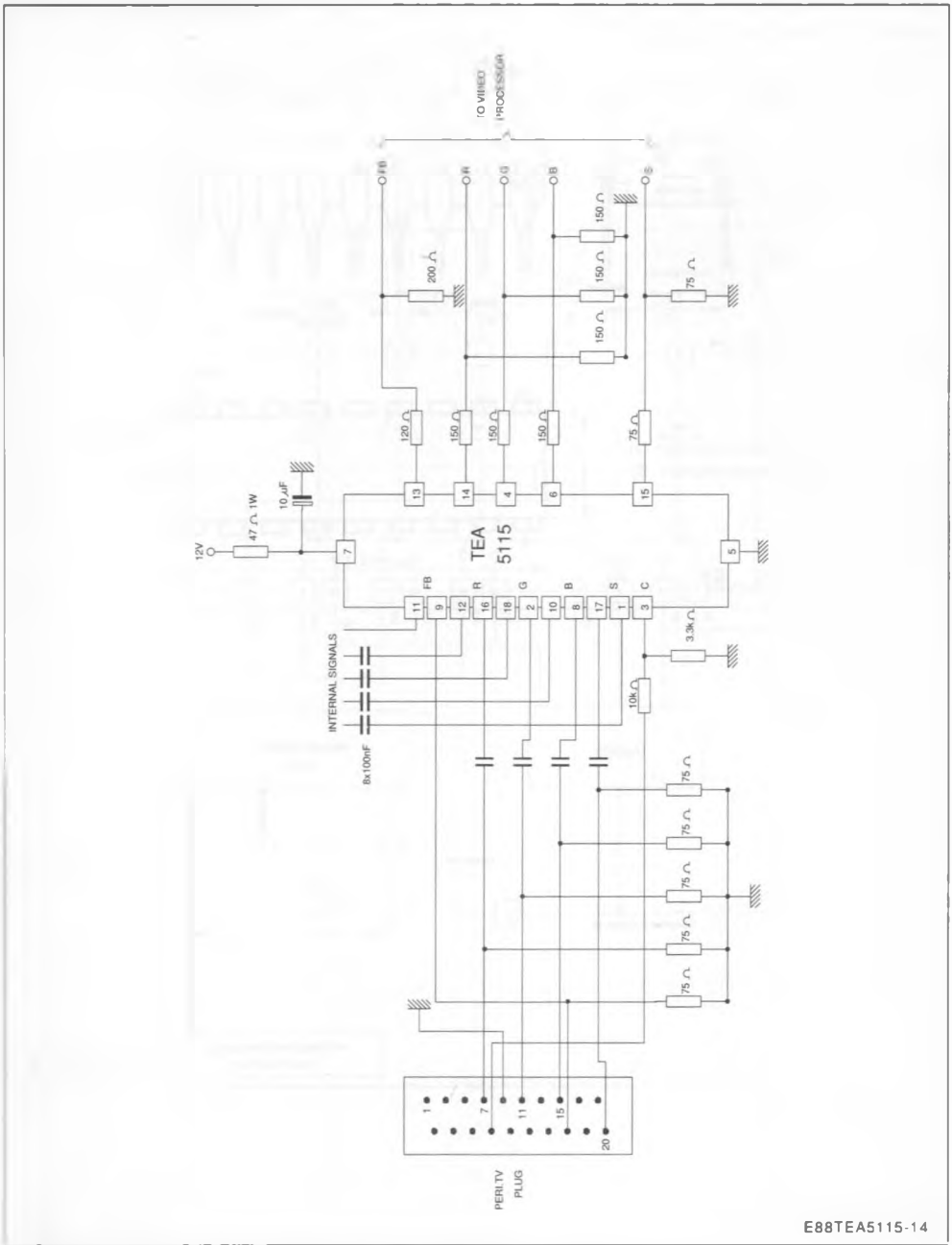
All Outputs (pins 4, 6, 13, 14, 15)



I_{CC} Supply (shunt transistor regulation system) (pin 7)

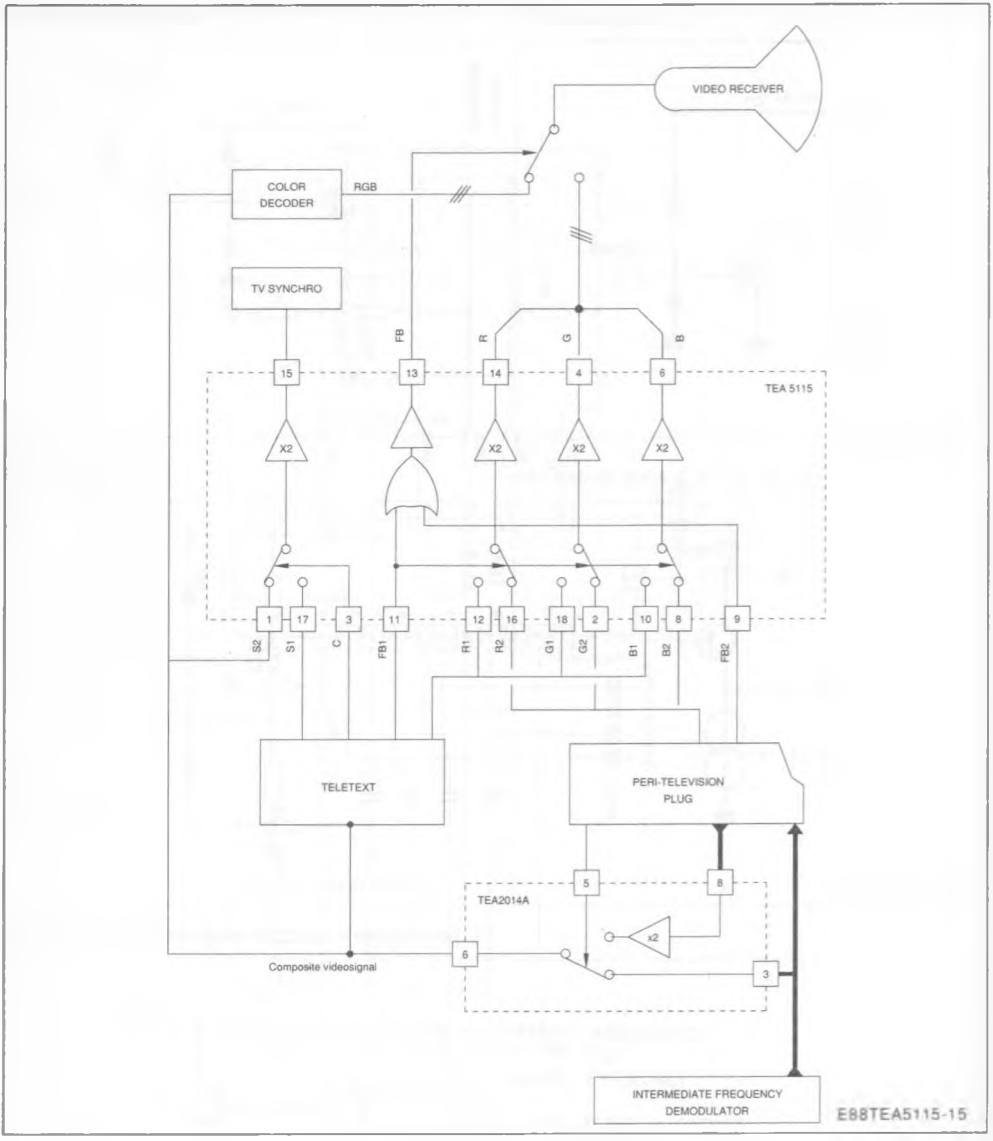


TYPICAL APPLICATION DIAGRAM



- Above given output load values are minimum values, in case of all output loading.
- Minimum output load is 150 Ω individually, provided that total supply current is less than 150 mA.

SIMAVELEC norm application with TEA5115 and TEA2014A.



PACKAGE MECHANICAL DATA

18 PINS – PLASTIC PACKAGE