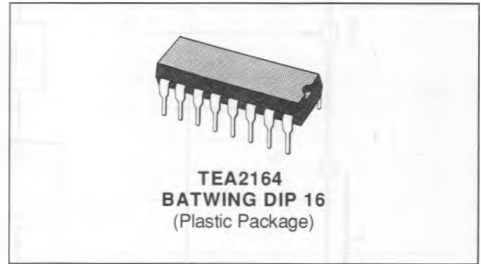# SGS-THOMSON
MICROELECTRONICS

TEA2164

SWITCH MODE POWER SUPPLY PRIMARY CIRCUIT

- POSITIVE AND NEGATIVE OUTPUT CURRENT UP TO 1.2A AND – 1.7A
- A TWO LEVEL COLLECTOR CURRENT LIMITATION
- COMPLETE TURN OFF AFTER LONG DURATION OVERLOADS
- UNDER AND OVER VOLTAGE LOCK-OUT
- SOFT START BY PROGRESSIVE CURRENT LIMITATION
- DOUBLE PULSE SUPPRESSION
- BURST MODE OPERATION UNDER STAND-BY CONDITIONS

DESCRIPTION

In a master slave architecture, the TEA2164 control IC achieves the slave function. Primarily designed for TV receivers and monitors applications, this circuit provides an easy synchronization and smart solution for low power stand by operation.
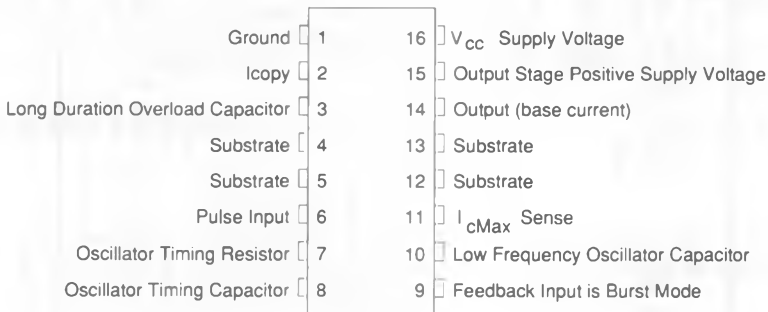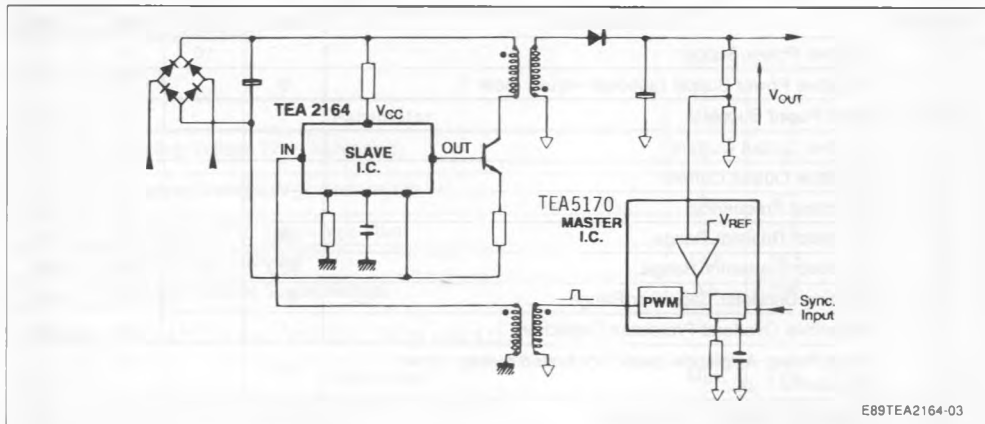Located at the primary side the TEA2164 Control IC ensures :

- the power supply start-up
- the power supply control under stand-by conditions
- the process of the regulation signals sent by the master circuit located at the secondary side
- direct base drive of the bipolar switching transistor
- the protection of the transistor and the power supply under abnormal conditions.

TEA2164
BATWING DIP 16
(Plastic Package)

PIN CONNECTIONS

Ground	1	16	V_{CC} Supply Voltage
Icopy	2	15	Output Stage Positive Supply Voltage
Long Duration Overload Capacitor	3	14	Output (base current)
Substrate	4	13	Substrate
Substrate	5	12	Substrate
Pulse Input	6	11	I_{cMax} Sense
Oscillator Timing Resistor	7	10	Low Frequency Oscillator Capacitor
Oscillator Timing Capacitor	8	9	Feedback Input is Burst Mode

E89TEA2164-03

BLOCK DIAGRAM

E89TEA2164-02

Figure 1 : Simplified Application Diagram.

E89TEA2164-03

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive Power Supply V16-V1	18	V
V+	Positive Power Supply of the Output Stage V15-V1	18	V
V−	Negative Power Supply V4, 5, 12, 13-V1	− 5	V
V_{CC} - V− V+ - V−	Total Power Supply V16-V4, 5, 12, 13 or V15-V4, 5, 12, 13	20	V
I_{out+}	Positive Output Current	1.5	A
$I_{out−}$	Negative Output Current	2	A
T_j	Operating Junction Temperature	150	°C
T_{stag}	Storage Temperature Range	− 40 to 150	°C

THERMAL DATA

$R_{th(j-c)}$	Junction Case Thermal Resistance	11	°C/W
$R_{th(j-a)}^*$	Junction Ambiant Thermal Resistance	45	°C/ W

* Soldered on a 35μm thick 40 cm³ PC board copper area.

MAXIMUM POWER DISSIPATION
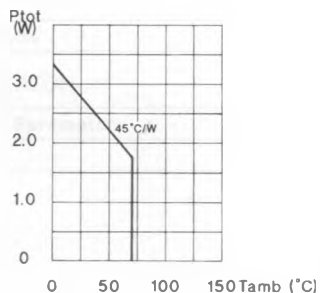
E89TEA2164-04

RECOMMANDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Positive Power Supply		10	14	V
$\lvert V-\rvert$	Negative Power Supply (absolute value) (note 1)	0		5	V
$V_{CC} - V-$	Total Power Supply			18	V
I_{out+}	Positive Output Current			1.2	A
I_{out-}	Negative Output Current			1.7	A
Fsw	Switching Frequency			50	Khz
Ro	Oscillator Resistor Range	30		150	KΩ
Co	Oscillator Capacitor Range	470		2700	pF
C1	Starting Oscillator Capacitor Range	0.1		4.7	µF
C2	Repetitive Overload Protection Capacitor	1		22	µF
$\lvert V_{in}\rvert$	Input Pulses Amplitude (peak) (derivated pulses - time constant = 1 µs)	0.5		1	V
T_{oper}	Operating Ambiant Temperature	– 20		70	°C

Note : 1. The TEA2164 can be used without negative supply voltage, in this case pins 4 - 5 - 12 - 13 must be grounded.

E89TEA2164-05

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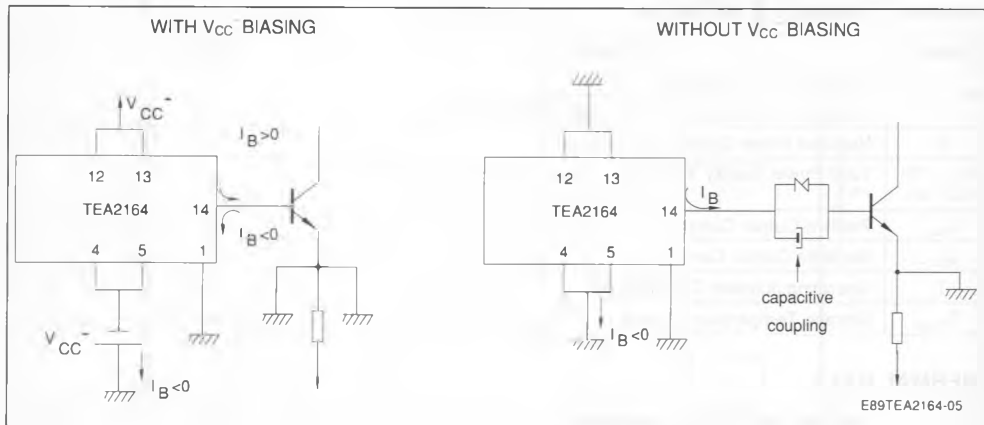
ELECTRICAL OPERATING CHARACTERISTICS
T_{amb} = 25 °C, V_{CC} = 10 V, V_{CC-} = 0 V, potentials referenced to ground (pin 1)
(unless otherwise specified)

POWER SUPPLY

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC} (start)	Starting Voltage (V_{CC} increasing)	8	9	9.6	V
V_{CC} (stop)	Stopping Voltage (V_{CC} decreasing)	5	6.2	7.4	V
ΔV_{CC}	Hysteresis (V_{CC} start – V_{CC} stop)	2	2.8	3.5	V
V_{ccmax}	Overvoltage Lock-out	14.8	15.5	16.2	V
$I_{ccstart}$	Starting Positive Supply Voltage	0.5	0.8	1.5	mA

CURRENT LIMITATION AND PROTECTION (pin 11)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$|VCM1|$	Pulse by Pulse Current Limitation Threshold	720	840	970	mV
$|VCM2|$	Current Monitoring 2nd Threshold	1200	1350	1500	mV
ΔVCM	$\Delta VCM = |VCM2| - |VCM1|$	300	500	700	mV

REPETITIVE OVERCURRENT PROTECTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
$|VCM3|$	Repetitive Overcurrent Threshold (pin 11)	700	900	1100	mV
VCM3-VCM1	(VCM3-VCM1)	– 20	50	130	mV
VC2	Lock-out Voltage on Pin 3	2.4	3	3.6	V
I3 disch	Capacitor C2 Discharge Current (synchronized mode)	10	20	30	µA
I3 ch.	Capacitor C2 Charge Current	50	80	110	µA

OSCILLATOR, MAX DUTY CYCLE, SYNCHRONIZATION

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_o	Oscillator Initial Accuracy RT = 50 K, CT = 1 nF	19.3	21	22.7	µs
$T_{on(max)}$	Maximum Duty Cycle (T_{syn} = 1.05 T_o)	60	70	85	%
$\frac{T_{syn}}{T_o}$	Synchronization Window	1.0		1.5	

OUTPUT STAGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	I_c Copy Current Gain		1000		
I_{BON}	Base Current Starting Pulse		300		mA

VERY LOW FREQUENCY OSCILLATOR

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Burst Duty Cycle		13		%

1. FIELD OF APPLICATION

The TEA2164 control circuit has been designed primarily for discontinuous mode flyback built with a master-slave architecture, whatever the field of application.

But due to its capability to synchronize the transistor switching-off with an external signal (line flyback) and due to an adapted burst-mode operation for a low power stand-by operation, the TEA2164 offers a smart solution for monitors and TV sets applications.

Power supply main features :
- maximum output power 140W (transistor forced gain : 3.5)
- stand-by mode output power (1W $\leq$ Psb $\leq$ 6W ; efficiency > 50%)
- operating frequency up to 50kHz
- power-switch : bipolar transistor

Adapted master-circuit :
Monitor application   ⟶ TEA5170
Standard TV application ⟶ TEA2028B
                                                  TEA2029C
                                                  TEA5170
Digital TV application   ⟶ TEA5170

(TEA2028B and TEA2029C are deflection processor with built-in PWM generator).

2. GENERAL DESCRIPTION

In a master slave architecture, the TEA2164 Control IC, located at the primary side of an off line power supply achieves the slave function ; whereas the master circuit is located at the secondary side. The link between both circuits is realized by a small pulse transformer (fig. 3).

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Figure 2 : Master Slave Power Supply Architecture.

P1 : Output voltage adjustment in normal mode
P2 : Output voltage adjustment in stand-by

E89TEA2164-06
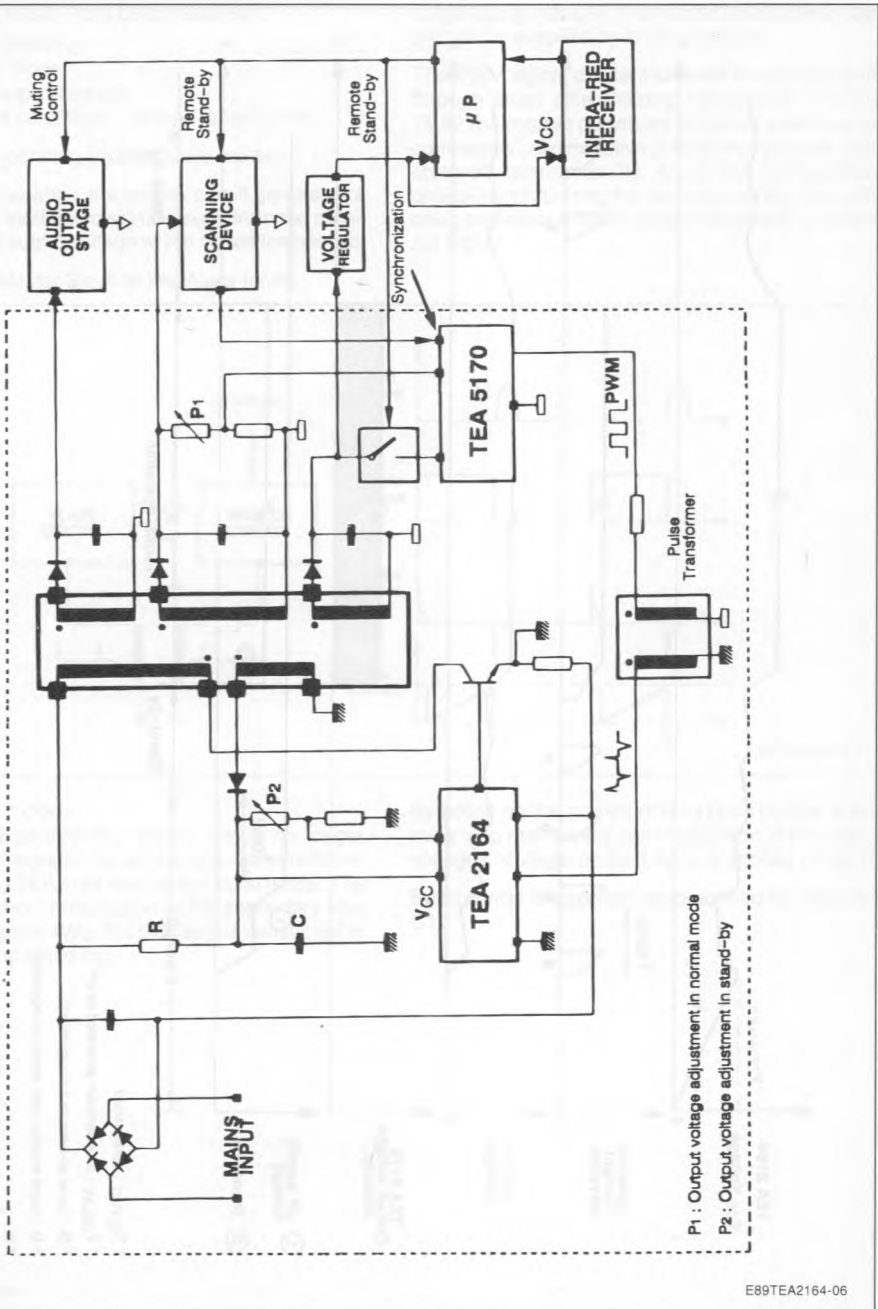
Figure 3 : System Description Waveforms.

* T_{BURST} : burst period
* T_{DELAY} : time constant generated by μP
* B : burst envelop (out of regulation)
* b : burst envelop (with stand–by regulation)
* t1
* t2

 commands issued by μP

E89TEA2164-07

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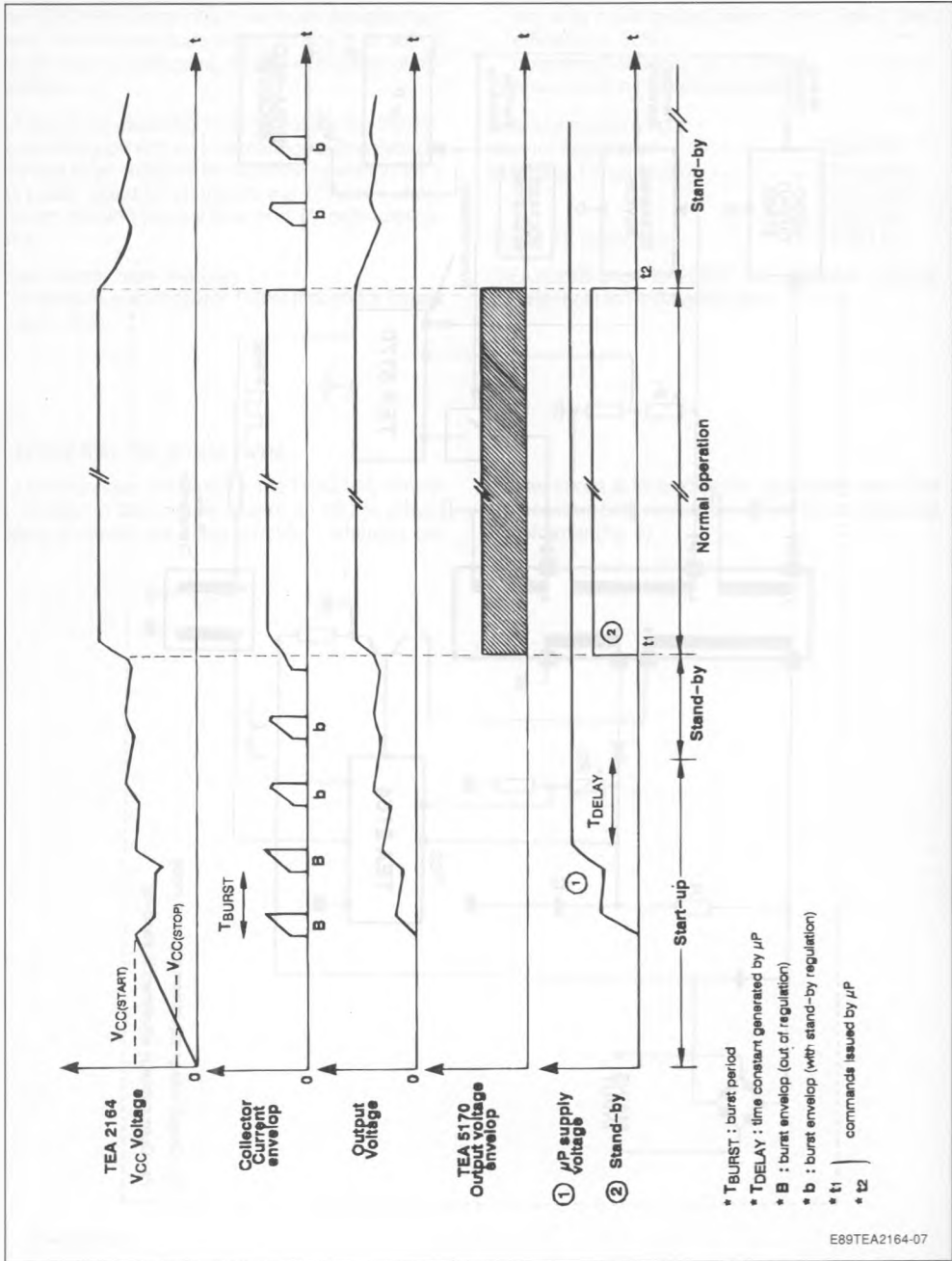
In the operation of the master-slave architecture, four majors cases must be considered :

- normal operating
- stand-by mode
- power supply start-up
- abnormal conditions : off load, short circuit, ...

a) Normal operating (master slave mode)

In this configuration, the master circuit generates a pulse width modulated signal issued from the monitoring of the output voltage which needs the best accuracy (in TV applications : the horizontal deflection stage supply voltage). The master circuit power supply can be supplied by another output.

The PWM signal are sent towards the primary side through small differentiating transformer. For the TEA2164 positive pulses are transistor switching-on commands ; and negative pulses are transistor switching-off commands (fig. 4). In this configuration, only by synchronizing the master oscillator, the switching transistor may be synchronized with an external signal.

Figure 4 : Master Slave Mode Wave-forms.
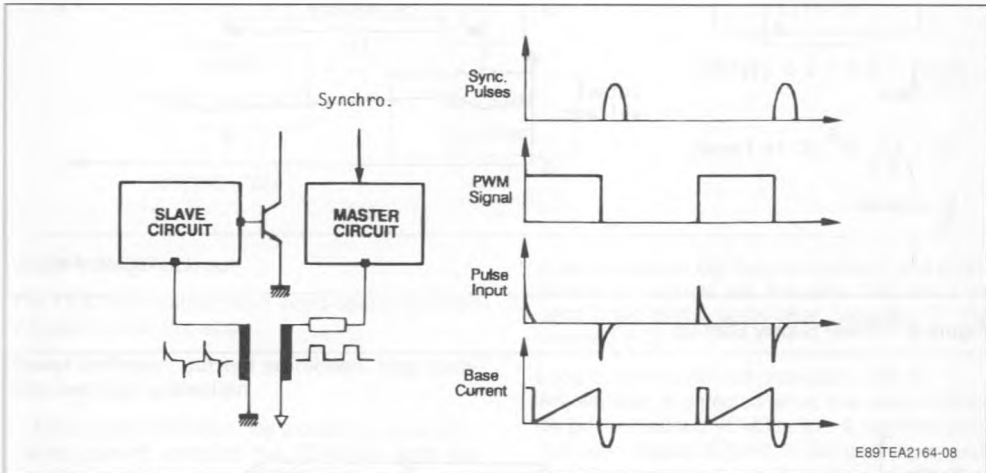
b) Stand by mode

In this configuration the master circuit no longer sends PWM signals, the structure is not synchronized ; and the TEA2164 operates in burst mode. The average power consumption at the secondary side may be very low $1W \leq P \leq 6W$ (as it is consumed in TV set during stand by).

By action on the maximum duty cycle control, a primary loop maintains a semi-regulation of the output voltages. Voltage on feed-back is applied on pin 9.

Burst period is externally programmed by capacitor C1.
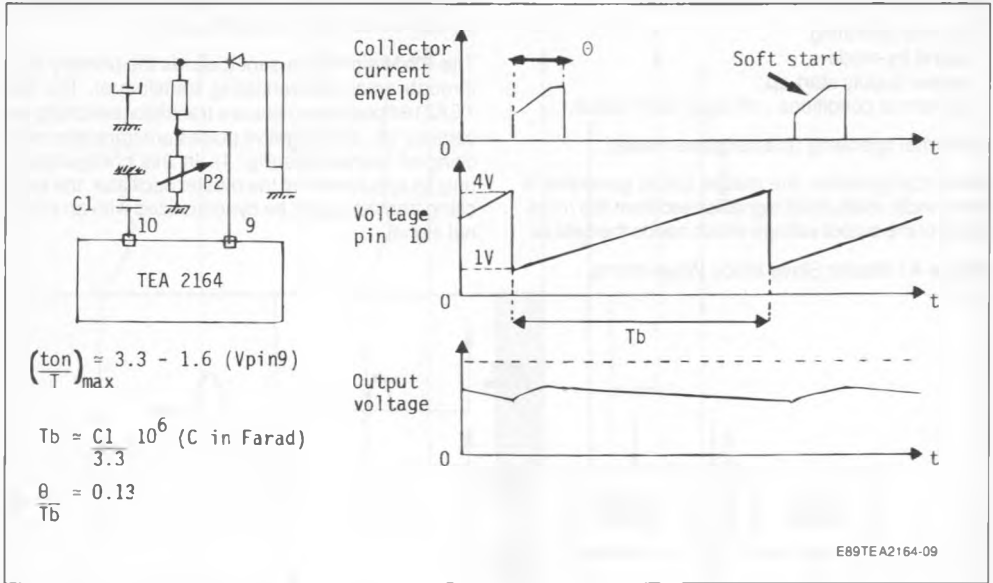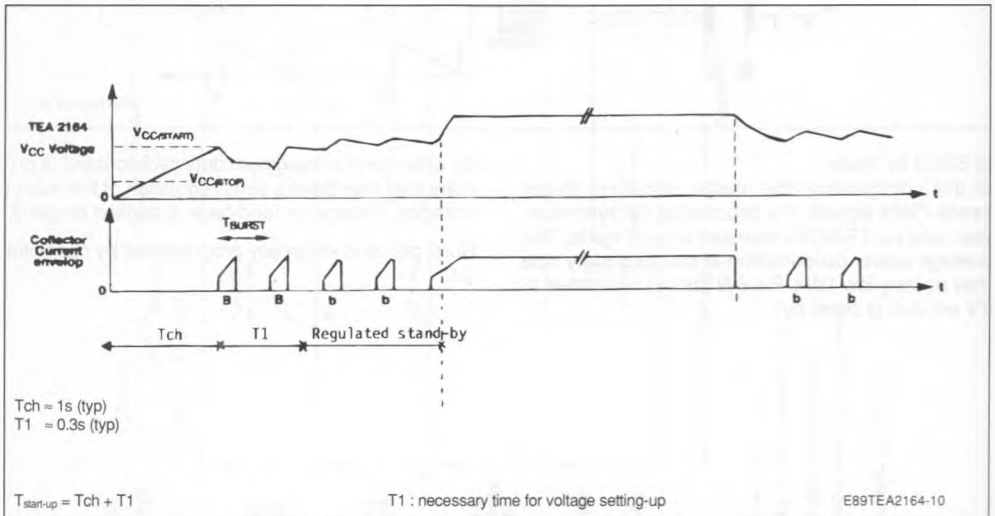
Figure 5 : Burst Mode Waveforms.

$$\left(\frac{ton}{T}\right)_{max} \simeq 3.3 - 1.6\ (Vpin9)$$

$$Tb \simeq \frac{C1}{3.3}\ 10^6\ (C\ in\ Farad)$$

$$\frac{\theta}{Tb} \simeq 0.13$$

E89TEA2164-09

Figure 6 : Power Supply Start-up.

Tch ≈ 1s (typ)
T1 ≈ 0.3s (typ)

$T_{start-up} = Tch + T1$ T1 : necessary time for voltage setting-up   E89TEA2164-10

c) Power supply start-up

After the mains have been switched-on, the Vcc storage capacitor of the TEA2164 is charged through a high value resistor connected to the rectified high voltage. When Vcc reaches Vcc start threshold (9V typ), the TEA2164 starts operating in burst mode. Since available output power is low in burst mode the output power consumption must remain low before complete setting-up of output voltage. In TV application it can be achieved by maintaining the TV in stand-by mode during start-up (fig. 6).

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d) Abnormal conditions : safety functions

Overvoltage protection
When Vcc exceeds Vcc max, an internal flip-flop stops output conduction signals. The circuit will start again after the capacitor C1 discharge ; it means :

after loss of synchronization or after Vcc stop crossing (fig. 7).

In flyback converters, this function protects the power supply against output voltage runaway.

Figure 7 : Over Voltage Lock-out.
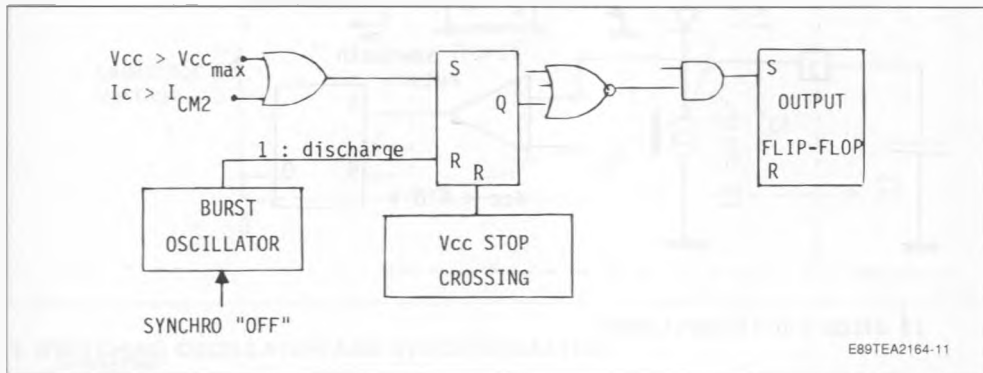
Under voltage lock-out

The TEA2164 control circuit stops operating when Vcc goes under Vcc stop.

Power limitation, current protection, long duration overload protection

· Output power limitation : by a pulse by pulse collector current limitation the TEA2164 limits the maximum output power. VCM1 is the corresponding voltage threshold, its detection is memorized up to the next period.

· Current protection (transistor protection)
Under particular conditions a hard overload or short circuit may induce a flux runaway in spite of the current limitation (VCM1).

The TEA2164 control circuit features a second current protection, VCM2. When this threshold is reached an internal flip-flop memorizes it and output conduction signals are inhibited. The circuit will send base drives again after capacitor C1 discharge(fig 7).
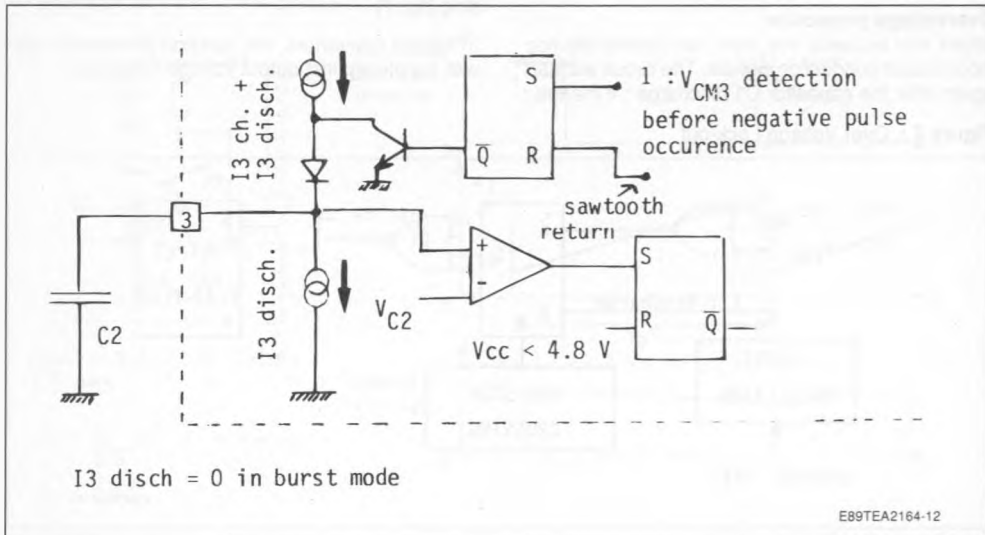
- Long duration overload protection : (fig. 8)
An overload is detected when the sense-voltage on pin 11 reaches VCM3 before a negative pulse has been applied to pin 6. In this case the capacitor C2 (connected to pin 3) is charged with I3 ch up to the end of the period and discharged with I3 disch until a next VCM3 detector. By this way in case of long duration overload, the capacitor keeps charging at each period and its voltage encreases gradually. When the voltage on pin 3 exceeds VC2, the TEA2164 control circuit stops sending base drives and memorizes this event. No restart is allowed as long as Vpin 3 is higher than VC2 and Vcc higher than 4.8V.

Figure 8 : Long Duration Overload Monitoring Circuit.

I3 disch = 0 in burst mode

E89TEA2164-12

* Remark :

- The harder is the overload the faster is the protection
- The capacitor keeps charging between two burst after VCM2 detection.

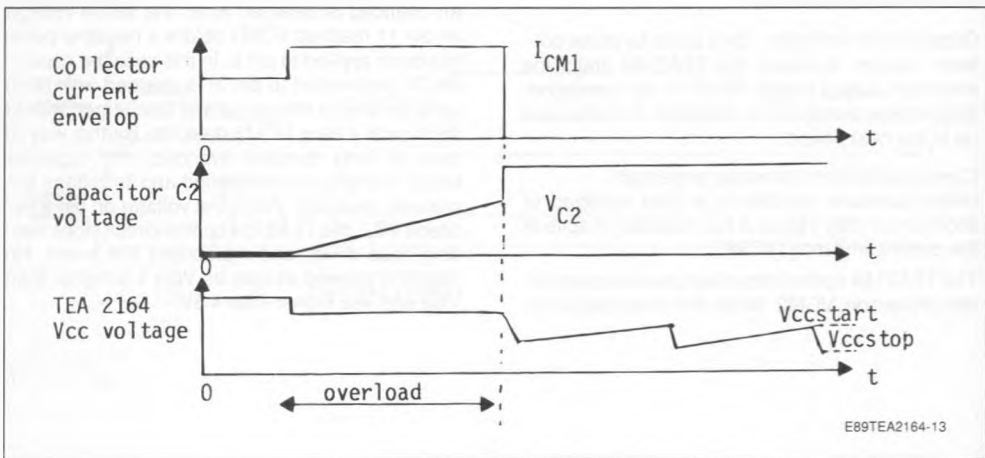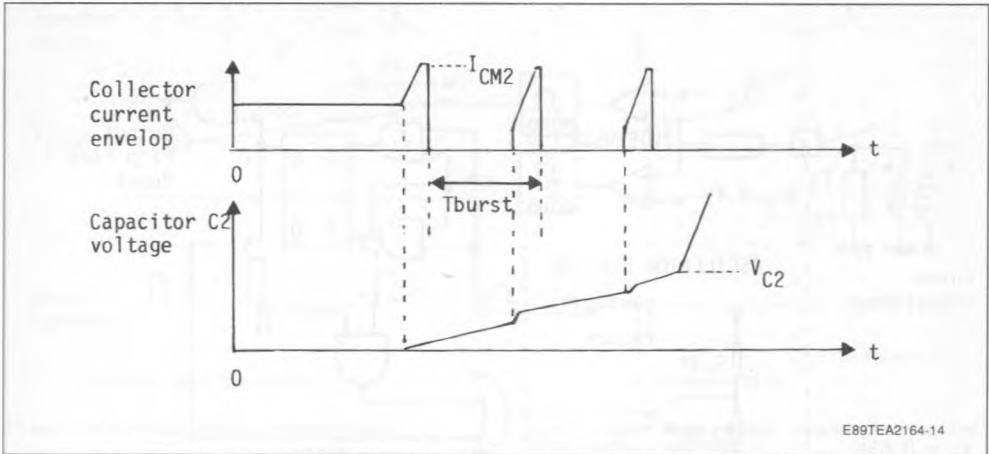**Figure 9 :** Long Duration Over-load Detection.

E89TEA2164-13

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Figure 10 : Repetive Over-current Protection.
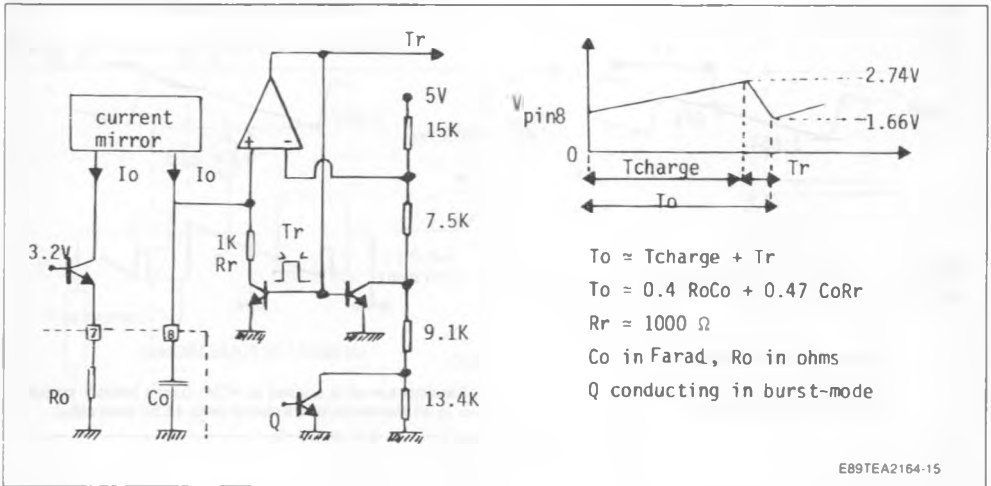

3. SWITCHING OSCILLATOR AND SYNCHRONIZATION

- Switching oscillator

When the TEA2164 control circuit operates in burst mode, the switching frequency is fixed by the free frequency oscillator. The period is determined by two external components Co and Ro.

Figure 11 : Free Frequency Running.

$To \simeq Tcharge + Tr$

$To \simeq 0.4\ RoCo + 0.47\ CoRr$

$Rr \simeq 1000\ \Omega$

Co in Farad, Ro in ohms
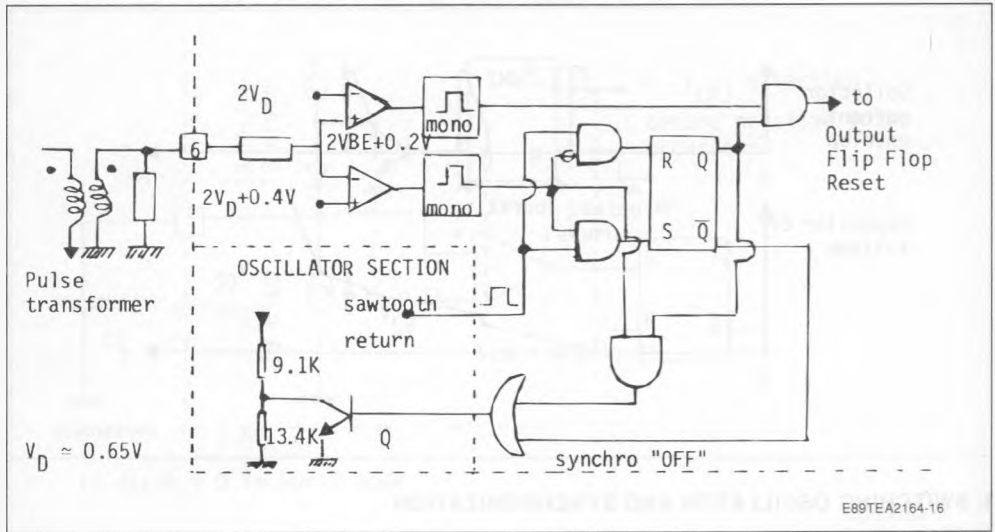
Q conducting in burst-mode

- Synchronization

When the master-circuit starts to send pulses both oscillators are not synchronous. In order to avoid any erratic conduction of the power transistor, the first synchronization will be taken into account when a positive synchronization pulse will arrive simultanously with the sawtooth return of the TEA2164 oscillator.
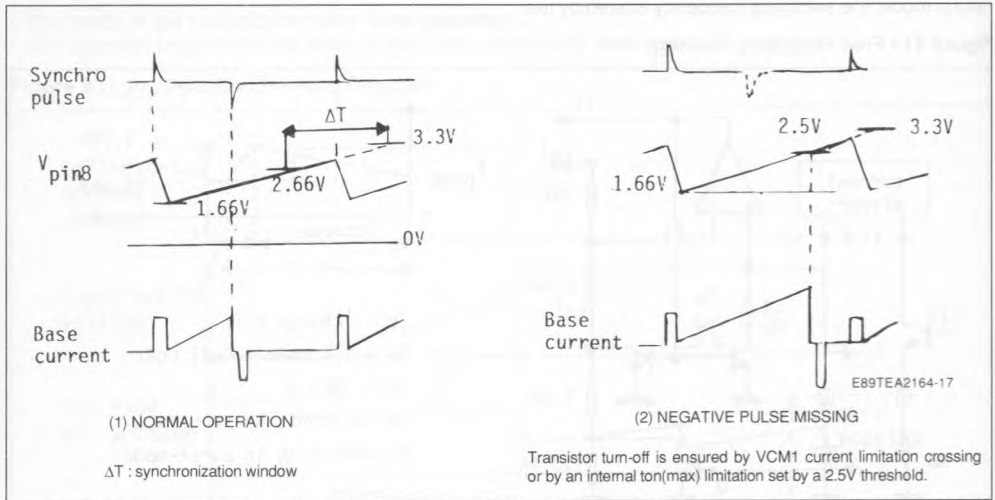
To get synchronization the free frequency must be higher than the synchronization frequency.
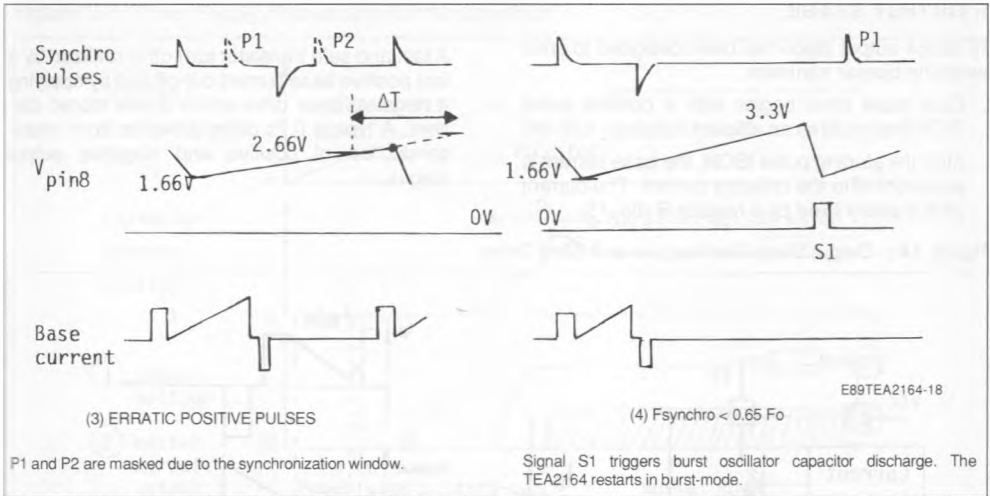
$$To < Tsync. < 1.50\ To$$

Figure 12 : Synchronization Pulse Shaper and Synchronization.

- Operation after synchronization

(1) NORMAL OPERATION

ΔT : synchronization window

(2) NEGATIVE PULSE MISSING

Transistor turn-off is ensured by VCM1 current limitation crossing or by an internal ton(max) limitation set by a 2.5V threshold.

(3) ERRATIC POSITIVE PULSES

P1 and P2 are masked due to the synchronization window.

(4) Fsynchro < 0.65 Fo

Signal S1 triggers burst oscillator capacitor discharge. The TEA2164 restarts in burst-mode.

E89TEA2164-18

Cases (2) (3) (4) do not occur in normal operating.

4. MAXIMUM DUTY CYCLE LIMITATION

Burst mode : The maximum duty cycle is controlled by the voltage on pin 9 (fig. 13).

Synchronized mode : Normally the maximum duty cycle is set by the master circuit. However the maximum conducting time will never exceed the value given by the comparison of the oscillator wave-form with the 2.5V internal threshold.

Figure 13 : Maximum Duty Cycle Limitation.

$$V1 = 4.5V - 1.25 \times (e) \; ; \; Io = \frac{2.5V}{Ro}$$

E89TEA2164-19
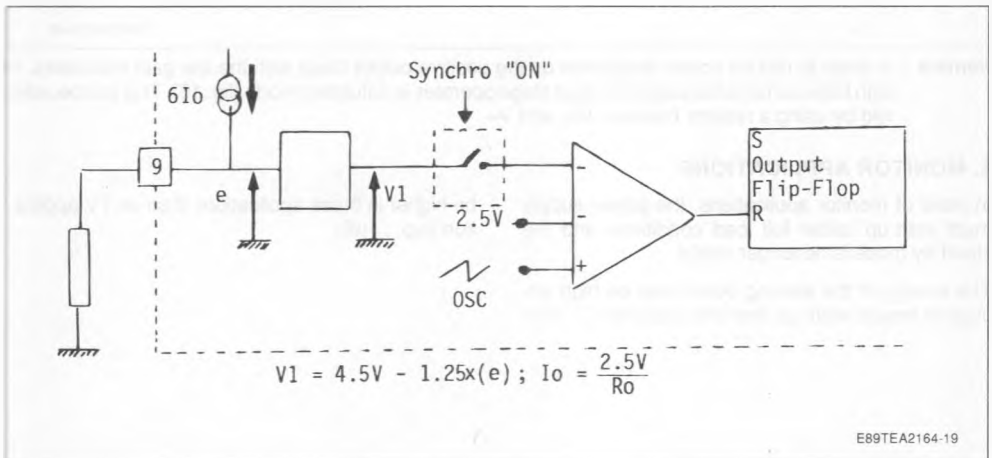
5. OUTPUT STAGE

TEA2164 output stage has been designed to drive switching bipolar transistor.

- Each base drive begins with a positive pulse IBON that realizes an efficient transistor turn-on.

- After the starting pulse IBON, the base current is proportional to the collector current. The current gain is easily fixed by a resistor R (fig. 15).

- A fast and safe transistor turn-off is realized by a fast positive base current cut-off and by applying a negative base drive which draws stored carriers. A typical 0.7s delay prevents from cross-conduction of positive and negative output stages.

Figure 14 : Output Stage Architecture and Base Drive.

E89TEA2164-20
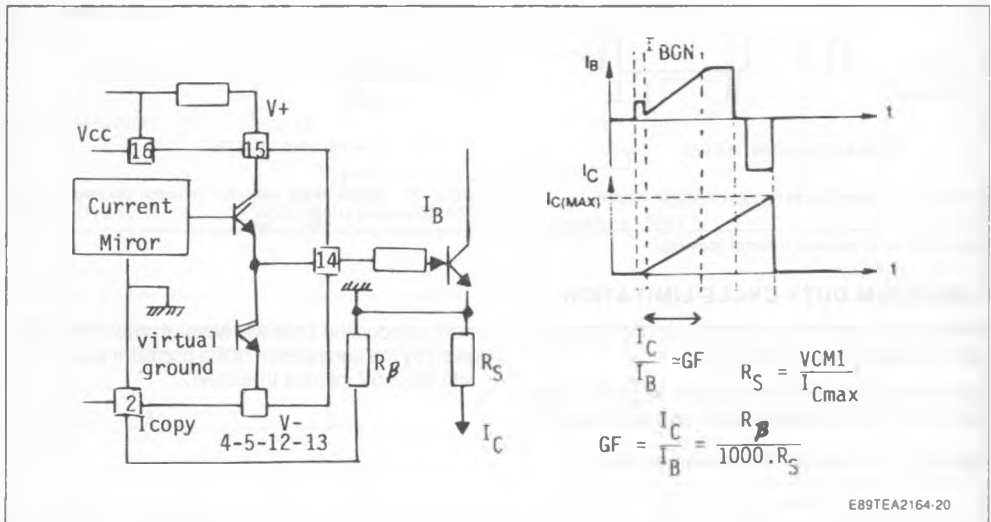
Remark : In order to reduce power dissipation on the positive output stage with the low gain transistors, for high base currents the positive output stage operates in saturated mode (fig. 15). This can be achieved by using a resistor between Vcc and V+.
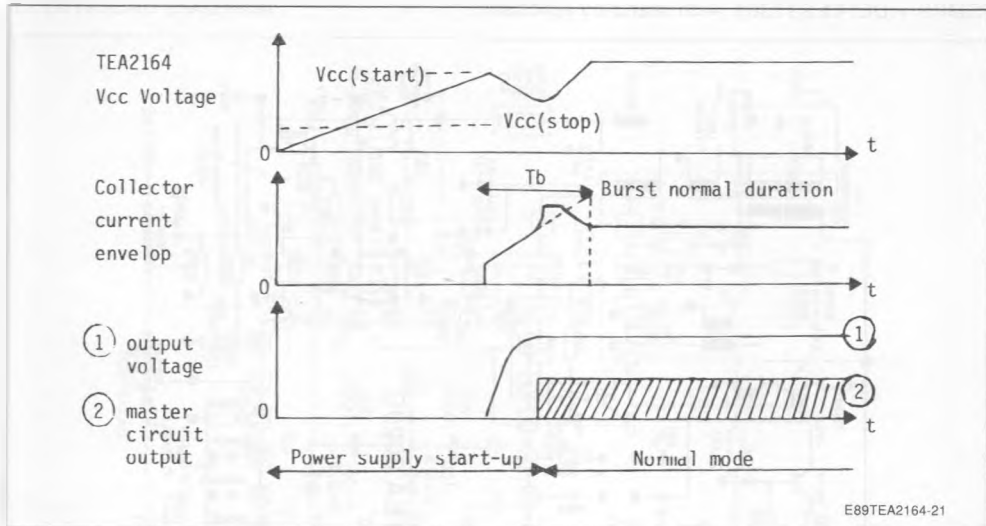
6. MONITOR APPLICATIONS

In most of monitor applications, the power supply must start-up under full load conditions and the stand-by mode is no longer useful.
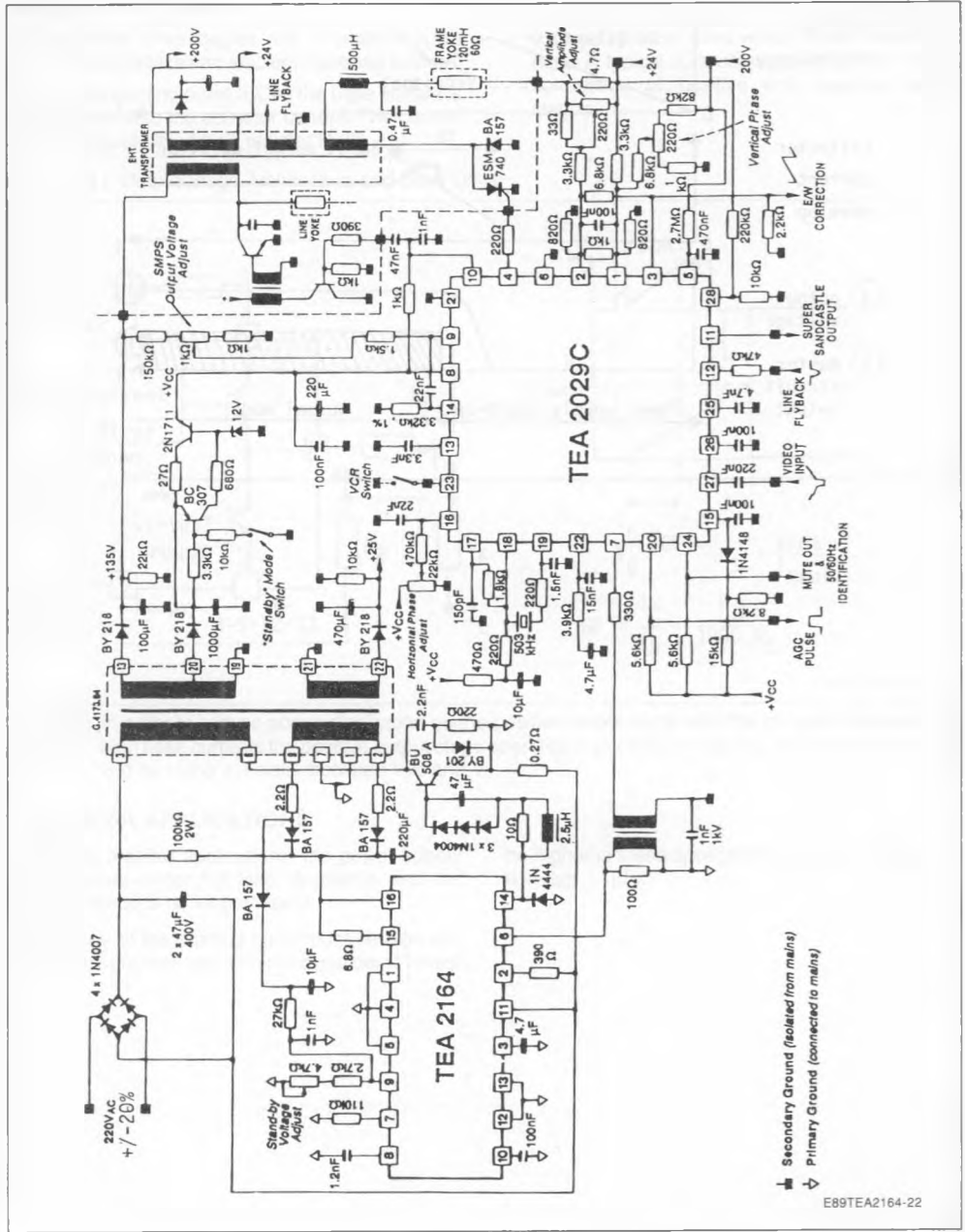
The energy of the starting burst must be high enough to ensure start-up, then the capacitor C1 must be higher in these applications than on TV application (typ. : 1μF).

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Figure 15 : Power Supply Start-up and Normal Operation.

COMPLETE APPLICATION DIAGRAM
(SMPS + DEFLECTION) (with stand-by function)

E89TEA2164-22

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STAND-ALONE 32 KHz POWER SUPPLY
ELECTRICAL DIAGRAM

E89TEA2164-23

PACKAGE MECHANICAL DATA

16 PINS - PLASTIC DIP

mm

e = 2,54 (2)

5.08 max.

4.57 max.

3.1 / 3,9

0.38 / 0.508

1.77 max.

8.5 max.

0.51 min.

0.2 / 0,3

7.62 (2)

0° / 15°

Datum

Or

22.44 max.

6.35 (1)

(1) Nominal dimension
(2) True geometrical position

16 pins

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