DATA SHEET

TDA9715H/A
Y/C one-chip processor (VHS standard)

Product specification
Supersedes data of August 1993
File under Integrated Circuits, IC02

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Philips Semiconductors

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Y/C one-chip processor (VHS standard) TDA9715H/A

FEATURES

- Luminance Noise Reduction (YNR)
- Chrominance Noise Reduction (CNR)
- Saturation dependent writing current control (CACC)
- Integrated filter
- Simple SVHS playback
- Skew output for long-play TRICK mode.

GENERAL DESCRIPTION

The TDA9715H/A is an integrated circuit for chrominance and luminance processing (record and playback) in VHS tape recorders for the TV standard PAL, NTSC, SECAM/ME (4.43 MHz chrominance systems).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.5	V
I_{CC}	supply current	V_{CC} = 5 V	–	200	mA
T_{amb}	operating ambient temperature		–20	+70	°C
T_{stg}	storage temperature		–25	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9715H/A	QFP80	plastic quad flat package; 80 leads (lead length 1.6 mm); body 14 × 20 × 3.0 mm	SOT310-1

BLOCK DIAGRAM

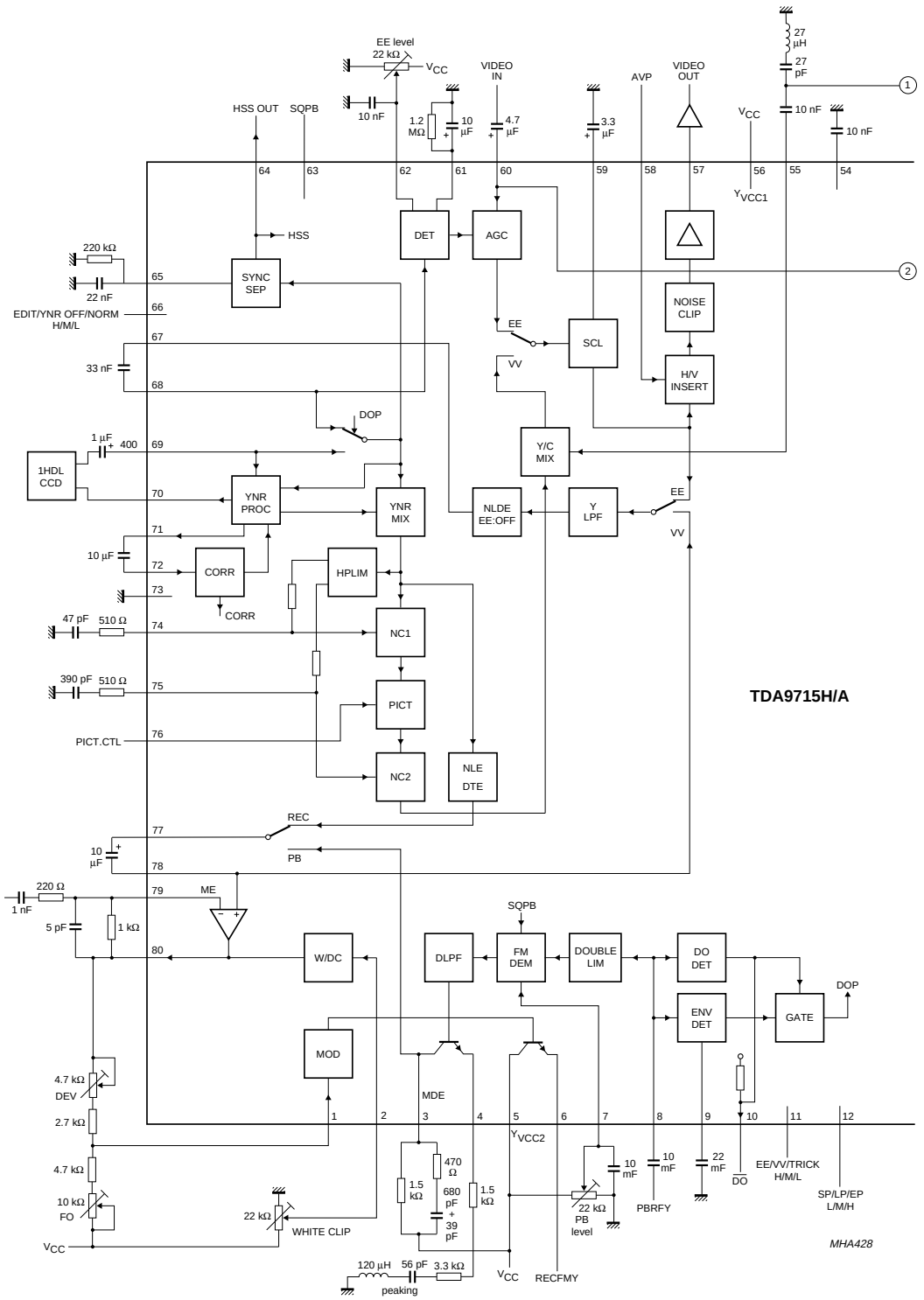


Fig.1 Block diagram (continued in Fig.2).

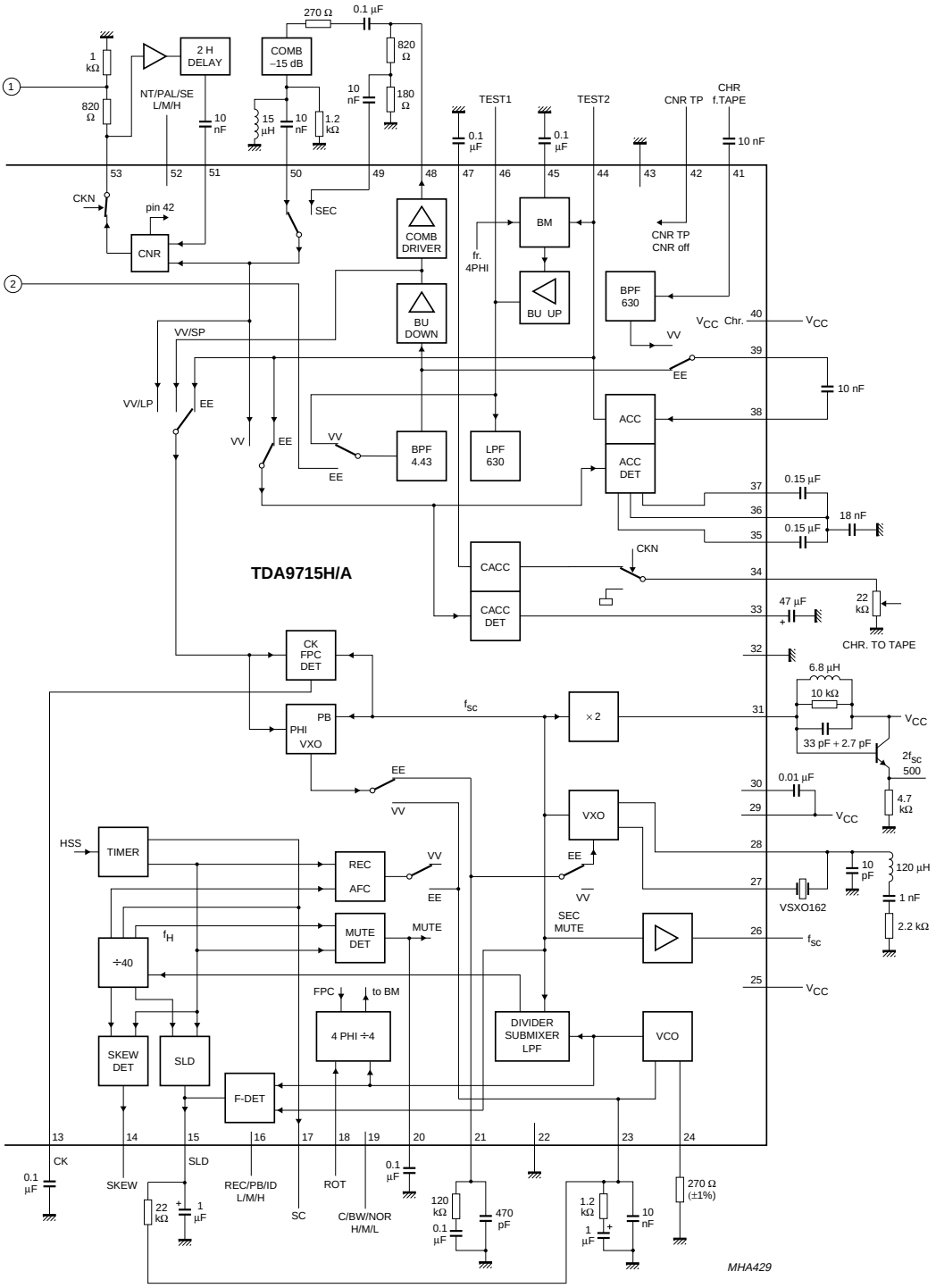


Fig.2 Block diagram (continued from Fig.1).

FUNCTIONAL DESCRIPTION

Record/Electric-to-Electric (REC/EE) mode

LUMINANCE

The CVBS signal appears at the output pin 57 and at the internal Y Low-Pass Filter (YLPF) via pin 60 and Automatic Gain Control (AGC) stage. Exempt from chrominance, the luminance signal is fed first to the sync separator stage to obtain the separated sync pulse at pin 64 and secondly via Non-Linear Emphasis (NLE), main emphasis, white-dark clip and FM modulator to the FM output pin 6.

CHROMINANCE

Exempt from the luminance signal in the internal 4.43 MHz band-pass filter and controlled by the Automatic Chrominance Control (ACC) stage the chrominance signal is mixed in the band mixer with a 4-phase shifted 5.06 MHz signal, produced by the internal adjustment-free oscillator. The formed $N \times f_H$ signal is fed via an internal low-pass filter and CACC to the output at pin 34.

Playback/Video-to-Video (PB/VV) mode

LUMINANCE

The FM signal is fed to the FM demodulator stage and the internal sub low-pass filter (DLPF) via input pin 8 and the double limiter. After passing main de-emphasis, Non-Linear De-emphasis (NLDE) and the luminance Noise Reduction (YNR) the signal is fed first to the sync separator stage and then (via picture control stage) mixed with the chrominance signal. This CVBS signal is output at pin 57.

CHROMINANCE

The internal $N \times f_H$ band-pass filter (BPF 627 kHz) and the ACC stage the signal is mixed in the band mixer with a 4-phase shifted 5.06 MHz signal, produced by the internal adjustment-free oscillator via input pin 41. The formed f_{SC}-chrominance signal is fed via internal BPF 4.43 MHz, external comb filter and internal Chrominance Noise Reduction (CNR) to the internal Y/C mixer.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		–	–	5.5	V
V_{65}	voltage V_{65}	referenced to GND	–	–	4.5	V
V_I	input voltage V_{68}, V_{69}, V_{78}	referenced to GND	–	–	4.1	V
V_n	input voltage on all other pins		0	–	V_{CC}	V
I_O	output currents $-I_4$, $-I_6$, $+I_{24}$, $-I_{39}$, $-I_{57}$, $-I_{67}$, $-I_{71}$, $-I_{77}$, $-I_{80}$		–	–	10	mA
P_{tot}	total power dissipation	see Fig.3	–	1887	–	mW
T_{stg}	storage temperature		–25	–	+150	°C
T_{amb}	operating ambient temperature	see Fig.3	–20	–	+70	°C
V_{es}	electrostatic handling for all pins	note 1	–300	–	+300	V

Note

1. Charge device model class B: equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.

QUALITY SPECIFICATION

In accordance with *"URV-4-2-59/601"*.

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = +25 °C and typical application (see Figs 1 and 2), unless otherwise specified.
Luminance part: All amplitudes are VBS peak-to-peak values, unless otherwise specified.
Chrominance part: All amplitudes for PAL and NTSC are red values with 75% saturation and chrominance-to-burst ratio of 2.2 : 1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	4.95	5.5	V
I_P	current consumption ($I_5 + I_{25} + I_{29} + I_{40} + I_{56}$) at PB/VV		140	165	200	mA
I_R	current consumption ($I_5 + I_{25} + I_{29} + I_{40} + I_{56}$) at REC/EE		130	150	180	mA
Modulator input (pin 1)						
φ	sensitivity		10	12.5	15	kHz/μA
White clip control (pin 2; open base)						
CTLφ	control sensitivity		60	80	100	%/V
Main de-emphasis output (pin 3; open collector)						
V_3	DC voltage	FM input = 3.8 MHz; V_7 = 1.7 V	2.5	3.0	3.5	V
$V_{s3(p-p)}$	video signal (peak-to-peak value)	V_7 = 1.7 V	230	300	370	mV
DEMφ	demodulator sensitivity	normal VHS mode; V_7 = 1.7 V	0.23	0.3	0.37	V/MHz
		SQPB mode	0.14	0.19	0.24	V/MHz
LIN_3	demodulator linearity $\frac{V_0(5\ MHz) - V_0(4\ MHz)}{V_0(4\ MHz) - V_0(3\ MHz)}$	VHS mode	0.95	0.98	1.01	
	demodulator linearity $\frac{V_0(9\ MHz) - V_0(7\ MHz)}{V_0(7\ MHz) - V_0(5\ MHz)}$	SVHS mode	0.9	0.98	1.05	
α	suppression of demodulator carrier $\frac{V(4\ MHz)}{V(2\ MHz)}$	measured with FM input = 2 MHz	40	–	–	dB
f_b	boundary frequency for demodulating	V_7 = 1.2 V	10	–	–	MHz
Main de-emphasis and peaking (pin 4; open emitter)						
V_4	DC voltage	FM input = 3.8 MHz; V_7 = 1.7 V	1.7	2.0	2.3	V
$V_{s4(p-p)}$	video signal (reverse) (peak-to-peak value)	V_7 = 1.7 V	230	300	370	mV
Supply voltage (pin 5)						
I_{SP}	DC current PB		13	–	19	mA
I_{5R}	DC current REC		8	–	14	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM output (pin 6)						
V_{o6}	output mean value of DC voltage	R_L = 1 kΩ	3.0	3.3	3.6	V
$V_{s(p-p)}$	output signal voltage (peak-to-peak value)	R_L = 1 kΩ	0.7	0.9	1.1	V
f_o	output frequency	I_1 = 304 μA	3.4	3.8	4.2	MHz
α	second distortion level	f = 4 MHz	–	–50	–42	dB
Δf	carrier down frequency	NTSC mode	320	400	480	kHz
LIN_6	modulator linearity $\frac{I_1(6\ MHz) - I_1(4\ MHz)}{I_1(4\ MHz) - I_1(2\ MHz)}$		0.98	1.00	1.02	
f_{mod}	modulator frequency range		1.5	–	10	MHz
Demodulator gain control (pin 7; open base)						
V_7	active range of gain control		1.2	1.7	2.2	V
CTLφ	control sensitivity	SYNC-white = 100%	65	80	95	%/V
Playback FM input (pin 8)						
V_8	DC voltage		2.7	3.0	3.3	V
$V_{s8(p-p)}$	input signal (peak-to-peak value)		–	350	–	mV
$V_{b(p-p)}$	boundary input range (peak-to-peak value)		10	–	1000	mV
Envelope detector (pin 9)						
V_{D9}	DC range of normal mode		3.0	–	5.0	V
V_{D0}	DC range of drop-out correction (DOC) off mode		0	–	2.0	V
V_9	DC level at no signal		1.8	2.3	2.8	V
G_{env}	envelope detector switch-on level (drop-out active)	0 dB = V_{s8} = 350 mV (p-p); f_i = 3.8 MHz	–13	–10	–7	dB
t_{env}	envelope detector operating time	C_i = 0.022 μF	480	600	720	μs
Drop-out pulse output (pin 10)						
V_{10L}	LOW level DC voltage	V_{s8} = 0 V	0	–	500	mV
V_{10H}	HIGH level DC voltage	V_{s8} = 350 mV (p-p); R_L = 15 kΩ to GND	2.0	2.5	3.0	V
G_{DOC}	DOC-on level	0 dB = V_8 = 350 mV (p-p); f_i = 3.8 MHz	–18	–15	–12	dB
G_{DOF}	DOC-off level (hysteresis)		1	3	5	dB
V_{th}	threshold voltage for forced DO on		0.2	0.7	1.2	V
Switch: EE/VV/TRICK (pin 11)						
V_{EE}	voltage range for active EE		3.5	–	5.0	V
V_{VV}	voltage range for active VV		1.75	–	3.0	V
V_{TR}	voltage range for active TRICK		0	–	1.25	V
V_{11}	DC level	pin open-circuit	4.8	–	5.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switch: SP/LP/EP (pin 12; open PNP base)						
V_{SP}	voltage range for active SP		0	–	1.25	V
V_{LP}	voltage range for active LP		1.75	–	3.0	V
V_{EP}	voltage range for active EP		3.5	–	5.0	V
Colour killer (pin 13)						
V_{13}	DC at no chrominance input		1.6	1.8	2.0	V
V_{CON}	threshold voltage colour on		2.0	2.2	2.4	V
G_{CKON}	colour killer active	relative to nominal input signal V_{s38} = 110 mV (p-p)	–27	–30	–33	dB
G_{HY}	colour killer hysteresis		1	2	3	dB
Skew output (pin 14; NPN collector with 25 kΩ to V_{CC})						
V_{SL}	output voltage skew LOW		–	–	0.8	V
V_{SH}	output voltage skew HIGH		4	–	–	V
Frequency correction output (pin 15)						
I_{SLD}	output current SLD	VV mode; side-lock detector	±12	±17	±22	µA
t_{SLD}	pulse duration	VV mode; side-lock detector; f_H = 15.625 kHz	–	64	–	µs
f_{SLH}	start of detection at positive frequency deviation (referenced to $f_{SC} + N \times f_H$ at pin 46; $-I_{15}$)	VV mode; side-lock detector; PAL	1.0	2.0	3.0	kHz
		VV mode; side-lock detector; NTSC	2.0	4.0	5.0	kHz
f_{SLL}	start of detection at negative frequency deviation (referenced to $f_{SC} + N \times f_H$ at pin 46; $+I_{15}$)	VV mode; side-lock detector; PAL	–3.0	–2.0	–1.0	kHz
		VV mode; side-lock detector; NTSC	–5.0	–4.0	–2.0	kHz
V_{SLO}	operating range	EE and VV mode; frequency detector	0.8	–	4.2	V
I_{FD}	output current of frequency detector		±12	±17	±22	µA
t_{FD}	pulse duration		70	75	80	µs
f_{FDH}	start of detection at positive frequency deviation (referenced to $f_{SC} + N \times f_H$ at pin 46; $-I_{15}$)	EE mode	40	70	100	kHz
f_{FDL}	start of detection at negative frequency deviation (referenced to $f_{SC} + N \times f_H$ at pin 46; $+I_{15}$)	EE mode	–100	–70	–40	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switch: REC/PB/ID (pin 16)						
V_{REC}	voltage range for active REC mode		0	–	1.25	V
V_{PB}	voltage range for active PB mode and FPC on		1.75	2.5	3.0	V
V_{ID}	voltage range for active PB mode and FPC off (ID mode)		3.5	–	5.0	V
V_{16}	DC voltage level	pin open-circuit	4.8	–	5.0	V
Sandcastle, BGP output (pin 17; active LOW; SC with external 20 kΩ resistance to GND); note 1						
t_{BGP}	duration of BGP		4.2	4.45	4.7	µs
t_{BGS}	start of BGP beyond sync start at pin 64		3.25	3.5	3.75	µs
V_{BGI}	LOW level DC voltage (BGP)	I_{17} = 1 mA	–	–	0.5	V
V_{med}	medium level DC voltage (horizontal blanking)	I_{17} = –0.2 mA	1.8	2.2	2.6	V
V_{HI}	HIGH level DC voltage (inactive)	I_{17} = –0.4 mA	4.0	4.4	–	V
V_{BGPO}	voltage for BGP not active	BGP with external 20 kΩ resistance to V_{CC}	4.6	–	–	V
V_{BGPA}	voltage for BGP active		–	–	0.6	V
Rotary pulse (pin 18; open PNP base)						
V_{C2}	voltage for –90° phase rotation (channel 2)		0	–	2.25	V
V_{C1}	voltage for non-rotation (PAL) or +90° rotation (NTSC) (channel 1)		2.75	–	5.0	V
Switch: C/BW/NORM (pin 19; open PNP base)						
V_{fCON}	voltage for forced colour on (C)		3.5	–	5.0	V
V_{fCOF}	voltage for forced colour off (BW)		1.75	–	3.0	V
V_{NORM}	voltage for NORM mode		0	–	1.25	V
Mute detector (pin 20)						
V_C	voltage at coincidence		3.5	–	–	V
V_{NC}	voltage at no coincidence (mute)		–	–	1.5	V
V_{MUTE}	threshold voltage to switch VXO to VV mode		2.2	–	2.8	V
Loop filter (EE) VXO (pin 21)						
V_{21}	DC level		1.0	2.4	3.6	V
β	VXO sensitivity		1.0	1.6	2.2	Hz/mV
f_{PRU}	upper pull-in range		0.8	1.3	1.8	kHz
f_{PRL}	lower pull-in range		–1.8	–1.3	–0.8	kHz
Loop filter VCO (pin 23)						
V_{23}	DC voltage level	EE mode	1.3	2.1	2.9	V
β	VCO sensitivity (f_H related)	EE mode	17	19	21	kHz/V
	VCO sensitivity (f_{SC} related)	VV mode	680	760	840	kHz/V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCO bias current (pin 24)						
V_{24}	DC voltage level		0.5	V_{BE}	0.8	V
R_{24}	external resistance to ground		267	270	273	Ω
Supply voltage VCO (pin 25)						
I_{25}	DC current		4.5	–	6.5	mA
f_{SC} output (pin 26)						
V_{26}	DC voltage level		1.8	2.3	2.8	V
$V_{s26(p-p)}$	output signal (peak-to-peak value)		500	600	700	mV
α_2	second distortion		–	–	–25	dB
α_3	third distortion		–	–	–20	dB
Δf_i	deviation of oscillator frequency (due to internal spread)	VV mode	–	–	±50	Hz
Δf_B	deviation of oscillator frequency (video signal without burst applied)	EE mode	–	–	±1.4	kHz
Δf_C	deviation of oscillator frequency (no video signal applied)	EE/MUTE/blueback option	–	–	±100	Hz
Δf_{VT}	deviation of frequency due to supply voltage from 4.5 to 5.5 V and T_{amb} from –20 to +70 °C	VV mode	–	–	±100	Hz
VXO (crystal output) (pin 27)						
V_{27}	DC voltage level		3.1	3.5	3.9	V
VXO (crystal input) (pin 28)						
V_{28}	DC voltage level		2.6	3.0	3.4	V
Supply voltage VXO (pin 29)						
I_{29}	DC current level		10	–	17	mA
Filter reference terminal (chrominance filter) (pin 30)						
V_{30}	active range of DC voltage level when controlling		2.5	3.0	3.5	V
2 × f_{SC} output (pin 31; open NPN collector)						
V_{31}	DC voltage level		4.5	5.0	–	V
$V_{s31(p-p)}$	output signal (peak-to-peak value)	1 kΩ connected to V_{CC} and emitter follower (EF)	40	55	70	mV
α	second distortion	tuned LC circuit (Q > 20) and EF	–	–	–30	dB
Loop filter CACC (pin 33; loading via EF) (see Fig.5)						
V_{C-B}	DC voltage level	chrominance/burst = 2.2	2.0	2.5	3.0	V
V_{CTR}	control range		1.0	–	3.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CACC output (pin 34) see Fig.5 and Table 8						
V_{COF}	DC voltage level at colour on		2.1	2.4	2.7	V
V_{CON}	DC voltage level at active colour killer	EE or VV mode	–	0.1	0.3	V
$V_{s34(p-p)}$	chrominance output signal ($N \times f_H$) (peak-to-peak value)		467	660	932	mV
ΔG_{34}	maximum CACC gain $\Delta V_{34}/V_{46}$ ($N \times f_H$)		–	2.7	–	dB
$\alpha_{2, 3}$	second, third distortion	V_{s46} = 0 dB	–	–	–40	dB
		V_{s46} = +6 dB	–	–	–35	dB
α_{ck}	colour killer suppression		40	–	–	dB
$G_{1.5}$	1.5 dB up gain	see Table 9	1.0	1.5	2.0	dB
α_{cr}	crosstalk CVBS signal		–	–	–40	dB
ACC loop filter switch (channel 2) (pin 35; open NPN collector; non-conducting during VV TRICK)						
R_{35}	output resistance, VV and EE input switched to ground while ROT (pin 18) HIGH		–	–	200	Ω
$t_{att/rec}$	attack and recover time	input signal 0 to 6 dB	50	–	100	lines
		–6 to 0 dB	50	–	100	lines
		–12 to –6 dB	50	–	100	lines
ACC loop filter (pin 36)						
t	attack time (TRICK mode)	0 to 6 dB	4	–	8	lines
	recover time (TRICK mode)		9	–	15	lines
	attack time (TRICK mode)	–6 to 0 dB	4	–	8	lines
	recover time (TRICK mode)		9	–	15	lines
	attack time (TRICK mode)	–12 to –6 dB	4	–	8	lines
	recover time (TRICK mode)		9	–	15	lines
ACC loop filter switch (channel 1) (pin 37; open NPN collector; non-conducting during VV TRICK)						
R_{37}	output resistance, VV and EE input switched to ground while ROT (pin 18) LOW		–	–	200	Ω
$t_{att/rec}$	attack and recover time	input signal 0 to 6 dB	50	–	100	lines
		–6 to 0 dB	50	–	100	lines
		–12 to –6 dB	50	–	100	lines
ACC input (pin 38) (see Fig.6)						
V_{38}	DC voltage level		1.1	1.6	2.1	V
$V_{s38(p-p)}$	input signal (peak-to-peak value)		11	110	310	mV
f_B	bandwidth (–3 dB) upper cut-off frequency		10	–	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BPF switch output (pin 39; EE mode: from BPF 4.43 MHz; VV mode: from BPF 630 kHz)						
V_{39}	DC voltage level	EE mode	1.9	2.4	2.9	V
		VV mode	2.5	3.0	3.5	V
G	gain $\frac{V_{39}}{V_{41}}$	VV mode; f = 630 kHz	–1	0	+1	dB
$V_{s39V(p-p)}$	output signal (peak-to-peak value)	VV mode	–	110	310	mV
$V_{s40E(p-p)}$	output signal (peak-to-peak value)	EE mode	121	135	149	mV
α_{cr}	switch crosstalk EE → VV or VV → EE		–	–	–45	dB
$\alpha_{2, 3}$	second, third distortion	0 dB input signal	–	–	–40	dB
		6 dB input signal	–	–	–35	dB
Supply voltage (pin 40)						
I_{40E}	DC current	EE mode	60	–	85	mA
I_{40V}	DC current	VV mode	60	–	85	mA
PB chrominance from tape (pin 41)						
V_{41}	DC voltage level		1.7	2.2	2.7	V
$V_{s41(p-p)}$	input signal (chrominance) (peak-to-peak value)		–	110	310	mV
CNR test pin (pin 42; NPN EF with internal current source of 50 μA)						
V_{42}	DC voltage level		2.4	3.0	3.6	V
α	second distortion	external resistor 10 kΩ to GND	–	–	–35	dB
$V_{OUs(p-p)}$	limited output signal (peak-to-peak value)	CNR on	225	275	350	mV
V_{CNRO}	CNR off mode		4.8	–	V_{CC}	V
TEST PIN 2 (pin 44)						
V_{44}	DC voltage level		1.75	2.25	2.75	V
$V_{OUs(p-p)}$	controlled output signal (peak-to-peak value)		340	440	540	mV
G_{o44}	deviation of output signal	V_{IN} –10 dB/+3 dB	–0.3	–	+0.3	dB
		V_{IN} –15 dB/+6 dB	–0.5	–	+0.5	dB
f_B	bandwidth (–3 dB)		10	–	–	MHz
$\alpha_{2, 3}$	distortion of second, third harmonic with +6 dB signal amplitude atpin 38 or pin 44		–	–	–35	dB
	distortion of second, third harmonic with nominal signal at pin 38 and pin 44		–	–	–40	dB
Mixer balance (pin 45)						
V_{45}	DC voltage level		1.75	2.25	2.75	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TEST PIN 1 (pin 46)						
$V_{SL46(p-p)}$	output signal $N \times f_H$ (peak-to-peak value)	EE mode	80	110	140	mV
$V_{SH46(p-p)}$	output signal $2 \times f_{SC} + N \times f_H$ (peak-to-peak value)	EE mode	80	110	140	mV
α_{EESP}	suppression of $f_{SC} + N \times f_H$	EE mode	38	–	–	dB
	suppression of f_{SC}	EE mode	38	–	–	dB
$BURST_{up}$	burst up at NTSC SP or NTSC EP mode	EE mode	5	6	7	dB
$V_{fsc(p-p)}$	output signal f_{SC} (peak-to-peak value)	VV mode	80	110	140	mV
$V_{fsc+(p-p)}$	output signal $f_{SC} + 2N \times f_H$ (peak-to-peak value)	VV mode	80	110	140	mV
α_{VVSP}	suppression of $f_{SC} + N \times f_H$	VV mode	38	–	–	dB
	suppression of $N \times f_H$	VV mode	38	–	–	dB
V_{46}	DC voltage level	EE and VV mode	1.8	2.2	2.6	V
$\alpha_{2, 3}$	second, third distortion	EE and VV mode; input 0 dB	–	–	–40	dB
		EE and VV mode; input 6 dB	–	–	–35	dB
f_B	bandwidth (–3 dB)	EE and VV mode	10	–	–	MHz
AC coupling (pin 47)						
V_{47}	DC voltage level		1.85	2.2	2.55	V
Output COMB driver (VV) (pin 48)						
V_{48}	DC voltage level		2.0	2.5	3.0	V
$V_{s48N(p-p)}$	output signal (peak-to-peak value)	NTSC	290	350	420	mV
$V_{s48P(p-p)}$	output signal (peak-to-peak value)	PAL, SECAM	520	620	740	mV
f_B	bandwidth (–3 dB)		10	–	–	MHz
$\alpha_{2, 3}$	distortion of second, third harmonic	input signal at pin 46 = 110 mV (p-p)	–	–	–40	dB
		input signal at pin 46 = 220 mV (p-p)	–	–	–35	dB
$BURST_{down}$	burst down	NTSC SP mode	–6.0	–5.0	–4.0	dB
		NTSC EP mode	–5.0	–4.0	–3.0	dB
Through side chrominance input (pin 49)						
V_{49}	DC voltage level		2.2	2.7	3.2	V
$V_{s49(p-p)}$	chrominance input signal (peak-to-peak value)		–	110	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
COMB side chrominance input (pin 50)						
V_{50}	DC voltage level		2.2	2.7	3.2	V
$V_{s50(p-p)}$	input signal (peak-to-peak value)		–	110	–	mV
CNR limiter input (pin 51)						
V_{51}	DC voltage level		0.6	0.8	1.0	V
$V_{s51(p-p)}$	input signal (peak-to-peak value)		–	39	100	mV
Switch: PAL/SECAM/NTSC (pin 52)						
V_{PAL}	voltage range for active PAL mode		1.75	–	3.0	V
V_{SEC}	voltage range for active SECAM mode		3.5	–	5.0	V
V_{NT}	voltage range for active NTSC mode		0	–	1.25	V
V_{52}	DC voltage level	pin open-circuit	4.8	–	5.0	V
Chrominance output (pin 53)						
V_{53}	DC voltage level		2.5	3.0	3.5	V
V_{sout}	output signal	input signal pin 49 or pin 50 = 110 mV (p-p)	700	880	1060	mV
α_{ck}	colour killer suppression		40	–	–	dB
α_{SEC}	crosstalk from inactive comb-side	V_{s50} = 110 mV (p-p)	–	–40	–30	dB
K	CNR K factor	input signal pin 50 = 4 mV (p-p); CNR on/off	0.55	0.65	0.75	–
G_{51-53}	amplification –20lgK	input signal pin 51 = 1.4 mV (p-p)	24	27	30	dB
α_{CNR}	CNR second distortion	input signal pin 51 = 39 mV (p-p)	–	–35	–25	dB
Filter reference terminal (luminance filter) (pin 54; open base and collector)						
V_{54}	active range of DC voltage when controlling		1.8	2.5	3.2	V
PB chrominance input (pin 55)						
V_{55}	DC voltage level		1.7	2.0	2.3	V
$V_{s55(p-p)}$	input signal (peak-to-peak value)		–	400	–	mV
V_{th}	threshold level of AGCKP1		2.6	3.0	3.4	V
Supply voltage Y (pin 56)						
I_{56R}	DC current	REC mode	40	–	60	mA
I_{56P}	DC current	PB mode	45	–	65	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video output (pin 57)						
V_{SYT}	DC voltage (sync tip)		0.95	1.1	1.25	V
$V_{57(p-p)}$	EE output voltage level (standard output level) (peak-to-peak value)	adjusted at pin 62	–	2.05	–	V
	EE output voltage level (200 IRE) (peak-to-peak value)		2.12	2.22	2.32	V
	VV output voltage level (peak-to-peak value)	V_{68} = 400 mV (p-p)	1.80	2.05	2.30	V
WCSL	white clip suppression level	black-to-white = 100% and TRICK mode	115	135	–	%
$V_{sout(p-p)}$	chrominance output level (peak-to-peak value)	V_{s55} = 0.4 V (p-p)	1.3	1.55	1.8	V
ΔG_{55-57}	chrominance frequency response	V_{s55} = 400 mV (p-p); 5 MHz/100 kHz	–1.0	–	+0.5	dB
V_{STL}	artificial sync tip level offset voltage		–30	0	+40	mV
V_{GL}	artificial grey level offset voltage		0.85	1.0	1.15	V
α_{MU}	suppression at mute		40	–	–	dB
α_{ASP}	suppression of artificial sync pulse	REC mode	50	–	–	dB
α_{do}	drop-out switch crosstalk	V_{68} = 400 mV (p-p); f_{68} = 1 MHz	–	–	–40	dB
t_{8-57}	drop-out switch delay on	f_8 = 4 MHz	–	0.45	1.0	µs
	drop-out switch delay off		3.0	4.0	5.0	µs
ΔV_{57}	drop-out switch DC offset		–25	0	+25	mV
ΔG	EE frequency response	5 MHz referenced to 100 kHz; $V_I = V_{60}$	–1.0	–	0	dB
NOISE CANCELLER (PLAYBACK MODE)						
$NC1_1$	response $NC1_1$	–30 dB; 1 MHz; NORM; note 2	–10	–8	–6	dB
$NC1_2$	response $NC1_2$	–30 dB; 2 MHz; NORM; note 2	–21	–15	–11	dB
$NC1_3$	response $NC1_3$	0 dB; 2 MHz; NORM; note 2	–1.5	–0.5	+0.5	dB
$NC1_{ED}$	response $NC1_{ED}$	–30 dB; 2 MHz; EDIT; note 2	–5.5	–4.0	–2.5	dB
$NC2_1$	response $NC2_1$	–30 dB; 1 MHz; NORM; note 3	–1.0	–0.5	+0.2	dB
$NC2_2$	response $NC2_2$	–30 dB; 2 MHz; NORM; note 3	–4.0	–2.5	–1.0	dB
$NC2_3$	response $NC2_3$	–30 dB; 3 MHz; NORM; note 3	–8.8	–6.8	–4.8	dB
$NC2_4$	response $NC2_4$	0 dB; 3 MHz; NORM; note 3	–1.25	–0.5	+0.25	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EDIT NOISE CANCELLER (PLAYBACK MODE)						
ED_1	depth 1	–30 dB recursive; note 4	–8.5	–7.0	–6.0	dB
ED_2	depth 2	–20 dB recursive; note 4	–5.2	–4.2	–3.2	dB
ED_3	depth 3	0 dB recursive; note 4	–1.0	–0.2	0	dB
VERTICAL NOISE CANCELLER						
VNC_1	depth 1	–30 dB recursive; note 4	–10.2	–8.7	–7.7	dB
VNC_2	depth 2	–20 dB recursive; note 4	–9.2	–8.2	–7.2	dB
VNC_3	depth 3	0 dB recursive; note 4	–1.8	–0.4	0	dB
L1	limiter output level 1	V_{72} = 857 mV (p-p); f = 100 kHz; note 5	40	60	80	mV
L2	limiter output level 2	V_{72} = 285 mV (p-p); f = 100 kHz; note 5	40	60	80	mV
L3	limiter output level 3	V_{72} = 85 mV (p-p); f = 100 kHz; note 5	90	120	150	mV
L4	limiter output level 4	V_{72} = 285 mV (p-p); f = 1 MHz; note 5	150	200	250	mV
G_{AGC}	control characteristic of AGC	V_{s60} = 2.0 V (p-p)/ 0.5 V (p-p)	0	0.5	1.0	dB
COL_{AGC}	peak/keyed change-over level of AGC (black-to-white = 100%)	V_{s68} = 400 mV (p-p)	107	112	117	%
P_{AGC}	peak AGC characteristic [window signal → 2 µs white over 20 lines, 100% = 2.05 V (p-p)]	video/sync = 5.0	110	–	130	%
S/N	S/N (RMS value related to black/white amplitude)	100 kHz to 5 MHz; EE mode	60	–	–	dB
α_{cr}	FM carrier crosstalk suppression	0 dB = 2.05 V (p-p); f_{FM} = 5 MHz	60	–	–	dB
t_A	attack time of AGC	V_{s60}: 0.5 V (p-p) → 1.0 V (p-p)	–	–	0.1	s
t_R	recovery time of AGC	V_{s60}: 2.0 V (p-p) → 1.0 V (p-p)	–	–	0.5	s
VHS_{cg}	VHS standard (signal amplitude in case of copy guard)	100% = 2.05 V (p-p)	35	–	48	%
Artificial sync control (pin 58)						
V_{58}	DC voltage level	pin open-circuit	–	0.5	1.0	V
V_{thr}	voltage range of through mode		0	–	1.25	V
V_{arts}	voltage range of artificial H SYNC mode (inserts grey level and artificial H SYNC)		1.75	–	3.0	V
V_{artV}	voltage range of artificial V SYNC mode (inserts sync level)		3.5	–	5.0	V
Sub clamp detector (pin 59; open base and collector)						
V_{59}	detecting voltage		1.75	–	2.75	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video input (pin 60)						
V_{60}	DC voltage level		2.35	2.75	3.15	V
$V_{s60(p-p)}$	input voltage level (CVBS signal) (peak-to-peak value)		0.3	1.0	2.0	V
AGC detector (pin 61)						
V_{61}	detecting voltage level	V_{s60} = 1 V (p-p)	1.8	–	2.6	V
EE adjust control (pin 62; open base)						
V_{ctrl}	active range of control	V_{s57} = 2.05 V (p-p); V_{s60} = 1 V (p-p)	2.0	2.5	3.0	V
Simple SVHS mode control (pin 63)						
V_{63}	DC voltage level	pin open-circuit	–	–	0.5	V
V_{VHS}	normal VHS mode		0	–	2.0	V
V_{SVHS}	simple SVHS mode		2.5	–	5.0	V
Sync separator output (pin 64; push/pull output)						
V_{OH}	HIGH level output voltage	R_L = 2 kΩ to GND	4.5	–	–	V
V_{OL}	LOW level output voltage	R_L = 10 kΩ to V_{CC}	–	–	0.3	V
SEN	input sensitivity	slicing level for SYNC level = 100% at pin 68 = 120 mV	26	33	40	%
t_{68-64}	front edge delay		600	750	900	ns
Sync separator detector (pin 65)						
V_{65}	detecting voltage level		2.3	–	3.3	V
EDIT control (pin 66)						
V_{66}	DC voltage level	pin open-circuit	–	–	0.5	V
V_{YNRO}	voltage range of YNR ON mode		0	–	1.25	V
V_{YNRF}	voltage range of YNR OFF mode		1.75	–	3.0	V
V_{EDIT}	voltage range of EDIT mode		3.5	–	5.0	V
Y-LPF output (pin 67)						
V_{SYT}	output sync tip level		1.0	1.3	1.6	V
$V_{67(p-p)}$	output signal (peak-to-peak value)	EE and VV mode; V_{57} = 2.05 V	350	400	450	mV
NL DE-EMPHASIS (VV MODE); note 6						
S1	response S1	–20 dB; 500 kHz; SP	–2.9	–1.9	–0.9	dB
S2	response S2	–20 dB; 2 MHz; SP	–7.3	–5.8	–4.5	dB
L1	response L1	–20 dB; 500 kHz; LP	–5.8	–4.3	–3.0	dB
L2	response L2	–20 dB; 2 MHz; LP	–10.3	–8.8	–7.3	dB
L3	response L3	0 dB; 2 MHz; LP	–4.5	–3.2	–2.0	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clamp 1 input (pin 68; open base for clamp off)						
$V_{s68(p-p)}$	input signal (peak-to-peak value)		–	400	–	mV
V_{CLON}	DC voltage level, when clamp is on (no signal)		2.0	2.1	2.2	V
Clamp 2 input (pin 69; open base for clamp off)						
$V_{s69(p-p)}$	input signal (peak-to-peak value)		–	400	–	mV
V_{CLON}	DC voltage level, when clamp is on (no signal)		2.0	2.1	2.2	V
To CCD drive (pin 70)						
V_{SYT}	output sync tip level		0.9	1.4	1.9	V
$V_{70(p-p)}$	output signal (peak-to-peak value)		350	400	450	mV
Delta Y output (pin 71)						
$V_{s71(p-p)}$	output signal (peak-to-peak value)	V_{s68} = 400 mV (p-p); 100 kHz; pin 69 capacitively to GND;				
		EDNC mode	4.8	6.3	7.8	dB
		VNC mode	2.7	4.2	5.7	dB
V_{71}	DC voltage level		1.4	2.1	2.8	V
Correlation input (pin 72)						
V_{72}	DC voltage level		2.0	2.45	3.0	V
L_{COR}	threshold level of correlation 1 (for chrominance non correlation switch, related to maximum output level at pin 71)		4	5	6	%
NC1 LPF (pin 74)						
V_{74}	DC voltage level		1.1	1.3	1.5	V
NC2 LPF (pin 75)						
V_{75}	DC voltage level		1.1	1.3	1.5	V
Picture control (pin 76)						
V_{76}	DC voltage level	pin open-circuit	2.3	2.5	2.7	V
V_{SHA}	DC range of ‘picture sharp’		0	–	2.3	V
V_{SOF}	DC range of ‘picture soft’		2.7	–	5.0	V
R1	response 1	V_{s76} = 0 V; 0.5 MHz; note 7	0	0.5	1.0	dB
R2	response 2	V_{s76} = 0 V; 2 MHz; note 7	3.0	4.5	6.0	dB
R3	response 3	V_{s76} = 5 V; 0.5 MHz; note 7	–2.0	–1.0	–0.5	dB
R4	response 4	V_{s76} = 5 V; 2 MHz; note 7	–6.7	–5.2	–3.7	dB
R5	response 5	V_{s76} = 2.5 V; 2 MHz; note 7	–0.3	+0.2	+0.7	dB
t_{DL}	delay time (pin 57 to pin 68)	V_{s76} = 2.5 V; 0.1 MHz	185	210	235	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
NLE output (REC)/MDE output (PB) (pin 77)						
V_{SYT}	sync tip DC voltage level	REC	1.6	1.9	2.2	V
		PB; V_7 = 1.7 V	1.2	1.6	2.0	V
$V_{s77R(p-p)}$	output signal (peak-to-peak value)	REC	–	400	–	mV
$V_{s77P(p-p)}$		PB	–	300	–	mV
REC: NON-LINEAR EMPHASIS (NLE)/DETAIL ENHANCER (DTE); note 8						
R_{D1}	response D1	–20 dB; 500 kHz; SP; NORM	1.7	2.7	3.7	dB
R_{D2}	response D2	–20 dB; 2 MHz; SP; NORM	4.25	5.75	7.25	dB
R_{S1}	response S1	–20 dB; 500 kHz; SP; EDIT	1.0	1.7	2.4	dB
R_{S2}	response S2	–20 dB; 2 MHz; SP; EDIT	3.0	4.0	5.0	dB
R_{L1}	response L1	–20 dB; 500 kHz; LP	3.1	4.4	5.7	dB
R_{L2}	response L2	–20 dB; 2 MHz; LP	5.5	7.5	9.5	dB
R_{L3}	response L3	0 dB; 2 MHz; LP	0.9	1.6	2.3	dB
REC: VERTICAL EMPHASIS; note 9						
P_{L1}	peak level 1	–30 dB recursive	3.0	4.0	5.0	dB
P_{L2}	peak level 2	–20 dB recursive	2.5	3.0	3.5	dB
P_{L3}	peak level 3	0 dB recursive	0	0.2	1.0	dB
ΔG_{77}	white level expansion	V_{68} = 100 mV (p-p); f_{68} = 10 kHz; V_{68DC} = 2.0/2.4 V	0	3	5	%
Clamp 3 input (pin 78; open base for clamp off)						
$V_{s78R(p-p)}$	input signal (peak-to-peak value)	REC	–	400	–	mV
$V_{s78P(p-p)}$	input signal (peak-to-peak value)	PB	–	300	–	mV
V_{78CO}	DC voltage level when clamp is on		1.3	1.5	1.7	V
Negative feedback input of main emphasis (pin 79; open base)						
Main emphasis output (pin 80)						
V_{SYT}	DC voltage level (sync tip)	feedback closed	1.9	2.1	2.3	V
$V_{s80(p-p)}$	output signal (peak-to-peak value)	V_{s57} = 2.05 V (p-p); V_{60} = 1 V (p-p)	350	400	450	mV
DCL	dark clip level	$V_I = V_{s78}$ = 400 mV (p-p)	45	55	65	%
WCL	white clip level	$V_I = V_{s78}$ = 400 mV (p-p); V_2 = 2.35 V	150	190	230	%
G_{78-80}	flat amplifier gain	f = 100 kHz; note 10	12	14	16	dB
ΔG_{78-80}	flat amplifier frequency characteristics	f = 3 MHz/100 kHz; note 10	–1	–	+0.5	dB
ΔV_{80}	DC offset voltage between rotary HIGH and LOW		2.8	3.2	3.6	mV

Notes to the characteristics

1. The blanking of BGP starts at first equalizing pulse and stops 24 lines after rotary transition.
2. All values referenced to 100 kHz and V_{76} = 2.5 V.
   Input: 0 dB = V_{68} = 400 mV (p-p).
   Output: 0 dB = V_{57} at 100 kHz and given input level.
   Pin 74: R = 2.2 kΩ; C = 68 pF. Pin 75: C = 22 μF.
3. All values referenced to 100 kHz and V_{76} = 2.5 V.
   Input: 0 dB = V_{68} = 400 mV (p-p).
   Output: 0 dB = V_{57} at 100 kHz and given input level.
   Pin 74: C = 22 μF. Pin 75: R = 1.2 kΩ; C = 3.3 nF.
4. V_{76} = 2.5 V.
   Input: 0 dB = V_{68} = 400 mV (p-p).
   Output: 0 dB = V_{57} at 1, 2, 3,... × f_H and given input level.
5. All measurements with sinusoidal input signal; output signal at pin 57 measured between $\frac{\pi}{4}$ and $\frac{3\pi}{4}$.
6. All values referenced to 10 kHz.
   Input: 0 dB = V_{78} = 300 mV (p-p).
   Output: 0 dB = V_{67} at 10 kHz and given input level.
7. All values referenced to 100 kHz.
   Input: V_{s68} = 40 mV (p-p) (–20 dB).
   Output: 0 dB = V_{57} at 100 kHz and given input level.
8. All values referenced to 10 kHz.
   Input: 0 dB = V_{s68} = 400 mV (p-p).
   Output: 0 dB = V_{77} at 10 kHz and given input level.
9. Input: 0 dB = V_{s68} = 400 mV (p-p).
   Output: 0 dB = V_{77} at 1, 2, 3,... × f_H and given input level.
10. Input: V_{78} = 75 mV (p-p). R (pin 78/80) = 1 kΩ. R/C (pin 79) = 220 Ω/0.1 μF.

CHROMINANCE FILTER CHARACTERISTICS

Table 1 Low-pass filter 630 kHz; frequency response pin 46 to pin 34

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL/EE						
ΔG1	frequency response 1	G(1 MHz)/G(0.2 MHz)	–4	–3	–2	dB
ΔG2	frequency response 2	G(1.5 MHz)/G(0.2 MHz)	–9	–7	–5	dB
ΔG3	frequency response 3	G(2 MHz)/G(0.2 MHz)	–10	–14	–18	dB
ΔG4	frequency response 4	G(3 MHz)/G(0.2 MHz)	–	–	–25	dB
ΔG5	frequency response 5	G(4.43 MHz)/G(0.2 MHz)	–	–	–40	dB
ΔG7	frequency response 7	G(9.5 MHz)/G(0.2 MHz)	–	–	–35	dB
t_d	group delay 1	f_i = 0.2 MHz	245	285	325	ns
SECAM/EE						
ΔG2	frequency response 2	G(1.5 MHz)/G(0.2 MHz)	–5	–3	–1	dB

Table 2 Band-pass filter 4.43 MHz at EE mode; frequency response pin 60 to pin 39

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL/EE						
ΔG1	frequency response 1	G(<2.7 MHz)/G(4.43 MHz)	–	–	–22	dB
ΔG2	frequency response 2	G(2.7 MHz)/G(4.43 MHz)	–	–	–30	dB
ΔG3	frequency response 3	G(3.93 MHz)/G(4.43 MHz)	–2	–1	0	dB
ΔG4	frequency response 4	G(4.93 MHz)/G(4.43 MHz)	–3	–2	–1	dB
ΔG6	frequency response 5	G(6.2 MHz)/G(4.43 MHz)	–	–	–30	dB
ΔG7	frequency response 6	G(>6.2 MHz)/G(4.43 MHz)	–	–	–15	dB
t_d	group delay 1	f_i = 4.43 MHz	380	420	460	ns
SECAM/EE						
ΔG7	frequency response 6	G(6.0 MHz)/G(4.43 MHz)	–	–	–30	dB

Table 3 Band-pass filter 4.43 MHz at VV mode; frequency response pin 46 to pin 48

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL/VV						
ΔG1	frequency response 1	G(<2.7 MHz)/G(4.43 MHz)	–	–	–20	dB
ΔG2	frequency response 2	G(2.9 MHz)/G(4.43 MHz)	–	–	–30	dB
ΔG3	frequency response 3	G(3.9 MHz)/G(4.43 MHz)	–3	–2	–1	dB
ΔG4	frequency response 4	G(4.93 MHz)/G(4.43 MHz)	–3.5	–2.5	–1.5	dB
ΔG5	frequency response 5	G(5.7 MHz)/G(4.43 MHz)	–	–21	–15	dB
ΔG6	frequency response 6	G(6 MHz)/G(4.43 MHz)	–	–	–30	dB
ΔG7	frequency response 7	G(>6 MHz)/G(4.43 MHz)	–	–26	–15	dB
t_d	group delay 1	f_i = 4.43 MHz	420	460	500	ns
SECAM/VV						
ΔG2	frequency response 2	G(2.7 MHz)/G(4.43 MHz)	–	–	–30	dB

Table 4 Band-pass filter 630 kHz; frequency response pin 41 to pin 39

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VV						
ΔG1	frequency response 1	G(<100 Hz)/G(630 kHz)	–	–	–20	dB
ΔG2	frequency response 2	G(100 kHz)/G(630 kHz)	–7	–5	–3	dB
ΔG3	frequency response 3	G(930 kHz)/G(630 kHz)	–3	–2	–1	dB
ΔG4	frequency response 4	G(1.5 MHz)/G(630 kHz)	–	–15	–10	dB
ΔG5	frequency response 5	G(2.3 MHz)/G(630 kHz)	–	–	–40	dB
ΔG6	frequency response 6	G(>2.4 MHz)/G(630 kHz)	–	–	–35	dB
t_d	group delay 1	f_i = 630 kHz	710	750	790	ns
Δt_d	delta group delay	SVHS/VHS	–200	–160	–120	ns

LUMINANCE FILTER CHARACTERISTICS

Table 5 Luminance main low-pass filter; frequency response pin 60 to pin 67

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EE						
ΔG1	frequency response 1	G(2 MHz)/G(0.2 MHz)	–2.5	–1.0	0	dB
ΔG2	frequency response 2	G(3 MHz)/G(0.2 MHz)	–4.5	–3.0	–1.5	dB
ΔG3	frequency response 3	G(4.43 MHz)/G(0.2 MHz)	–	–40	–30	dB
t_d	group delay 1	f_i = 0.2 MHz	660	700	740	ns

Table 6 Demodulator low-pass filter; frequency response from demodulator output to pin 4

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VV						
ΔG1	frequency response 1	G(3 MHz)/G(0.2 MHz)	–4.5	–	0	dB
ΔG2	frequency response 2	G(6 MHz)/G(0.2 MHz)	–	–25	–15	dB

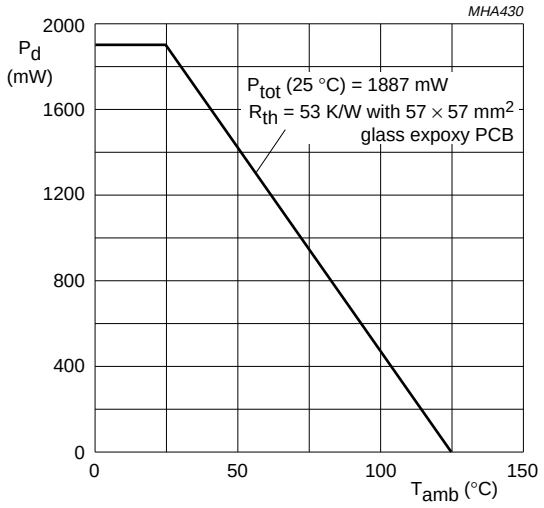


Fig.3 Power dissipation as a function of ambient temperature.

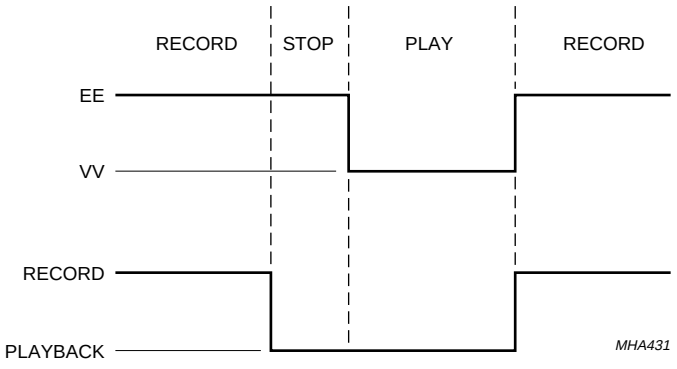


Fig.4 VCR/IC modes.

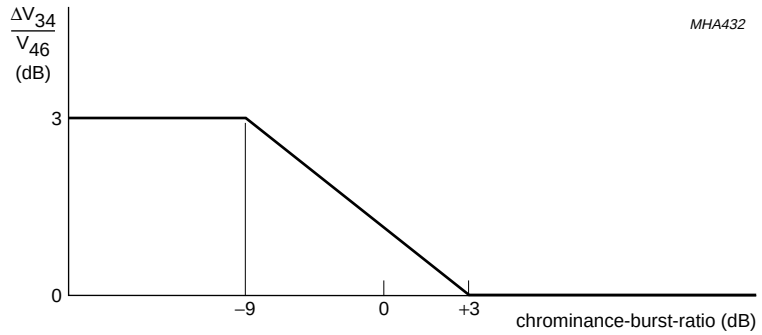
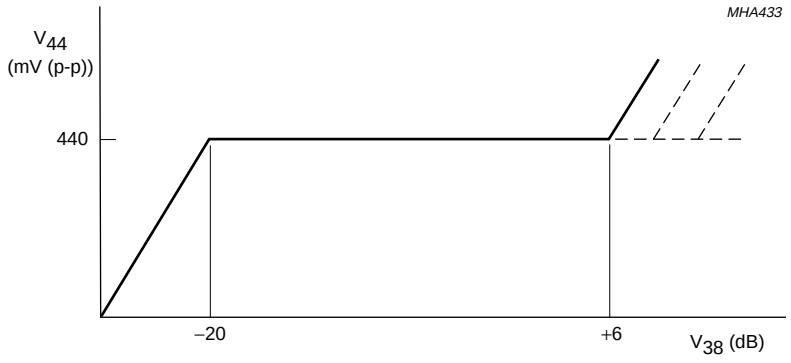


Fig.5 CACC control characteristics.



0 dB is equivalent to 110 mV (p-p) at pin 38.

Fig.6 ACC characteristics.

Table 7 Sensitivity of PB APC (multiplication factor for phase detector sensitivity)

PROGRAM	PAL		NTSC		
	SP	LP	SP	LP	EP
NORM	2	1	4	2	2
TRICK	2	1	2	2	2

Table 8 CACC logic

SYSTEM		CACC
NTSC	SP	ON
	LP	OFF
	EP	ON
PAL	SP	ON
	LP	OFF
SECAM	SP	OFF
	LP	

Table 9 1.5 dB up gain logic

SYSTEM		1.5 dB up
NTSC	SP	OFF
	LP	ON
	EP	
PAL	SP	OFF
	LP	ON
SECAM	SP	ON
	LP	

Table 10 CNR logic (NCorr: non correlation of luminance signal)

SYSTEM		CNR
NTSC	NORM	OFF
	EDIT	
	pin 42 to V_{CC}	
	NCorr	
PAL	NORM	ON
	EDIT	OFF
	pin 42 to V_{CC}	
	NCorr	
SECAM	NORM	OFF
	EDIT	
	pin 42 to V_{CC}	
	NCorr	

Table 11 Burst down logic

MODE	SYSTEM		BURST DOWN
EE	any mode		OFF
VV	NTSC	SP	ON (–5.0 dB)
		LP	OFF
		EP	ON (–4.0 dB)
	PAL		OFF
	SECAM		OFF

OPERATION MODE

Table 12 Operation mode (Y-block; PART 1)

FILTER	MODE	CONDITIONS	SP	LP
Filter	Y MAIN LPF		$f_c \approx 3$ MHz; 4.43 MHz Trap	
	Y SUB LPF (demodulation output)		$f_c \approx 3$ MHz	
YNR	REC	EDIT; pin 66 HIGH	OFF	
		YNR OFF; pin 66 medium	OFF	
		YNR ON; pin 66 LOW	OFF	vertical emphasis
	PB	EDIT; pin 66 HIGH	OFF	EDNC
		YNR OFF; pin 66 medium	OFF	
		YNR ON; pin 66 LOW	EDNC	VNC
NLE NLDE	REC	EDIT; pin 66 HIGH	NLE(C)	NLE(D)
		YNR OFF; pin 66 medium	NLE(C) + DTE	
		YNR ON; pin 66 LOW		
	PB		NLDE(C)	NLDE(D)
FM carrier interleave			ON	

Table 13 Operation mode (Y-block; PART 2)

FUNCTION	CONDITIONS		OPERATION
main clamp pin 68	REC		ON
	PB	NORM	
		drop-out; note 1	OFF
emergency clamp	REC		ON
	PB	NORM	
		TRICK; pin 11 LOW	OFF
noise canceller	REC		OFF
	PB	EDIT; pin 66 HIGH	ON (−6 dB)
		YNR ON; pin 66 LOW	ON
		YNR OFF; pin 66 medium	
picture control	REC		OFF
	PB	EDIT; pin 66 HIGH	
		YNR ON; pin 66 LOW	ON
		YNR OFF; pin 66 medium	
artificial H/V switch	REC		through
	PB	VIDEO; pin 58 LOW	
		GREY; pin 58 medium	grey level (30%)
		SYNC; pin 58 HIGH	sync tip level
search noise clip	REC		OFF
	PB	NORM	
		TRICK; pin 11 LOW	ON
SVHS PB	PB	VHS; pin 63 LOW	VHS
		SQPB; pin 63 medium/HIGH	SVHS

Note

1. Same timing as DOC SW.

INTERNAL CIRCUITRY

Table 14 Internal circuitry of Figs 1 and 2

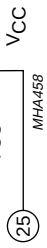
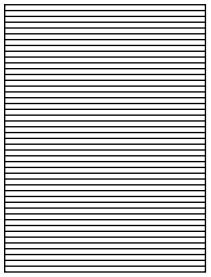
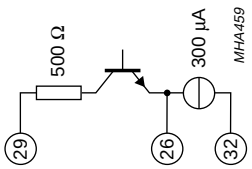
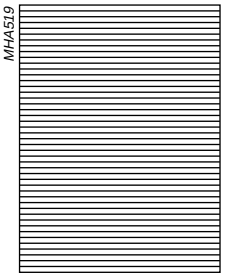
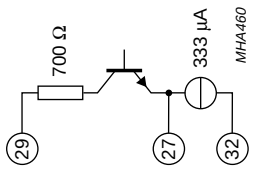
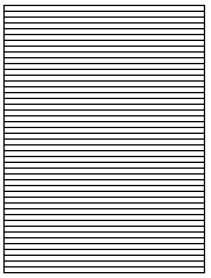
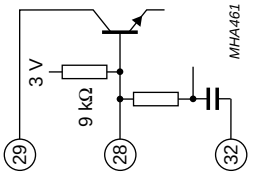
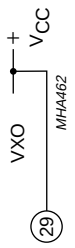
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
1	modulator input		2.1 V		V_T/I_E	
2	white clip control		2.35 V		open base	
3	main de-emphasis output	3.0 (sync)			open collector	
4	main de-emphasis and peaking	2.0 (sync)			V_T/I_E	
5	supply voltage modulator	5.0				

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
6	FM output	3.3			V_T/I_E + 100 Ω	
7	demodulator gain control	1.7 (typ)			open base	
8	PB FM input	3.0			10 kΩ	
9	envelope detector		(4.7 V)	(3.7 V) 2.3 V (no signal)	30 kΩ	
10	drop-out pulse output		4.15 V		15 kΩ	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
11	switch (EE/VV/TRICK)		3.5 to 5 V	0 to 1.25 V (TRICK) 1.75 to 3 V (VV)	50 kΩ	
12	switch (SP/LP/EP)		0 to 1.25 V (SP) 1.75 to 3 V (LP) 3.5 to 5 V (EP)		open base	
13	colour killer pin		1.8 V without chrominance signal colour on >2.2 V colour off <2.0 V			
14	skew output		HIGH (4.95 V) or LOW (0.2 V)		25 kΩ	
15	frequency correction output	(2.1)	current ±17 µA if active			

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
16	switch (REC/PB/ID)		0 to 1.25 V	1.75 to 3 V (PB) 3.5 to 5 V (ID)	50 kΩ	
17	sandcastle, BGP output (LOW active)					
18	rotary pulse		channel 1: 3 to 5 V channel 2: 0 to 2 V		open base	
19	switch (C/BW/NORM)		0 to 1.25 V (NORM) 1.75 to 3 V (BW) 3.5 to 5 V (C)		open base	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
20	mute detector		4.8 V at coincidence 0 V at no coincidence V_{th} = 2.5 V			
21	loop filter (EE) VXO	2.4				
22	ground VCO	0				
23	loop filter VCO	2.1				
24	VCO bias current	0.65				

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM EE	WAVEFORM VV	Z	INTERNAL CIRCUIT
25	supply voltage VCO	5.0				
26	f_{SC} output	2.3			V_T/I_E	
27	VXO (crystal output)				V_T/I_E	
28	VXO (crystal input)	3.0			9 kΩ	
29	supply voltage VXO	5.0				

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
30	filter reference terminal (chrominance filter)	3.0				
31	$2f_{SC}$ output	5.0	60 mV (p-p) with R_L = 1 kΩ		open collector	
32	ground VXO	0				
33	loop filter CACC	(2.5)				
34	CACC output	2.5		2.5 V colour on 0 V colour off	V_T/I_E	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM EE	WAVEFORM VV	Z	INTERNAL CIRCUIT
35	ACC loop filter switch (channel 2)		non conductive during channel 1 or TRICK		open collector	
36	ACC loop filter	(3.4)				
37	ACC loop filter switch (channel 1)	0.3	non conductive during channel 2 or TRICK		open collector	
38	ACC input	1.6			10 kΩ	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
39	BPF switch output				V_T/I_E	
40	supply voltage chrominance part	5.0				
41	PB chrominance from tape	2.2			10 kΩ	
42	CNR test pin	3.0				
43	ground chrominance part	0				

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
44	test pin 2	2.25	MHA570 440 mV (p–p)	MHA571 440 mV (p–p)		MHA477 + 1 kΩ 2.7 kΩ 2.7 kΩ 400 µA 44 45
45	mixer balance	2.25				MHA478 + 1 kΩ 2.7 kΩ 2.7 kΩ 400 µA 44 45
46	test pin 1	2.2	MHA523 110 mV (p–p) lower sideband (selectively measured)			MHA479 + 50 µA 46

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM EE	WAVEFORM VV	Z	INTERNAL CIRCUIT
47	AC coupling	2.2				
48	output comb driver (VV)	2.5			V_T/I_E	
49	through side chrominance input	2.7			10 kΩ	
50	comb side chrominance input	2.7			10 kΩ	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
51	CNR limiter input	0.77				
52	switch (PAL/ SECAM / NTSC)		0 to 1.25 V (NTSC) 1.75 to 3 V (PAL) 3.5 to 5 V (SECAM)		50 kΩ	
53	chrominance output	3.0			V_T/I_E	
54	filter reference terminal (luminance filter)	2.5			open base and open collector	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM EE	WAVEFORM VV	Z	INTERNAL CIRCUIT
55	PB chrominance input		0 V HIGH: no reaction on copy guard LOW: AGC reacts on copy guard V_{th} = 3.0 V		20 kΩ	
56	supply voltage luminance part	5.0				
57	video output	1.1 sync			V_T/I_E	
58	artificial sync control			0 to 1.25 V (VIDEO) 1.75 to 3 V (GREY + H_{sync}) 3.5 to 5 V (SYNC)	50 kΩ	
59	sub clamp detector	2.3				

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
60	video input			3.0 V	35 kΩ	
61	AGC detector		2.2 V	1.85 V	V_T/I_E + 450 Ω	
62	EE adjust control	2.5 (typ)			open base	
63	simple SVHS mode control			0 to 2 V (VHS) 2.5 to 5 V (SVHS)	50 kΩ	

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
64	sync separator output		HIGH: 5 V LOW: 0 V MHA526			
65	sync separator detector	2.8			V_T/I_E + 500 Ω	
66	EDIT control		0 to 1.25 V (YNR ON) 1.75 to 3 V (YNR OFF) 3.5 to 5 V (EDIT)		50 kΩ	
67	Y-LPF output				V_T/I_E	

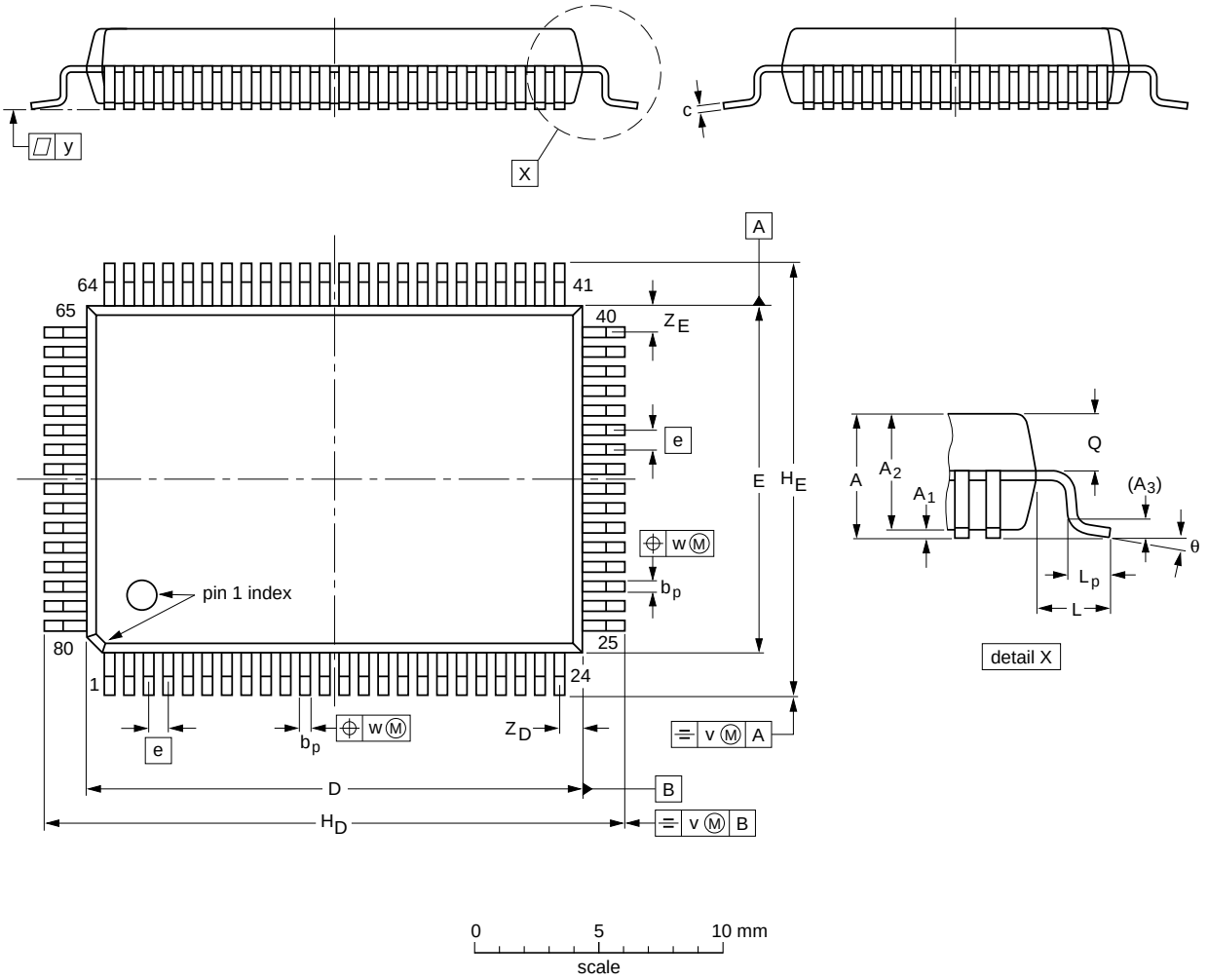
PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM EE	WAVEFORM VV	Z	INTERNAL CIRCUIT
68	clamp 1 input	2.1 (sync)	400 mV sync/white MHA582			2 kΩ 68 MHA501
69	clamp 2 input	2.1 (sync)	400 mV sync/white MHA582			2 kΩ 69 MHA502
70	to CCD drive	1.4 (sync)	400 mV sync/white MHA582		V_T/I_E	+ 500 Ω 5 kΩ 70 227 µA MHA503
71	delta Y output	2.1	noise MHA528		V_T/I_E	+ 200 Ω 71 455 µA MHA504

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM EE	WAVEFORM VV	Z	INTERNAL CIRCUIT
72	correlation input	2.45	noise MHA528		10 kΩ	2.5 V, 10 kΩ, 119 µA, MHA505, 72
73	ground luminance part	0				luminance, GND, MHA506, 73
74	NC1 LPF		0 V	noise 1.3 V MHA541	2 kΩ	2 kΩ, MHA507, 74
75	NC2 LPF		0 V	noise 1.3 V MHA541	2 kΩ	2 kΩ, MHA508, 75
76	picture control	2.5				100 kΩ, 100 kΩ, 25 kΩ, MHA509, 76

PIN NO.	PIN NAME (DESCRIPTION)	DC (V)	WAVEFORM		Z	INTERNAL CIRCUIT
			EE	VV		
77	NLE output (REC)/MDE output (PB)				V_T/I_E	
78	clamp 3 input	1.5 (sync)				
79	negative feedback input of main emphasis	2.1 (sync)			open base	
80	main emphasis output	2.1 (sync)			V_T/I_E	

PACKAGE OUTLINE

QFP80: plastic quad flat package; 80 leads (lead length 1.6 mm); body 14 x 20 x 3.0 mm **SOT310-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.4	0.2 0	3.2 2.8	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	23.6 22.8	17.6 16.8	1.6	1.1 0.5	1.55 1.25	0.3	0.15	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT310-1						~~92-06-30~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.