SGS-THOMSON MICROELECTRONICS

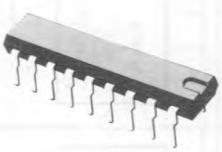
TDA7325

PLL RADIO TUNING SYNTHESIZER

ADVANCE DATA

- ON-CHIP PRESCALER WITH UP TO 150 MHz INPUT FREQUENCY.
- ON-CHIP AM AND FM INPUT AMPLIFIERS WITH HIGH SENSITIVITY (30 mV).
- LOW CURRENT DRAIN (TIPICALLY 20 mA FOR AM AND 25 mA FOR (FM) OVER A WIDE SUPPLY VOLTAGE RANGE (4V TO 10V).
- ON-CHIP AMPLIFIER FOR LOOP FILTER FOR BOTH AM AND FM (UP TO 25V TUNING VOLTAGE).
- ON-CHIP/PROGRAMMABLE CURRENT AMPLIFIER (CHARGE PUMP) TO ADJUST THE LOOP GAIN
- ONLY ONE REFERENCE FREQUENCY FOR BOTH AM AND FM
- HIGH SIGNAL PURITY DUE TO A SAMPLE AND HOLD PHASE DETECTOR FOR THE IN-LOCK CONDITION.
- HIGH TUNING SPEED DUE TO A POWERFUL DIGITAL MEMORY PHASE DETECTOR DURING THE OUT-LOCK CONDITION
- TUNING STEPS FOR AM ARE: 1kHz OR 1.25 kHz FOR A VCO FREQUENCY RANGE OF 512 kHz TO 32 MHz
- TUNING STEPS FOR FM ARE: 10 kHz OR 12.5 kHz FOR A VCO FREQUENCY RANGE OF 150MHz TO 80MHz
- SERIAL 3-LINE BUS INTERFACE TO A MICROCOMPUTER
- TEST OUTPUT PIN

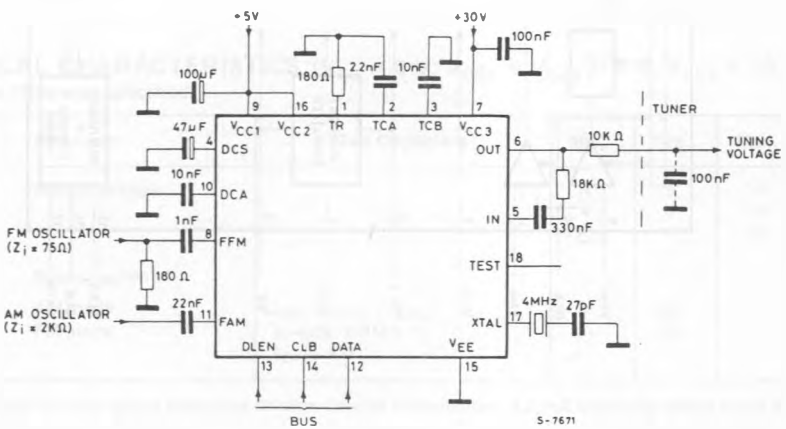
The TDA 7325 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.



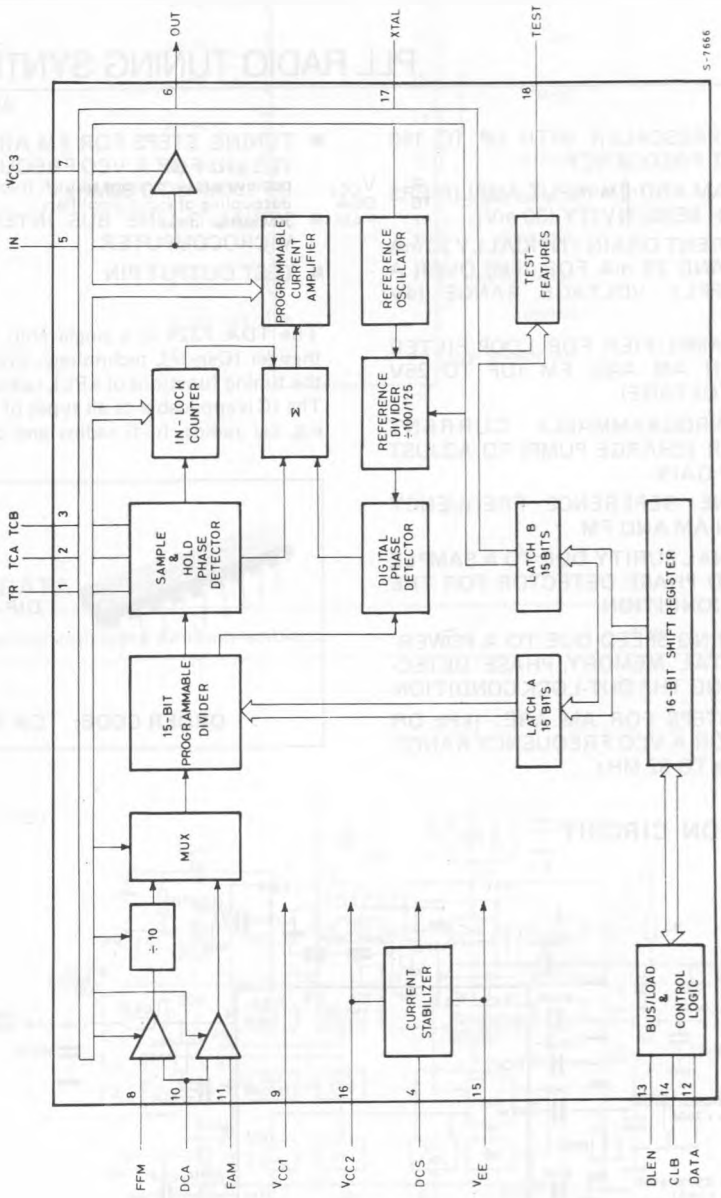
DIP-18 Plastic

ORDER CODE: TDA 7325

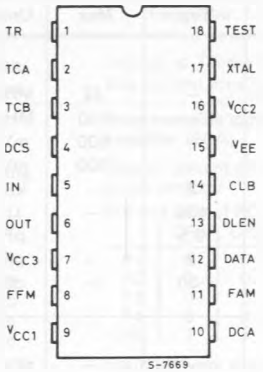
APPLICATION CIRCUIT



BLOCK DIAGRAM



CONNECTION DIAGRAM



PINNING

1	TR	resistor/capacitors
2	TCA	for sample and
3	TCB	hold circuit
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	
13	DLEN	BUS
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

ABSOLUTE MAXIMUM RATINGS

V_{CC1}; V_{CC2}	Supply voltage; logic and analogue part	-0.3 to 13.2	V
V_{CC3}	Supply voltage; output amplifier	V_{CC2} to +30	V
P_{tot}	Total power dissipation	max. 800	mW
T_{amb}	Operating ambient temperature range	-25 to +70	°C
T_{stg}	Storage temperature range	-40 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 20 V; T_{amb} = 25°C; unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{CC1}	Supply voltages		4	5	10	V
V_{CC2}			4	5	10	V
V_{CC3}			V_{CC2}	–	25	V
	Supply currents*					
I_{tot}	AM mode	$I_{tot} = I_{CC1} + I_{CC2}$	–	20	–	mA
I_{tot}	FM mode	in-lock; BRM = '1';	–	25	–	mA
I_{CC3}		I_{OUT} = 0			1	mA

* When the bus is in the active mode (see BRM in Control Information), 4.5 mA should be added to the figures given.

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	RF inputs (FAM, FFM)					
f_{FAM}	AM input frequency		512 kHz	–	32	MHz
f_{FFM}	FM input frequency		80	–	150	MHz
$V_{I(rms)}$	Input voltage at FAM		30	–	500	mV
$V_{I(rms)}$	Input voltage at FFM		30	–	500	mV
R_I	Input resistance at FAM		–	2	–	kΩ
R_I	Input resistance at FFM		–	135	–	Ω
C_I	Input capacitance at FAM		–	3.5	–	pF
C_I	Input capacitance at FFM		–	3	–	pF
V_s/V_{ns}	Voltage ratio allowed between selected and non-selected input		–	-30	–	dB
	Crystal oscillator (XTAL)	see note 1				
f_{XTAL}	Maximum input frequency		4	–	–	MHz
R_s	Crystal series resistance		–	–	150	Ω
	BUS inputs (DLEN, CLUB, DATA)					
V_{IL}	Input voltage LOW		0	–	0.8	V
V_{IH}	Input voltage HIGH		2.4	–	V_{CC1}	V
$-I_{IL}$	Input current LOW	V_{IL} = 0.8 V	–	–	10	μA
I_{IH}	Input current HIGH	V_{IH} = 2.4 V	–	–	10	μA
	BUS inputs timing (DLEN, CLB, DATA)	see also Fig. 2 and note 2				
$t_{CLBlead}$	Lead time for CLB to DLEN		1	–	–	μs
t_{Tlead}	Lead time for DATA to the first CLB pulse		0.5	–	–	μs
$t_{CLBlag1}$	Set-up time for DLEN to CLB		5	–	–	μs
t_{CLBH}	CLB pulse width HIFH		5	–	–	μs
t_{CLBL}	CLB pulse width LOW		5	–	–	μs
$t_{DATAlead}$	Set-up time for DATA to CLB		8	–	–	μs
$t_{DATAhold}$	Hold time for DATA to CLB		0	–	–	μs
$t_{DLENhold}$	Hold time for DLEN to CLB		2	–	–	μs
$t_{CLBlag2}$	Set-up time for DLEN to CLB load pulse		2	–	–	μs
t_{DIST}	Busy time from load pulse to next start to transmission	next transmission after word 'B' to other device	5	–	–	μs
t_{DIST}	Busy time	or	0.3	–	–	ms
	asynchronous mode	next transmission to SAA1057 after word 'A'	1.3	–	–	ms
	Sample and hold circuit (TR, TCA, TCB)	see also notes 3; 4				
V_{TCA}, V_{TCB}	Minimum output voltage		–	1.3	–	V
V_{TCA}, V_{TCB}	Maximum output voltage		–	V_{CC2}-0.7		V
C_{TCA}	Capacitance at TCA	REFH = '1'	–	–	2.2	nF
CTA	(external)	REFH = '0'	–	–	2.7	nF
t_{DIS}	Discharge time at TCA	REFH = '1'	–	5		μs
		REFH = '0'	–	6.25		μs

ELECTRICAL CHARACTERISTICS (continued)

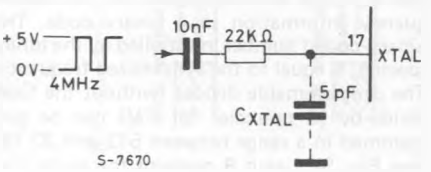
Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{TR}	Voltage at TR during discharge		–	0.7	–	V
I_{bias}	Bias current into TCA, TCB	in-look	–	10		nA
	Programmable current amplifier (PCA)					
$\pm I_{dig}$	Output current of the dig. phase detector		–	0.4	–	mA
	Current gain of PCA (CP3 CP2 CP1 CP0)					
G_{P1}	P1 0 0 0 0	$V_{CC2} \geq 5$ V (only for P1)	–	0.023	–	
G_{P2}	P2 0 0 0 1		–	0.07	–	
G_{P3}	P3 0 0 1 0		–	0.23	–	
G_{P4}	P4 0 1 1 0		–	0.7	–	
G_{P5}	P5 1 1 1 0		–	2.3	–	
	Ratio between the output current of S/H into PCA and the voltage on					
S_{TCB}	C_{TCB}		–	1.0	–	µA/A
ΔV_{TCB}	Offset voltage on TCB	in lock	–	1	–	V
	Output amplifier (IN, OUT)					
V_{IN}	Input voltage	in-lock; equal to internal reference voltage	–	1.3	–	V
V_{OUT}	Output voltages minimum	$-I_{OUT}$ = 1 mA	–	–	0.5	V
V_{OUT}	Output voltages maximum	I_{OUT} = 1 mA	V_{CC3}-2.5V	–	–	V
V_{OUT}	Output voltages maximum	I_{OUT} = 0.1 mA	–	V_{CC3}-1	–	V
$\pm I_{OUT}$	Maximum output current	$V_{OUT} = V_{CC3}$-4V	5	–	–	mA
	Test output (TEST) *					
V_{TL}	Output voltage LOW		–	–	0.5	V
V_{TH}	Output voltage HIGH		–	–	12	V
I_{Toff}	Output current OFF	V_{TH}	–	–	10	µA
I_{Ton}	Output current ON	V_{TL}	150	–	–	µA
	Ripple rejection **					
	at f_{ripple} = 100 Hz					
	$\Delta V_{CC1}/\Delta V_{OUT}$		–	77	–	dB
	$\Delta V_{CC2}/\Delta V_{OUT}$		–	70	–	dB
	$\Delta V_{CC3}/\Delta V_{OUT}$	$V_{OUT} \leq V_{CC3}$-3V	–	60	–	dB

* Open collector output ** Measured in Fig. 6

NOTES

1. Pin 17 (XTAL) can also be used as an input for an external clock.
   The values given in Fig. 1 are a typical application example.
2. See BUS information in section 'operation description .
3. The output voltage at TCB and TCA is typically $\frac{1}{2}V_{CC2}$+0.3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula $\frac{1}{2}V_{CC2}$+0.3 V.
4. Crystal oscillator frequency f_{XTAL} = 4 MHz.

Fig. 1 - Circuit configuration showing external 4 MHz clock



GENERAL DESCRIPTION

The TDA 7325 performs the entire PPL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.
The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signal.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An-in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1.25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1.25 kHz for AM, and 10 kHz and 12.5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the runing system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 25 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B, For data word format and bit position see Fig. 3.

FM FM/AM selection; '1' = FM, '0' = AM

REFH reference frequency selection; '1' = 1.25 kHz, '0' = 1 kHz (sample and hold phase (detector)

CP3
CP2
CP1
CP0 control bits for the programmable current amplifier (see section Electrical Characteristics)

SB2 enables last 8 bits (SLA to T0) of data word B;
'1' enables '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically

SLA load mode of latch A; '1' = synchronous, '0' asynchronous

PDM1
PDM0 phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on

T3 test bit; must be programmed always '0'

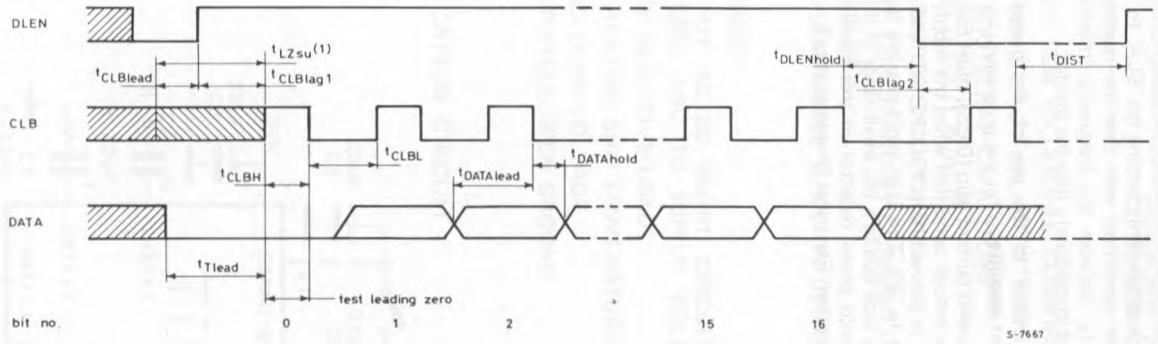
T2 test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin

T1 test bit; must be programmed always '0'

T0 test bit; selects the output of the programmable counter to the TEST pin

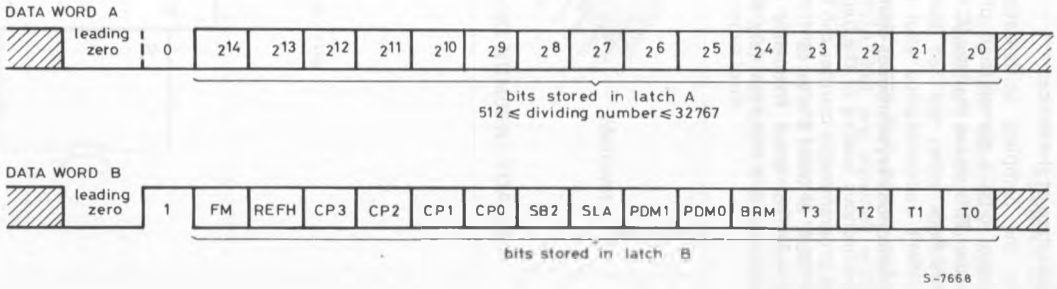
T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output progrrammable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

Fig. 2 – BUS format



(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I²C bus is used for other devices on the same data and clock lines

Fig. 3 – Bit organization of data words A and B



APPLICATION INFORMATION

Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.

For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

Synchronous/asynchronous operation

Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the use of the programmable current amplifier

The lowest current gain (0.023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Electrical Characteristics').