DATA SHEET

TDA4820T
Sync separation circuit for video applications

Preliminary specification
File under Integrated Circuits, IC02

June 1990

Philips
Semiconductors

PHILIPS

Sync separation circuit for video applications TDA4820T

FEATURES

- Fully integrated, few external components
- Positive video input signal, capacitively coupled
- Operates with non-standard video input signals
- Black level clamping
- Generation of composite sync slicing level at 50% of peak sync voltage
- Vertical sync separator with double slope integrator
- Delay time of the vertical output pulse is determined by an external resistor
- Vertical sync generation with a slicing level at 40% of peak sync voltage
- Output stage for composite sync
- Output stage for vertical sync

GENERAL DESCRIPTION

The TDA4820T is a monolithic integrated circuit including a horizontal and a vertical sync separator, offering composite sync and vertical sync extracted from the video signal.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12	13.2	V
I_P	supply current (pin 1)		–	8	12	mA
$V_{2(p-p)}$	input voltage amplitude (peak-to-peak value)		0.2	1	3	V
$V_{sync(p-p)}$	sync pulse input voltage amplitude (pin 2) (peak-to-peak value)		50	300	500	mV
V_o	maximum vertical sync output voltage (pin 6)	I_6 = –1 mA	10.0	–	–	V
V_o	maximum composite sync output voltage (pin 7)	I_7 = –3 mA	10.0	–	–	V
V_o	minimum output voltage (pins 6 and 7)	$I_{6,7}$ = 1 mA	–	–	0.6	V
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4820T	8	mini-pack	plastic	SO8; SOT96A (1)

Note

1. SOT96-1; 1997 January 08.

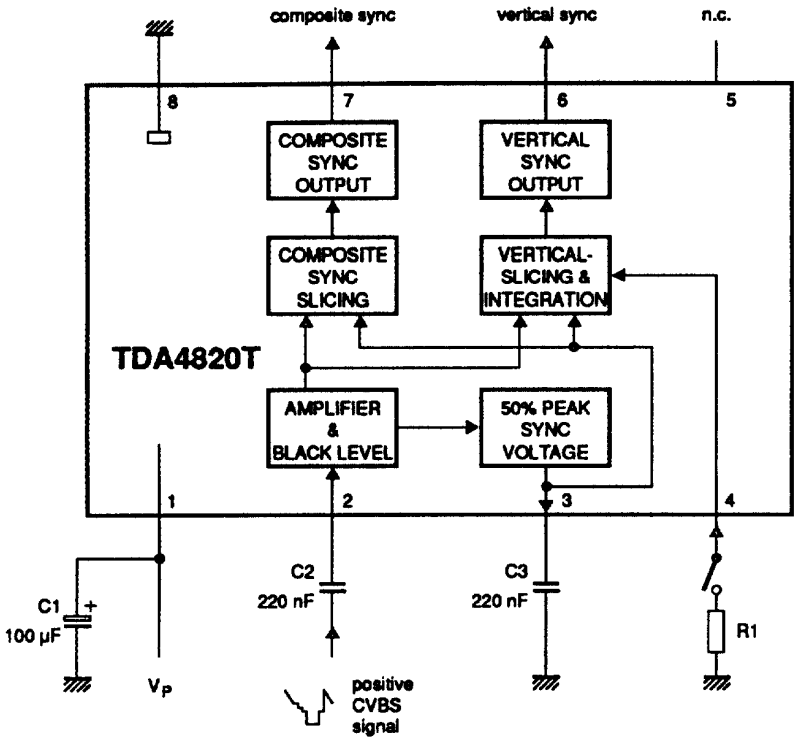


Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
V_{CVBS}	2	video input signal
SLEV	3	slicing level
VDEL	4	vertical integration delay time
n.c.	5	not connected
VSYN	6	vertical sync output signal
CSYN	7	composite sync output signal
GND	8	ground

PIN CONFIGURATION

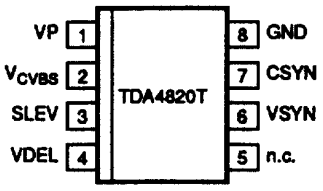


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

- Video amplifier and black level clamping
- 50% peak sync voltage
- Composite sync slicing
- Vertical slicing and double slope integrator
- Vertical sync output
- Composite sync output

Video amplifier and black level clamping (pin 2)

The sync separation circuit TDA4820T is designed for positive video input signals.
The video signal (supplied via capacitor C2 at pin 2) is amplified by approximately 15 in the input amplifier. The black level clamping voltage (approximately 2 V) is stored by capacitor C2.

50% peak sync voltage (pin 3)

From the black level and the peak sync voltage, the 50% value of the peak sync voltage is generated and stored by capacitor C3 at pin 3. A slicing level control circuit ensures a constant 50% value, as long as the sync pulse amplitude at pin 2 is between 50 mV and 500 mV, independent of the amplitude of the picture content.

Composite sync slicing

A comparator in the composite sync slicing stage compares the amplified video signal with the DC voltage derived from 50% peak sync voltage. This generates the composite sync output signal.

Vertical slicing and double slope integrator

Vertical slicing compares the composite sync signal with a DC level equal to 40 % of the peak sync voltage, similar to the composite sync slicing.
With signal interference (reflections or noise) the reduced vertical slicing level ensures more energy for the vertical pulse integration. The slope is double-integrated to eliminate the influence of signal interference.
The vertical integration delay time t_{dV} can be set from typically 45 µs (pin 4 open) to typically 18 µs (pin 4 grounded).
Between these maximum and minimum values, t_{dV} can be set by a resistor R1 from pin 4 to ground. For optimum sync behaviour with input line sync pulses only, R1 has to be ≥ 3.3 kΩ. In this case t_{dV} is typically ≥ 23 µs.

Vertical sync output Composite sync output

Both output stages are emitter followers with bias currents of 2 mA.

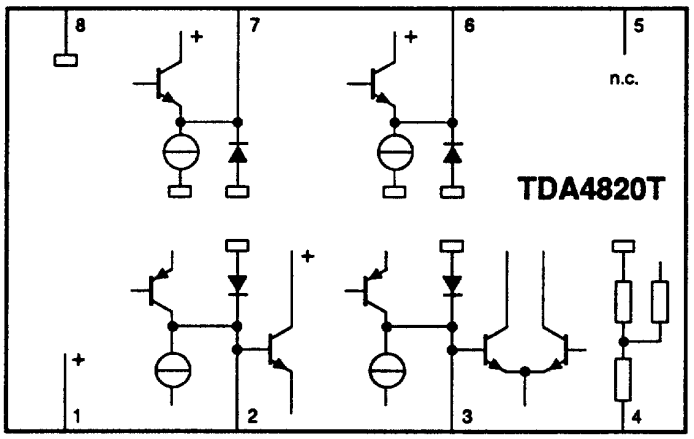


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	13.2	V
V_i	input voltage (pin 2)	−0.5	6	V
I_o	output current (pin 6 and pin 7)	3	−10	mA
T_{stg}	storage temperature range	−25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
T_j	maximum junction temperature	−	150	°C
P_{tot}	total power dissipation	−	500	mW

CHARACTERISTICS

All voltages measured to GND (pin 8); V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12.0	13.2	V
I_P	supply current (pin 1)		4	8	12	mA
Video amplifier						
$V_{2(p-p)}$	input amplitude (peak-to-peak value)	positive video signal AC coupled	0.2	1	3	V
$V_{sync\ (p-p)}$	sync pulse amplitude (pin 2) (peak-to-peak value)	composite sync slicing level 50% for 0.2 V ≤ $V_{2(p-p)}$ ≤ 1.5 V	50	300	500	mV
Z_S	source impedance		–	–	200	Ω
Black level clamping						
I_2	discharge current of C2	during video content	–	5	–	µA
	charge currents of C2	sync below slicing level	–	–40	–	µA
		sync above slicing level	–	–25	–	µA
		during black level	–	–20	–	µA
50% peak sync voltage						
I_3	discharge current of C3	during video content	–	16	–	µA
	maximum charge current of C3		–	–345	–	µA
	reduced charge current of C3	during vertical sync	–	–255	–	µA
	charge current of C3	during sync pulse	–	–160	–	µA
Composite sync slicing (see Fig.4)						
	composite sync slicing level	0.2 V ≤ $V_{2(p-p)}$ ≤ 1.5 V	–	50	–	%
t_{dH}	horizontal delay time (pin 7)	maximum load at pin 7: C_L ≤ 5 pF; R_L ≥ 100 kΩ	–	250	500	ns
Vertical sync separation (see Fig.5)						
	slicing level for vertical sync	0.2 V ≤ $V_{2(p-p)}$ ≤ 1.5 V	–	40	–	%
t_{dV}	vertical leading edge delay times (pin 6)	pin 4 open	30	45	60	µs
		pin 4 grounded	11	18	25	µs
Vertical and composite sync outputs						
V_o	maximum vertical sync output voltage (pin 6)	I_6 = –1 mA	10.0	10.5	11.5	V
V_o	maximum composite sync output voltage (pin 7)	I_7 = –3 mA	10.0	10.5	11.5	V
V_o	minimum output voltages (pins 6 and 7)	$I_{6,7}$ = 1 mA	0.1	0.3	0.6	V
t_W	vertical sync pulse width	pin 4 open; standard signal of 625 lines	–	180	–	µs

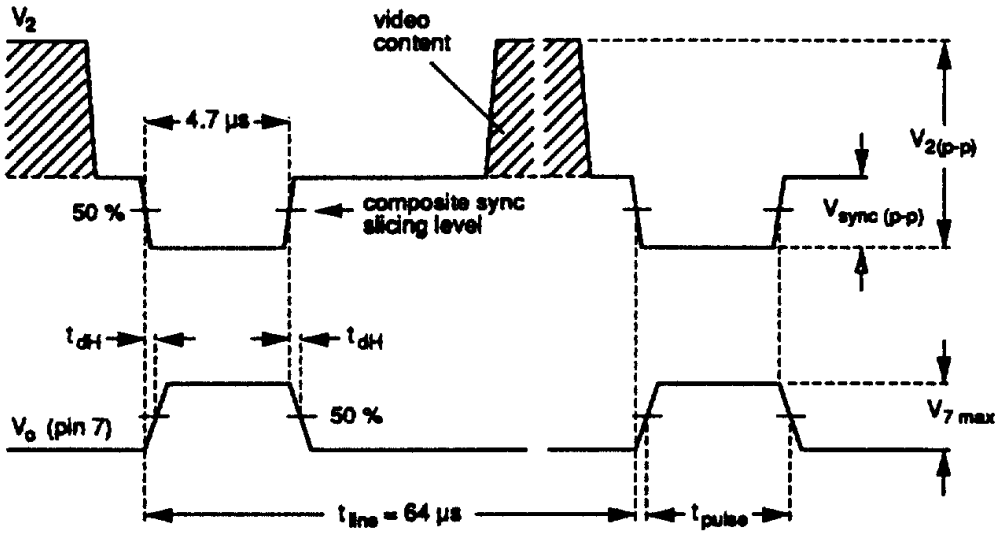
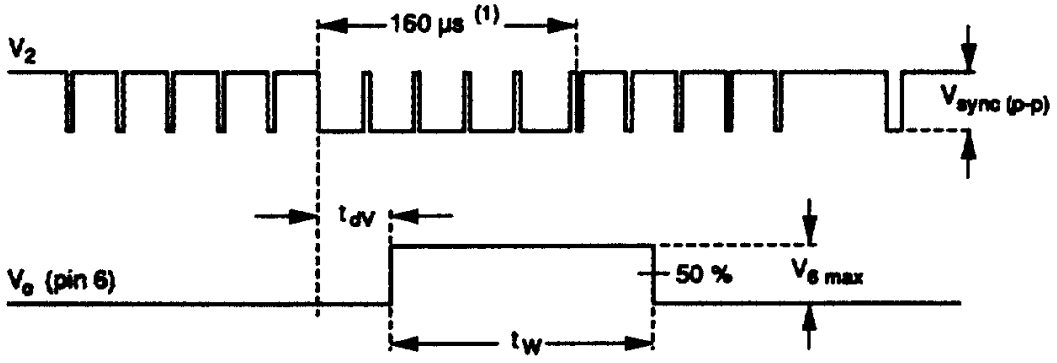


Fig.4 Typical horizontal sync signal.

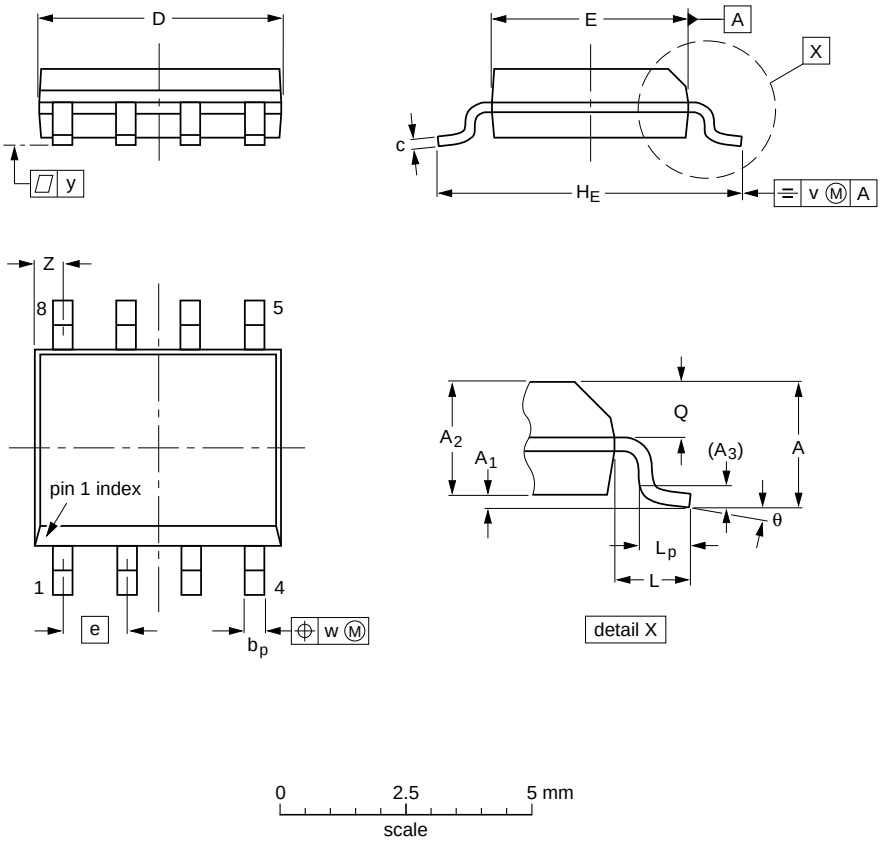


(1) due to 625 line standard

Fig.5 Typical vertical signal

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.