

## Video Processor with RGB Insertion

**Technology:** Bipolar

### Features

- Capacitive coupling of color difference-, Y input signals with black level clamping in the output stages
- Linear saturation adjustment at the color difference input stage
- (G-Y)- and RGB matrix
- Linear processing of inserted RGB-signals
- Same black level for inserted as for matrixed signals
- Linear contrast and brightness adjustment acting on inserted and matrixed signals
- Peak white limiting
- Horizontal and vertical blanking and black level clamping by a super sandcastle-pulse
- White level adjustment by three electronic potentiometers
- Emitter follower output stages as well as drivers for RGB-power stages
- Three identical RGB channels

**Case:** 28-pin dual inline plastic

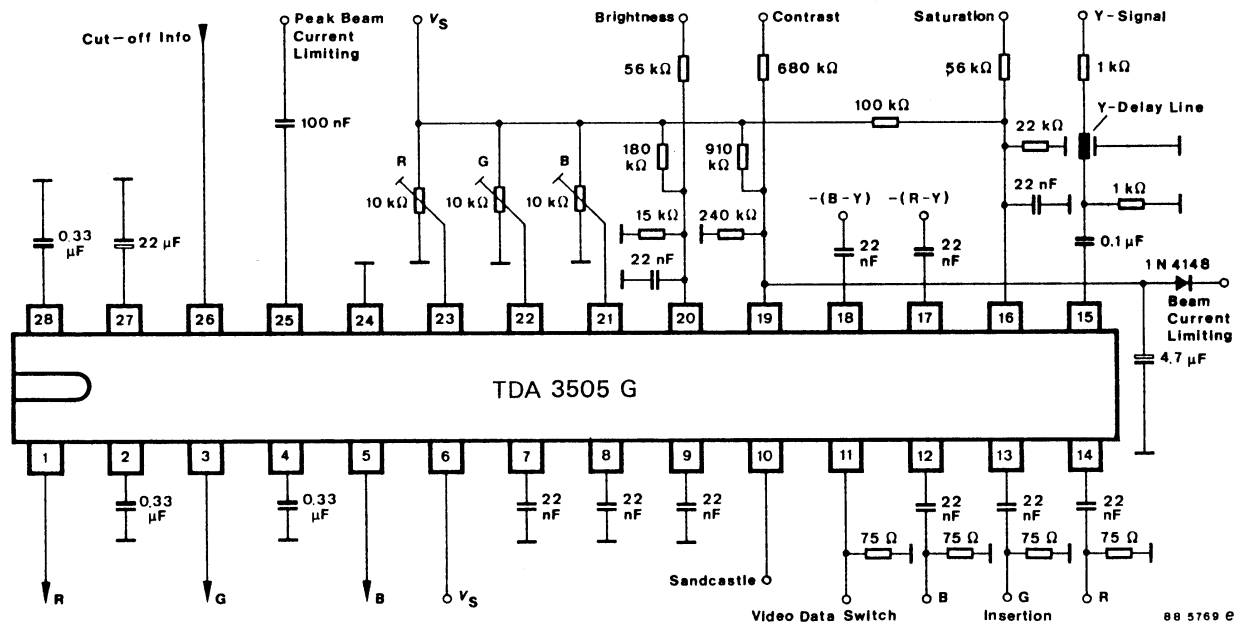


Figure 1 Application circuit

### Absolute Maximum Ratings

Reference point Pin 24

Parameters	Symbol	Value	Unit
Supply voltage Pin 6	$V_S$	13.2	V
External voltages Pins 10, 21, 22, 23, 25 and 26 Pins 16, 19 and 20 Pin 11 No dc voltages allowed at Pins: 1 to 5, 7 to 9, 12 to 15, 17, 18, 27 and 28	$V_{ext}$	0 to $V_S$ 0 to 0.5 $V_{SS}$ -0.5 to +3	V
Currents Pins 1, 3 and 5 Pin 19 Pin 20 Pin 25	$-I_o$ $I_I$ $I_I$ $-I_I$	3 10 5 5	mA mA mA mA
Power dissipation $T_{amb} = 25^\circ\text{C}$	$P_{tot}$	1.7	W
Junction temperature	$T_j$	125	$^\circ\text{C}$
Ambient temperature range	$T_{amb}$	0 to +70	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	-25 to +150	$^\circ\text{C}$

### Electrical Characteristics

 $V_S = 12\text{ V}$ , figure 1, reference point Pin 24,  $T_{amb} = 25^\circ\text{C}$ , unless otherwise specified.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 6	$V_S$	10.8		13.2	V
Supply current	Pin 6	$I_S$		85		mA
<b>Color difference stages</b>						
Input voltage	-(B-Y)-signal for 75% color Pin 18 -(R-Y)-signal for 75% color Pin 17	$V_{ipp}$		1.33 1.05		V
Input resistance	Pins 17 and 18	$R_i$	100			k $\Omega$
Input current during scanning	Pins 17 and 18	$I_i$			1	$\mu\text{A}$
Internal bias clamping voltage	Pins 17 and 18	$V_I$		4.2		V
<b>Saturation</b>						
Control voltage range	$\Delta_{Sat} = -20$ to +6 dB Pin 16	$V_I$		2.1 to 4.3		V
Control voltage for attenuation	$d_{Sat} \geq 40$ dB $d_{satnom} = 0$ dB	$V_I$		3.1	1.8	V
Input current		$I_I$			20	$\mu\text{A}$

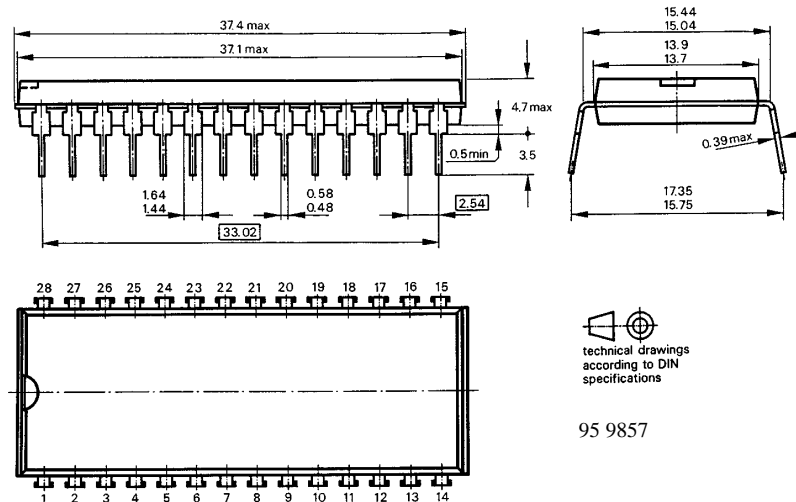
Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
<b>Luminance amplifier</b> Pin 15						
Comp. video signal amplitude		$V_I$		0.45		V
Input resistance		$R_i$	100			k $\Omega$
Input current during scanning		$I_I$			1	$\mu$ A
Internal bias voltage		$V_I$		2.7		V
<b>RGB-Channels, signal switch pin 11</b>						
Signal insertion	“ON” “OFF”	$V_I$	0.9		3 0.4	V
Input current		$I_I$	-100 to + 200			$\mu$ A
<b>RGB insertion inputs</b> Pins 12, 13 and 14						
Black-white input signal	$V_{11} \leq 0.4$ V <sup>1)</sup> $V_{11} \geq 0.9$ V <sup>1)</sup>	$V_{Ipp}$ $V_I$ $V_I$		1 4.3 4.4		V
Input currents during scanning		$I_i$			1	$\mu$ A
<b>Contrast</b> Pin 19						
Control voltage range	$\Delta_{Contr} = -18$ to +3 dB	$V_I$		2 to 4.3		V
Control voltage	$d_{Contr\ nom} = 0$ dB $d_{Contr\ nom} = -6$ dB	$V_I$		3.6 2.8		V
Input current	$V_{25} \geq 6$ V	$I_I$			2	$\mu$ A
<b>Peak beam current limiting</b>						
Internal bias voltage	Pin 25	$V_I$		5.5		V
Input resistance	Pin 25	$R_i$		10		k $\Omega$
Contrast control input current	$V_{25} = 5.1$ V Pin 19	$I_I$		17		mA
<b>Brightness</b> Pin 20						
Control voltage range		$V_I$	1		3	V
Input current		$I_I$			10	$\mu$ A
Control voltage for nom. black level		$V_I$			2	V
Black level change in the control range w.r.t. the nom. black-white signal				$\pm 50$		%
Internal signal limiting w.r.t. the nom. black-white signal and nom. black level	“black” direction “white” direction			-25 120		%
<b>White adjustment</b> Pins 21, 22 and 23						
AC amplification <sup>2)</sup>	$V_{21,22,23} = 5.5$ V = 0 V = 12 V	$G_v$		100 60 140		%
Input resistance		$R_i$		20		k $\Omega$

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
<b>RGB emitter follower outputs</b> Pins 1, 3 and 5						
Nom.: Contr, Sat, white adjustment Output signals	Black-white	$V_{0pp}$		2		V
Black level without cut off control	$V_{2,4,28} = 10$ V	$V_0$		6.7		V
Current of the internal current sources		I		3		mA
Cut off control range		$\Delta V_0$		4.6		V
<b>Cut off control</b> Pin 26						
Input voltage range		$V_I$	0		6.5	V
Voltage difference between cut off and leakage current levels <sup>3)</sup>		$\Delta V_I$		0.5		V
Input voltage clamping during flyback		$V_I$		0		V
<b>Amplifications, nom.:</b> Contr, Sat, white adjustment, reference point Pin 15						
Voltage amplification	Pins 1, 3 and 5	$G_V$		16		dB
Frequency response	B = 0 to 5 MHz	d			3	dB
<b>(R-Y)-signal, reference point Pin 17</b>						
Voltage amplification	Output R Pin 1	$G_V$		6		dB
Frequency response	B = 0 to 2 MHz Pin 1	d			3	dB
<b>(B-Y)-signal, reference point Pin 18</b>						
Voltage amplification	Output B Pin 5	$G_V$		6		dB
Frequency response	B = 0 to 2 MHz Pin 5	d			3	dB
<b>RGB insertion signals, reference point Pins 12, 13 and 14</b>						
Voltage amplification	Pins 1, 3 and 5	$G_V$		6		dB
Frequency response	B = 0 to 6 MHz Pins 1, 3 and 5	d			3	dB
<b>Sandcastle detector with 3 thresholds for separation of sandcastle pulse, pin 10</b>						
H- and V-pulses blanking to ultra black (-25 %)		$V_i$	2		3	V
H-pulse		$V_i$	4		5	V
Clamping pulse	$t_p \geq 3.5$ $\mu$ s	$V_I$	7.5			V
No gating		$V_I$			1	V
Input current		$-I_I$			110	$\mu$ A

- 1) During clamping pulse time the inserted signals are clamped at the black level of the RGB signals matrixed by the color difference – and Y-stages ( $V_{11} \leq 0.4$  V). At  $V_{11} \geq 0.9$  V the inserted signals are clamped at an internal bias voltage.
- 2) If the inputs for white adjustment (Pins 21, 22 and 23) are not connected there is an internal bias voltage of 5.5 V.
- 3) Black level at the measured channel at nom. value where is in other two channels at ultra black level.  
By leakage current measure: all three channels gated at ultra black level.

## Dimensions in mm

Package: DIP 28



**We reserve the right to make changes to improve technical design without further notice.**

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