INTEGRATED CIRCUIT

TOSHIBA

TECHNICAL DATA

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT
TC9210P, TC9211P
SILICON MONOLITHIC
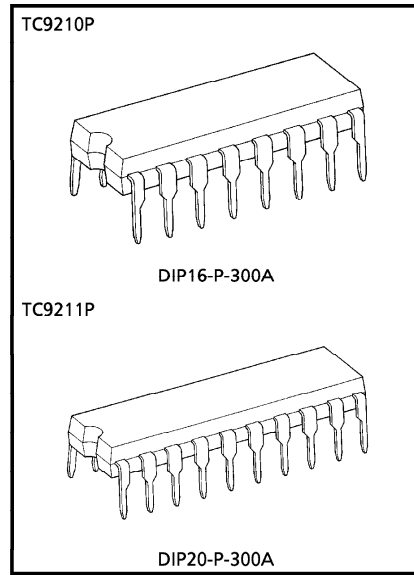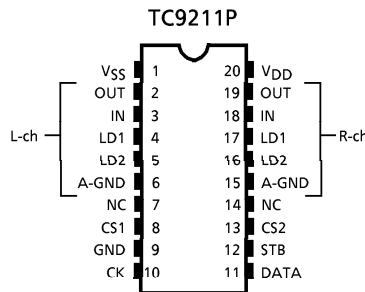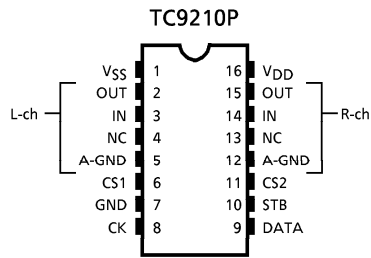
ELECTRONIC VOLUME CONTROL IC

TC9210P and TC9211P are electronic volume control ICs developed for use in audio equipment such as home stereo sets.
The volume, balance and loudness circuits can be controlled by serial data which are input externally.

FEATURES

● Forty-level volume control in 2dB steps from 0dB to 78dB, ∞ dB.

● The volume circuit features 2 built-in channels which can be controlled independently, thus controlling balance.

● TC9211P features a built-in loudness circuit (20dB tap).

● Single and dual power supply operation.

● Chip select input allows control of up to four of these chips on the same bus.

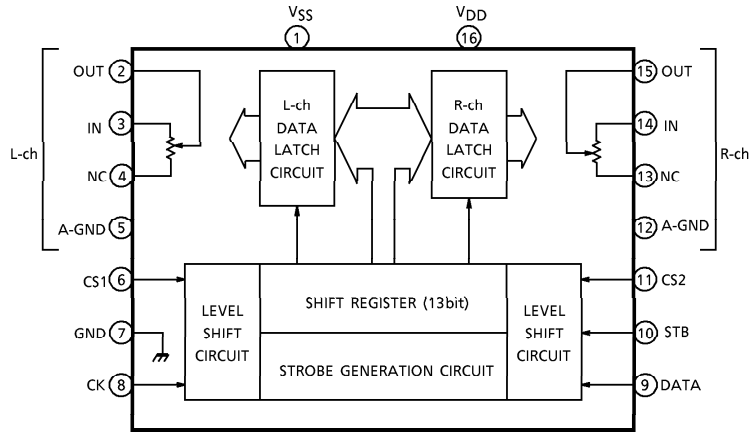● Polysilicon resistors enables low-distortion, high-performance volume systems.

TC9210P

DIP16-P-300A

TC9211P

DIP20-P-300A

Weight DIP16-P-300A : 1.0g (Typ.)
　　　　DIP20-P-300A : 1.4g (Typ.)

PIN CONNECTION

TC9210P

V$_{SS}$	1	16	V$_{DD}$
OUT	2	15	OUT
IN	3	14	IN
NC	4	13	NC
A-GND	5	12	A-GND
CS1	6	11	CS2
GND	7	10	STB
CK	8	9	DATA

L-ch (pins 2,3) ─ R-ch (pins 14,15)

TC9211P

V$_{SS}$	1	20	V$_{DD}$
OUT	2	19	OUT
IN	3	18	IN
LD1	4	17	LD1
LD2	5	16	LD2
A-GND	6	15	A-GND
NC	7	14	NC
CS1	8	13	CS2
GND	9	12	STB
CK	10	11	DATA

L-ch (pins 2,3,4,5) ─ R-ch (pins 16,17,18,19)

BLOCK DIAGRAM (TC9210P)

BLOCK DIAGRAM (TC9211P)

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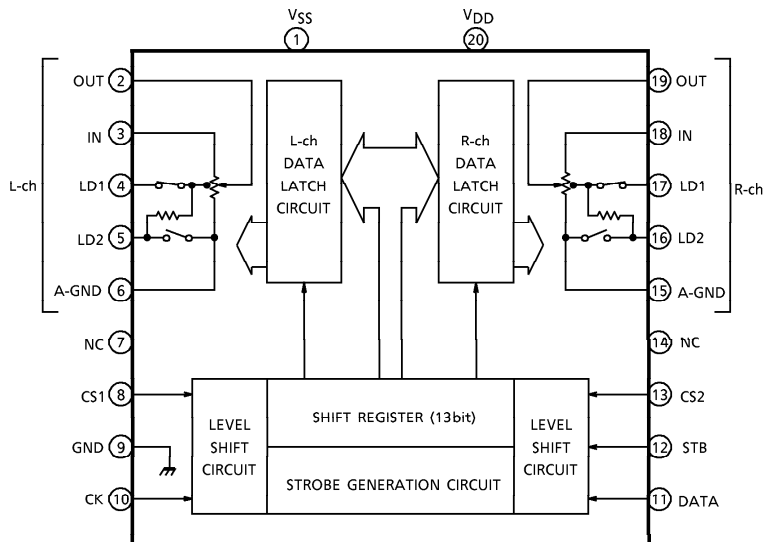
PIN FUNCTION NUMBERS IN PARENTHESES APPLY TO TC9210P

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION AND OPERATION	NOTE
1 (1)	V_{SS}	Negative power supply pin	Dual power supply: $V_{DD} = 6.0 \sim 17V$, $GND = 0V$, $V_{SS} = -6.0 \sim -17V$	—
9 (7)	GND	Digital ground pin		
20 (16)	V_{DD}	Positive power supply pin	Single power supply: $V_{DD} = 6.0 \sim 18V$, $GND = V_{SS} = 0V$	
2 (2)	L-OUT	Volume output pins	● Volume circuit (TC9211P)	—
19 (15)	R-OUT			
3 (3)	L-IN	Volume input pins		
18 (14)	R-IN			
4 (—)	L-LD1	Tap output pins for loudness		
17 (—)	R-LD1			
5 (—)	L-LD2			
16 (—)	R-LD2			
6 (5)	L-A-GND	Analog ground pins		
15 (12)	R-A-GND			
8 (6)	CS1	Chip select input pins	Switching chip select code allows control of up to 4 chips simultaneously on one bus.	—
13 (11)	CS2			
10 (8)	CK	Clock input pin	Clock input for data transfer	Low threshold value input pins
11 (9)	DATA	Data input pin	Serial data input for setting volume	
12 (10)	STB	Strobe input pin	Strobe input for writing data	
7, 14 (4, 13)	NC	Not connected		—

Volume circuit diagram (TC9211P):

OUT, IN, LD1, LD2, A-GND pins with LA1, LA2 switches, 24.7kΩ, 17.5kΩ, 3.3kΩ resistors

	LA1	LA2
Loudness "ON"	ON	OFF
Loudness "OFF"	OFF	ON

OPERATIONAL DESCRIPTION

1. Setting volume values (attenuation)

The volume values are set using 13bit serial data.

● Data format
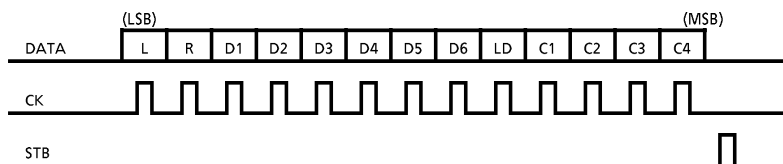
1) L is left-channel select data ; R is right-channel select data.
When L = 1, left-channel volume is set ; when R = 1, right-channel volume is set. (When R = L = 1, both channel volumes are set simultaneously).

2) LD is loudness setting data. When LD = 1, loudness is on. (Only for TC9211P. Set to 0 for TC9210P.)

3) D1-D6 are volume value setting data.

VOLUME VALUE	D1	D2	D3	D4	D5	D6
0dB	0	0	0	0	0	0
2	1	0	0	0	0	0
4	0	1	0	0	0	0
6	1	1	0	0	0	0
8	0	0	1	0	0	0
10	1	0	1	0	0	0
12	0	1	1	0	0	0
14	1	1	1	0	0	0
16	0	0	0	1	0	0
18	1	0	0	1	0	0
20	0	1	0	1	0	0
22	1	1	0	1	0	0
24	0	0	1	1	0	0
26	1	0	1	1	0	0
28	0	1	1	1	0	0
30	1	1	1	1	0	0
32	0	0	0	0	1	0
34	1	0	0	0	1	0
36	0	1	0	0	1	0
38	1	1	0	0	1	0

| VOLUME VALUE	D1	D2	D3	D4	D5	D6
40dB	0	0	1	0	1	0
42	1	0	1	0	1	0
44	0	1	1	0	1	0
46	1	1	1	0	1	0
48	0	0	0	1	1	0
50	1	0	0	1	1	0
52	0	1	0	1	1	0
54	1	1	0	1	1	0
56	0	0	1	1	1	0
58	1	0	1	1	1	0
60	0	1	1	1	1	0
62	1	1	1	1	1	0
64	0	0	0	0	0	1
66	1	0	0	0	0	1
68	0	1	0	0	0	1
70	1	1	0	0	0	1
72	0	0	1	0	0	1
74	1	0	1	0	0	1
76	0	1	1	0	0	1
78	1	1	1	0	0	1
∞	0	0	0	1	0	1

(Note) Note that if data other than those listed above are input, volume values are undefined.

4) C1-C4 are chip select code data.
   Code data are set according to CS1 and CS2 input.

CS1	CS2	C1	C2	C3	C4
L	L	0	0	1	1
H	L	1	0	1	1
L	H	0	1	1	1
H	H	1	1	1	1

2. Serial data timing

   Input CK, DATA and STB according to the following timing.
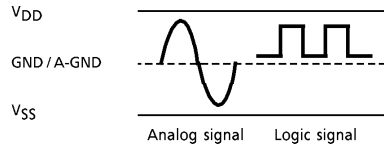

$a \geq 0.5\mu s, b \geq 1.0\mu s$
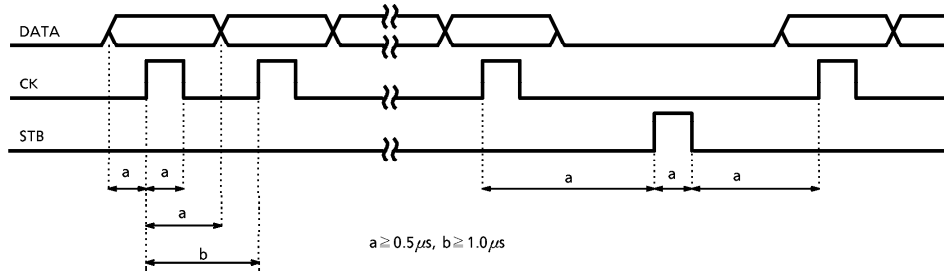
3. Single and dual power supply operation

   TC9210P and TC9211P can operate with single or dual power supplies.
   With single or dual power supply, serial data logic level can be 0-5V.

● Single power supply operation

V_{DD}

A-GND
(1 / 2 V_{DD})

GND / V_{SS}

Analog signal   Logic signal

● Dual power supply operation

V_{DD}

GND / A-GND

V_{SS}

Analog signal   Logic signal
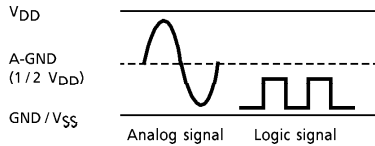
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage (1)	V_{DD}-V_{SS}	$-0.3\sim36$	V
Power Supply Voltage (2)	V_{DD}-GND	$-0.3\sim20$	V
GND Input Voltage	V_{IN} (1)	$-0.3\sim V_{DD}+0.3$	V
V_{SS} Input Voltage	V_{IN} (2)	$V_{SS}-0.3\sim V_{DD}+0.3$	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{opr}	$-40\sim85$	°C
Storage Temperature	T_{stg}	$-65\sim150$	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{DD} = 15V, V_{SS} = $-$ 15V, GND = 0V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage (1)		V_{DD}-V_{SS}	—	Dual power supply operation		12	~	34	V
Operating Supply Voltage (2)		V_{DD}-GND	—	Single power supply operation		6.0	~	18	V
Operating Supply Current		I_{DD}	1	No load, No input		—	0.5	1.0	mA
Input Voltage	"H" Level	V_{IH} (1)	—	CK, DATA, STB terminal V_{DD} = 6.0~18V		4.0	~	V_{DD}	V
	"L" Level	V_{IL} (1)				GND	~	1.0	
Input Voltage	"H" Level	V_{IH} (2)	—	CS1, CS2 terminal		$V_{DD}\times0.7$	~	V_{DD}	V
	"L" Level	V_{IL} (2)				GND	~	$V_{DD}\times0.3$	
Input Current	"H" Level	I_{IH}	—	CK, DATA, STB, CS1, CS2 terminal	V_{IH} = 15V	-1.0	~	1.0	μA
	"L" Level	I_{IL}			V_{IL} = 0V	-1.0	~	1.0	
Operating Frequency Range		fop	—	CK, DATA, STB terminal		0	~	1.0	MHz
Minimum Clock Frequency		Tck				0.5	—	—	μs
Volume Resistance Value		R_{VR}	—	Loudness "OFF"		18.5	27.5	36.5	kΩ
Step Deviation		ΔVR	—	Volume step deviation		-1.2	~	1.2	dB
Analog Switch ON Resistance		R_{ON}	—	Internal analog switch		—	350	600	Ω
Analog Switch OFF Leak Current		I_{OFF}				-0.1	~	0.1	μA
Total Harmonic Distortion		THD	1	f_{IN} = 1kHz V_{IN} = 1Vrms R_g = 600Ω, R_L = 100kΩ BW = 20Hz~20kHz		—	0.005	—	%
Maximum Attenuation		ATT_{MAX}				—	100	—	dB
Output Noise Voltage		V_N				—	1.0	—	μV_{rms}
Cross Talk		C·T				—	100	—	dB

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TEST CIRCUIT 1 (I_{DD} / THD / ATT_{MAX} / V_N / C·T)
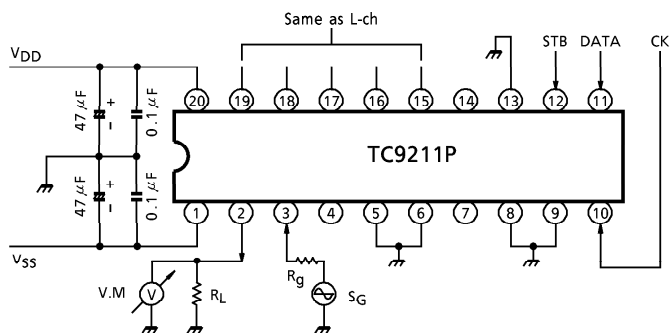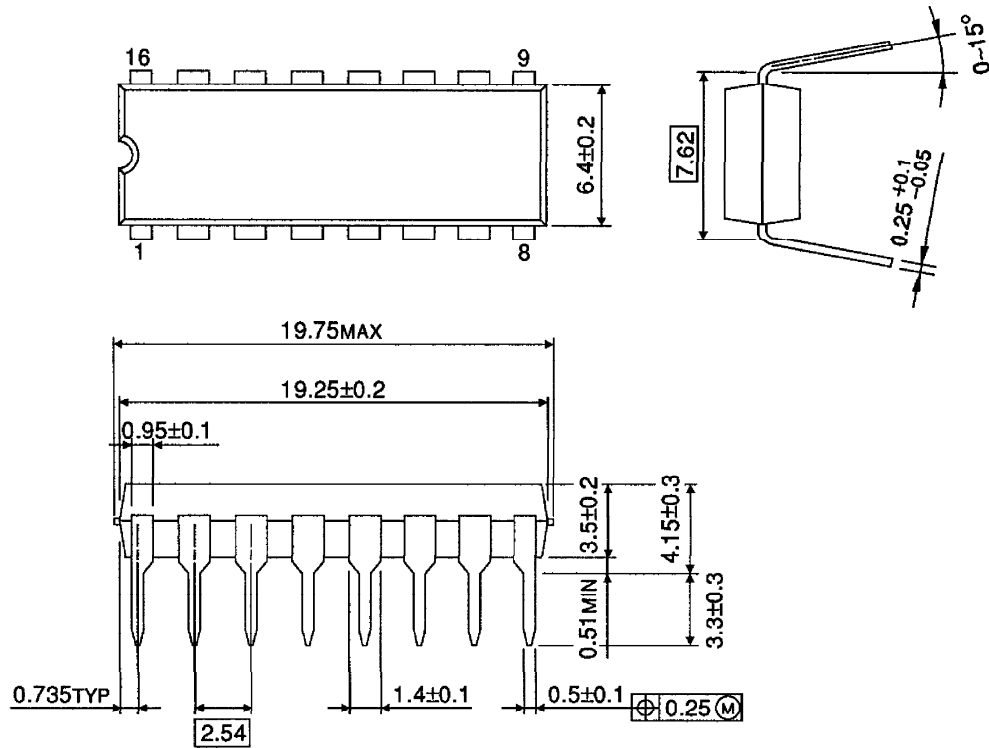

APPLICATION CIRCUIT (TC9211P)
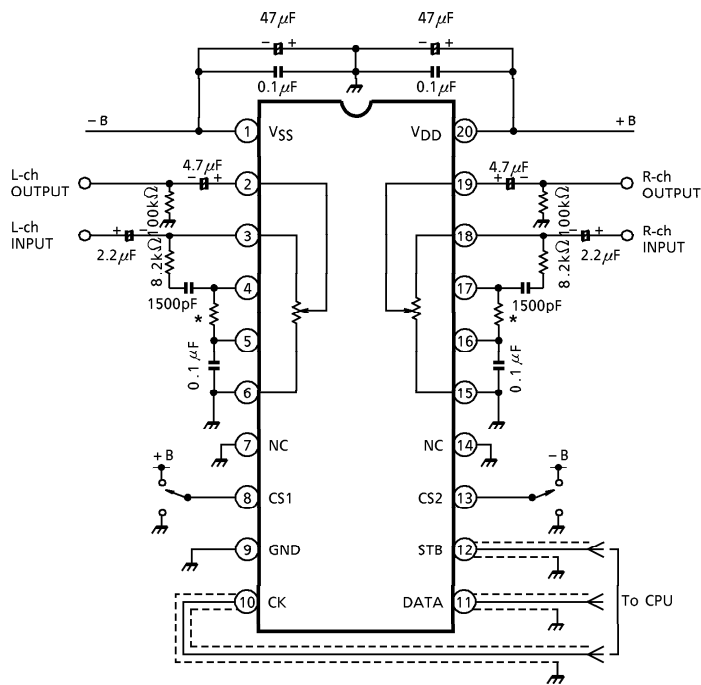
* For preventing noise when loudness is turned on or off. $R = 220k\Omega \sim 470k\Omega$

(Note) High-frequency digital signals are input to pins CK, DATA and STB. Since these signals may cause noise in analog circuits, either use shield wire for CK, DATA, and STB signal lines, or design the pattern so that these signal lines are protected by the ground line.

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OUTLINE DRAWING
DIP16-P-300A

Unit : mm

Weight : 1.0g (Typ.)

OUTLINE DRAWING
DIP20-P-300A

Unit : mm

Weight : 1.4g (Typ.)