TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LVX4245FS

Dual Supply Octal Bus Transceiver

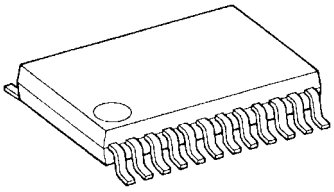
The TC74LVX4245FS is a dual supply, advanced high-speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 5V bus and a 3.3V bus in mixed 5V/3.3V supply systems' it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is intended for 2 way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated. The A-port interfaces with the 5V bus, the B-port with the 3.3V bus.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



SSOP24-P-300-0.65A

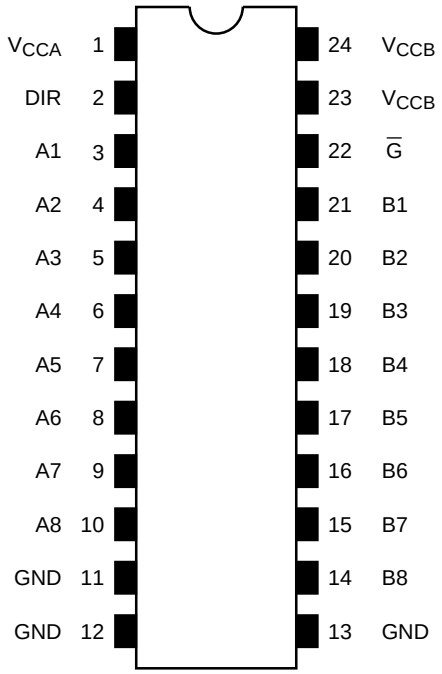
Weight: 0.14 g (typ.)

Features

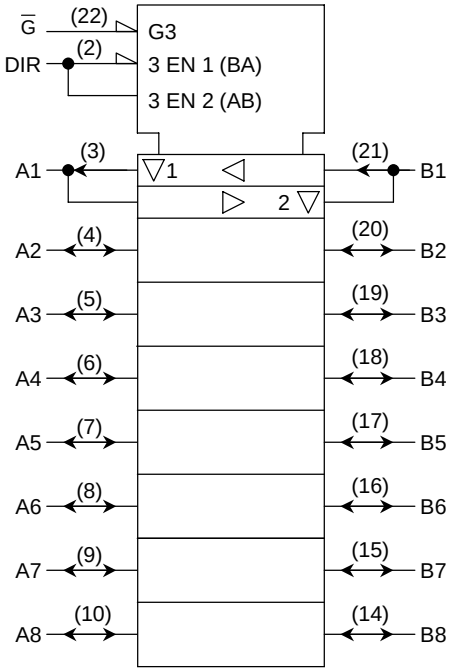
- Bi-directional interface between 5 V and 3 V buses
- High-speed: t_{pd} = 6.0 ns (typ.)
  (V_{CCA} = 5.0 V, V_{CCB} = 3.3 V)
- Low power dissipation: I_{CC} = 8 μA (max) (Ta = 25°C)
- Symmetrical output impedance: I_{OUTA} = ±24 mA (min)
  I_{OUTB} = ±12 mA (min)
  (V_{CCA} = 4.5 V, V_{CCB} = 3.0 V)
- Low noise: V_{OLP} = 1.5 V (max)
- Package: SSOP (shrink small outline package)

Note 1: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pin must have their input levels fixed by means of pull up or pull down resistors.

Pin Assignment (top view)



IEC Logic Symbol



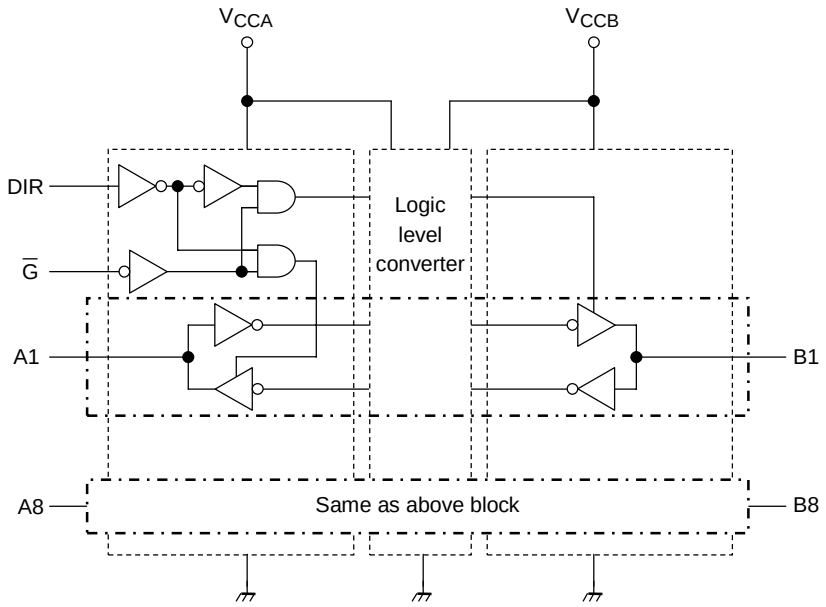
Truth Table

Inputs		Outputs	Function	
$\overline{G}$	DIR		A-Bus	B-Bus
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	High impedance	

X: Don’t care

Z: High impedance

Block Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CCA}	−0.5 to 7.0	V
(Note 2)	V_{CCB}	−0.5 to V_{CCA} + 0.5	
DC input voltage	V_{IN}	−0.5 to V_{CCA} + 0.5	V
DC bus I/O voltage	$V_{I/OA}$	−0.5 to V_{CCA} + 0.5	V
	$V_{I/OB}$	−0.5 to V_{CCB} + 0.5	
Input diode current	I_{IK}	−20	mA
Output diode current	$I_{I/OK}$	±50	mA
DC output current	I_{OUTA}	±50	mA
	I_{OUTB}	±50	
DC V_{CC}/ground current	I_{CCA}	±200	mA
	I_{CCB}	±100	
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 2: $V_{CCA} > V_{CCB}$
Don't use under the condition that V_{CCB} is 0 V.

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CCA}	4.5 to 5.5	V
	V_{CCB}	2.7 to 3.6	
Input voltage	V_{IN}	0 to V_{CCA}	V
Bus I/O voltage	$V_{I/OA}$	0 to V_{CCA}	V
	$V_{I/OB}$	0 to V_{CCB}	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 8 (V_{CCA} = 4.5 to 5.5 V)	ns/V
		0 to 8 (V_{CCB} = 2.7 to 3.6 V)	

Electrical Characteristics

DC Characteristics (V_{CCA}) (V_{CCB} = 2.7 to 3.6 V)

Characteristics		Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
				V_{CCA} (V)	Min	Typ.	Max	Min	Max	
Input voltage	H-level	V_{IHA}	DIR, $\overline{G}$, An	4.5 to 5.5	2.0	—	—	2.0	—	V
	L-level	V_{ILA}	DIR, $\overline{G}$, An	4.5 to 5.5	—	—	0.8	—	0.8	
Output voltage	H-level	V_{OHA}	V_{INA} = V_{IHA} or V_{ILA}, I_{OH} = −100 μA	4.5	4.4	4.5	—	4.4	—	V
			V_{INB} = V_{IHB} or V_{ILB}, I_{OH} = −24 mA	4.5	3.86	—	—	3.76	—	
	L-level	V_{OLA}	V_{INA} = V_{IHA} or V_{ILA}, I_{OL} = 100 μA	4.5	—	0.0	0.1	—	0.1	
			V_{INB} = V_{IHB} or V_{ILB}, I_{OL} = 24 mA	4.5	—	—	0.36	—	0.44	
3-state output Off-state current		I_{OZA}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB} $V_{I/OA}$ = V_{CCA} or GND	5.5	—	—	±0.5	—	±5.0	μA
Input leakage current		I_{INA}	V_{IN} (DIR, $\overline{G}$) = V_{CCA} or GND	5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND	5.5	—	—	8.0	—	80.0	μA
		I_{CCTA}	V_{INA} = 3.4 V (per input) V_{CCA} or GND (other input)	5.5	—	—	2.3	—	2.5	mA

DC Characteristics (V_{CCB}) (V_{CCA} = 4.5 to 5.5 V)

Characteristics		Symbol	Test Condition		Ta = 25°C				Ta = −40 to 85°C		Unit
					V_{CCB} (V)	Min	Typ.	Max	Min	Max	
Input voltage	H-level	V_{IHB}	Bn		2.7	2.0	—	—	2.0	—	V
					3.6	2.2	—	—	2.2	—	
	L-level	V_{ILB}	Bn		2.7	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output voltage	H-level	V_{OHB}	V_{INA} = V_{IHA} or V_{ILA}	I_{OH} = −100 μA	3.0	2.9	3.0	—	2.9	—	V
				I_{OH} = −8 mA	2.7	2.26	—	—	2.20	—	
				I_{OH} = −12 mA	3.0	2.48	—	—	2.40	—	
	L-level	V_{OLB}	V_{INA} = V_{IHA} or V_{ILA}	I_{OL} = 100 μA	3.0	—	0.0	0.1	—	0.1	
				I_{OL} = 8 mA	2.7	—	—	0.31	—	0.40	
				I_{OL} = 12 mA	3.0	—	—	0.31	—	0.40	
3-state output Off-state current		I_{OZB}	V_{INA} = V_{IHA} or V_{ILA} $V_{I/OB}$ = V_{CCB} or GND		3.6	—	—	±0.5	—	±5.0	μA
Quiescent supply current		I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		3.6	—	—	5.0	—	50.0	μA
		I_{CCTB}	V_{INA} = 3.0 V (per input) V_{CCB} or GND (other input)		3.6	—	—	0.35	—	0.50	mA

AC Characteristics (input: $t_r = t_f = 3$ ns, $C_L = 50$ pF, $R_L = 500\ \Omega$, $V_{CCA} = 5.0 \pm 0.5$ V)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (An⇒Bn)	t_{pLH}	Input: An Outpu: Bn (DIR = "H")	2.7	—	7.1	9.5	1.0	10.5	ns
	t_{pHL}		3.3 ± 0.3	—	6.5	8.6	1.0	9.5	
3-state output enable time ($\overline{G}$ ⇒Bn)	t_{pZL}		2.7	—	9.5	12.5	1.0	13.8	ns
	t_{pZH}		3.3 ± 0.3	—	8.6	11.4	1.0	12.5	
3-state output disable time ($\overline{G}$ ⇒Bn)	t_{pLZ}		2.7	—	5.3	9.1	1.0	10.0	ns
	t_{pHZ}		3.3 ± 0.3	—	5.3	9.1	1.0	10.0	
Propagation delay time (Bn⇒An)	t_{pLH}	Input: Bn Output: An (DIR = "L")	2.7	—	7.0	9.5	1.0	10.5	ns
	t_{pHL}		3.3 ± 0.3	—	6.4	8.6	1.0	9.5	
3-state output enable time ($\overline{G}$ ⇒An)	t_{pZL}		2.7	—	8.5	11.6	1.0	12.7	ns
	t_{pZH}		3.3 ± 0.3	—	7.7	10.5	1.0	11.5	
3-state output disable time ($\overline{G}$ ⇒An)	t_{pLZ}		2.7	—	5.1	6.8	1.0	7.5	ns
	t_{pHZ}		3.3 ± 0.3	—	5.1	6.8	1.0	7.5	
Output to output skew	t_{osLH}	(Note 3)	2.7	—	—	1.5	—	1.5	ns
	t_{osHL}		3.3 ± 0.3	—	—	1.5	—	1.5	
Input capacitance	C_{INA}	DIR, $\overline{G}$	3.3 ± 0.3	—	5	10	—	10	pF
Bus input capacitance	$C_{I/O}$	An, Bn	3.3 ± 0.3	—	13	—	—	—	pF
Power dissipation capacitance (Note 4)	C_{PDA}	A⇒B (DIR = "H")	3.3 ± 0.3	—	17	—	—	—	pF
		B⇒A (DIR = "L")	3.3 ± 0.3	—	25	—	—	—	
	C_{PDB}	A⇒B (DIR = "H")	3.3 ± 0.3	—	4	—	—	—	
		B⇒A (DIR = "L")	3.3 ± 0.3	—	4	—	—	—	

Note 3: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

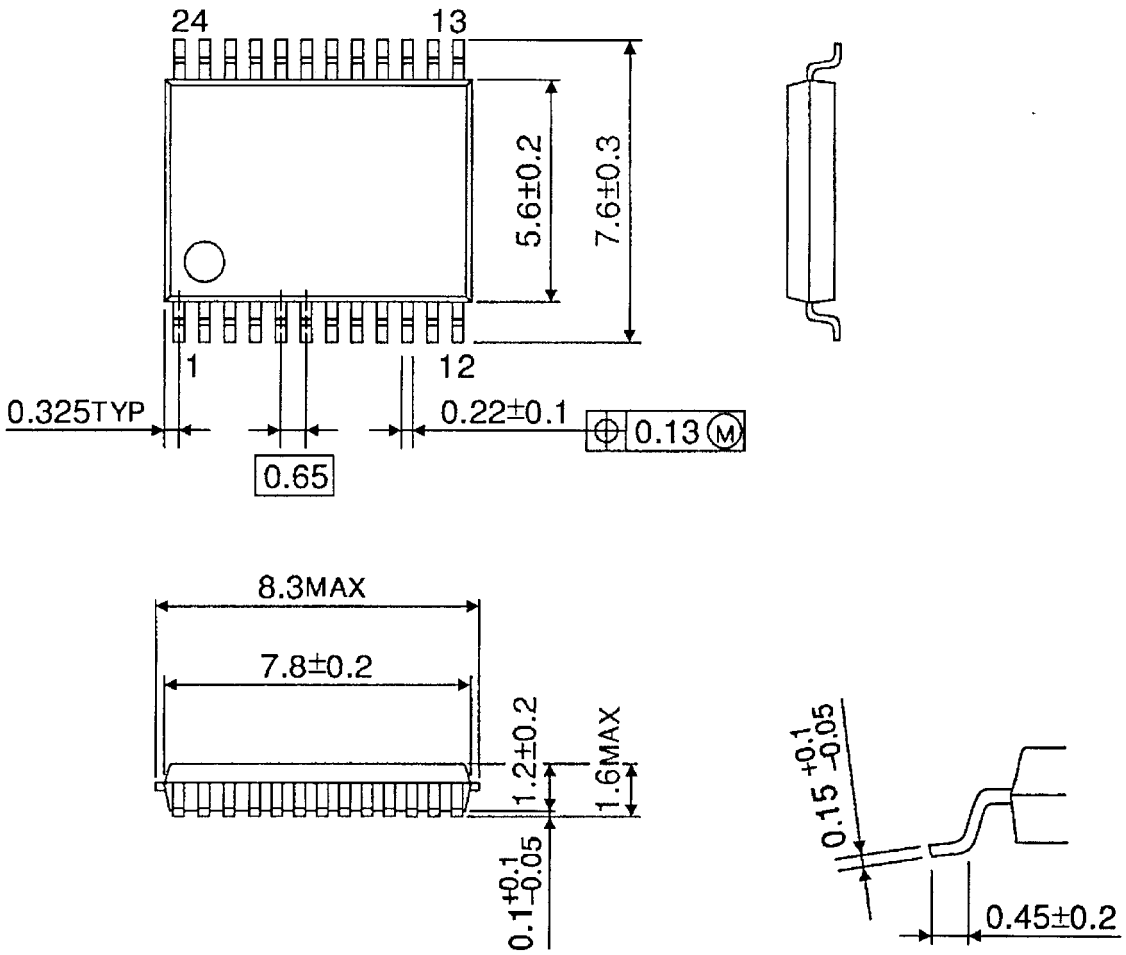
Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3$ ns, $C_L = 50$ pF, $R_L = 500\ \Omega$)

Characteristics		Symbol	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic	V_{OL} (A)	V_{OLPA}	Input: Bn Output: An (DIR = "L")	5.0	3.3	1.0	1.5	V
Quiet output mimimum dynamic	V_{OL} (A)	V_{OLVA}		5.0	3.3	−0.6	−1.2	V
Quiet output maximum dynamic	V_{OL} (B)	V_{OLPB}	Input: An Output: Bn (DIR = "H")	5.0	3.3	0.8	1.2	V
Quiet output mimimum dynamic	V_{OL} (B)	V_{OLVB}		5.0	3.3	−0.5	−0.8	V
Minimum high level dynamic input voltage	V_{IH} (A)	V_{IHDA}	Input: An	5.0	3.3	—	2.0	V
Maximum low level dynamic input voltage	V_{IL} (A)	V_{ILDA}	Input: An	5.0	3.3	—	0.8	V
Minimum high level dynamic input voltage	V_{IH} (B)	V_{IHDB}	Input: Bn	5.0	3.3	—	2.0	V
Maximum low level dynamic input voltage	V_{IL} (B)	V_{ILDB}	Input: Bn	5.0	3.3	—	0.8	V

Package Dimensions

SSOP24-P-300-0.65A Unit : mm



Weight: 0.14 g (typ.)

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