



MICROCHIP

**TC4404
TC4405**

1.5A DUAL OPEN-DRAIN MOSFET DRIVERS

FEATURES

- Independently-Programmable Rise and Fall Times
- Low Output Impedance 7Ω Typ.
- High Speed t_R , t_F <30nsec with 1000pF Load
- Short Delay Times < 30nsec
- Wide Operating Range 4.5V to 18V
- Latch-Up Protected Will Withstand > 500mA Reverse Current (Either Polarity)
- Input Withstands Negative Swings Up to – 5V

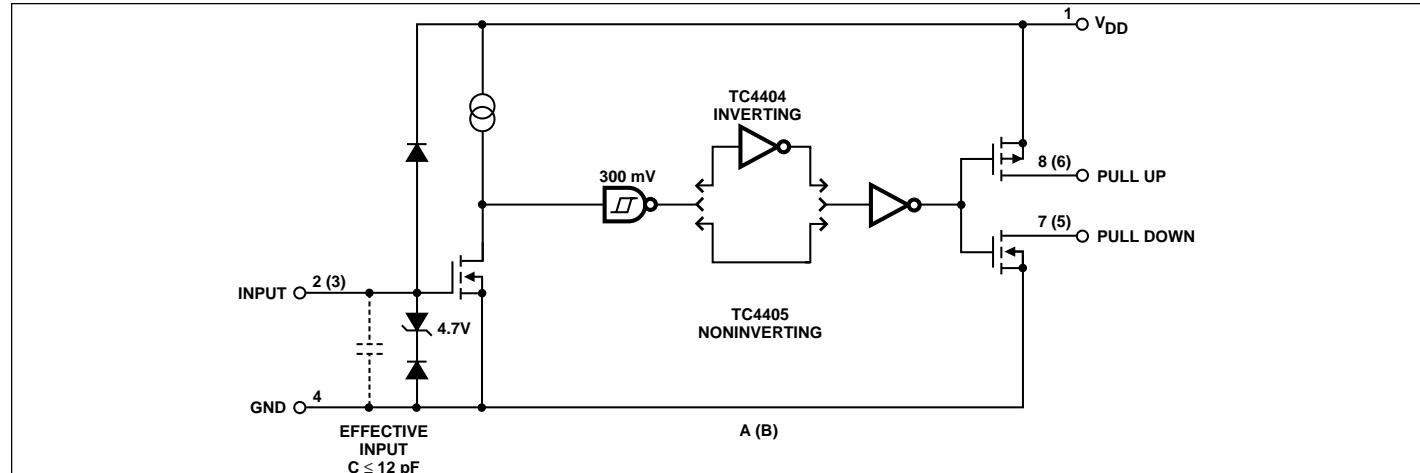
APPLICATIONS

- Motor Controls
- Driving Bipolar Transistors
- Driver for Non-overlapping Totem Poles
- Reach-Up/Reach-Down Driver

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC4404COA	8-Pin SOIC	0°C to +70°C
TC4404CPA	8-Pin PDIP	0°C to +70°C
TC4404EOA	8-Pin SOIC	– 40°C to +85°C
TC4404EPA	8-Pin PDIP	– 40°C to +85°C
TC4404MJA	8-Pin CerDIP	– 55°C to +125°C
TC4405COA	8-Pin SOIC	0°C to +70°C
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FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS: Specifications measured over operating temperature range with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$-0V \leq V_{IN} \leq V_{DD}$	-10	—	10	μA
Output						
V_{OH}	High Output Voltage	$V_{DD} - 0.025$	—	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	$I_{OUT} = 10\text{ mA}, V_{DD} = 18V; \text{Any Drain}$	—	9	12	Ω
I_{PK}	Peak Output Current (Any Drain)	Duty cycle <2%, $t \leq 300\mu\text{sec}$	—	1.5	—	A
I_{DC}	Continuous Output Current (Any Drain)		—	—	100	mA
I_R	Latch-Up Protection (Any Drain) Withstand Reverse Current	Duty cycle <2%, $t \leq 300\mu\text{sec}$	> 500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time Figure 1, $C_L = 1000\text{pF}$		—	—	40	nsec
t_F	Fall Time Figure 1, $C_L = 1000\text{pF}$		—	—	40	nsec
t_{D1}	Delay Time Figure 1, $C_L = 1000\text{pF}$		—	—	40	nsec
t_{D2}	Delay Time Figure 1, $C_L = 1000\text{pF}$		—	—	60	nsec
Power Supply						
I_S	Power Supply Current	$V_{IN} = 3V$ (Both Inputs) $V_{IN} = 0V$ (Both Inputs)	—	—	8	mA
			—	—	0.6	mA

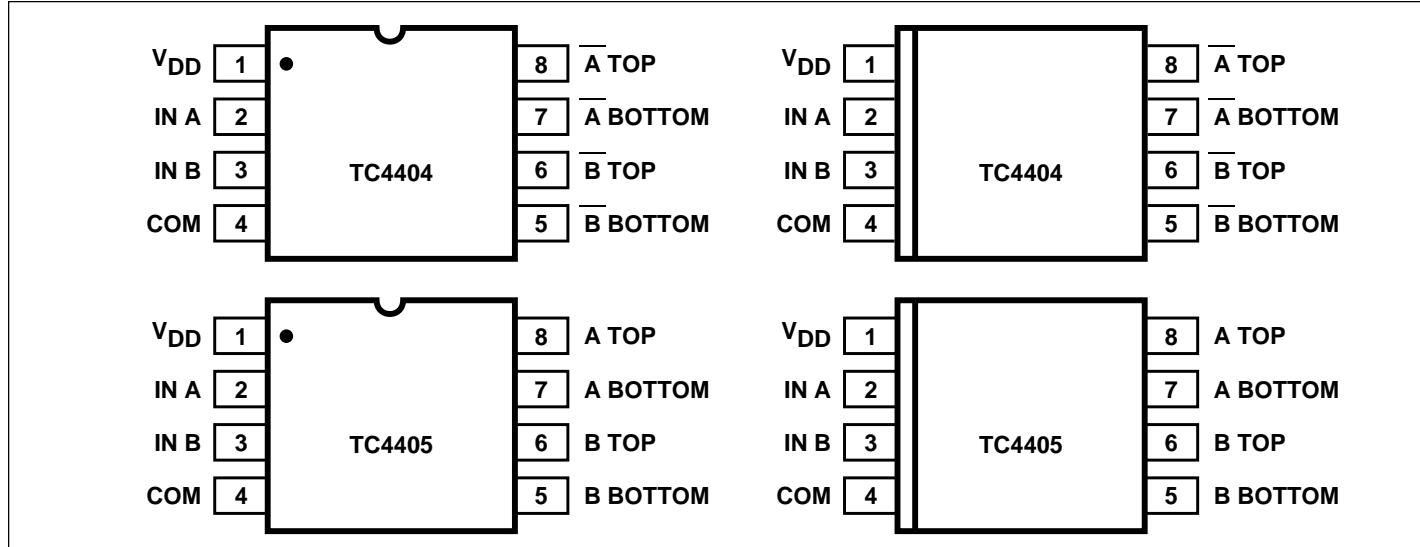
NOTE 1. Switching times guaranteed by design.

Circuit Layout Guidelines

Avoid long power supply and ground traces (added inductance causes unwanted voltage transients). Use power and ground planes wherever possible. In addition, it is advisable that low ESR bypass capacitors ($4.7\mu\text{F}$ or $10\mu\text{F}$

tantalum) be placed as close to the driver as possible. The driver should be physically located as close to the device it is driving as possible to minimize the length of the output trace.

PIN CONFIGURATIONS (DIP and SOIC)



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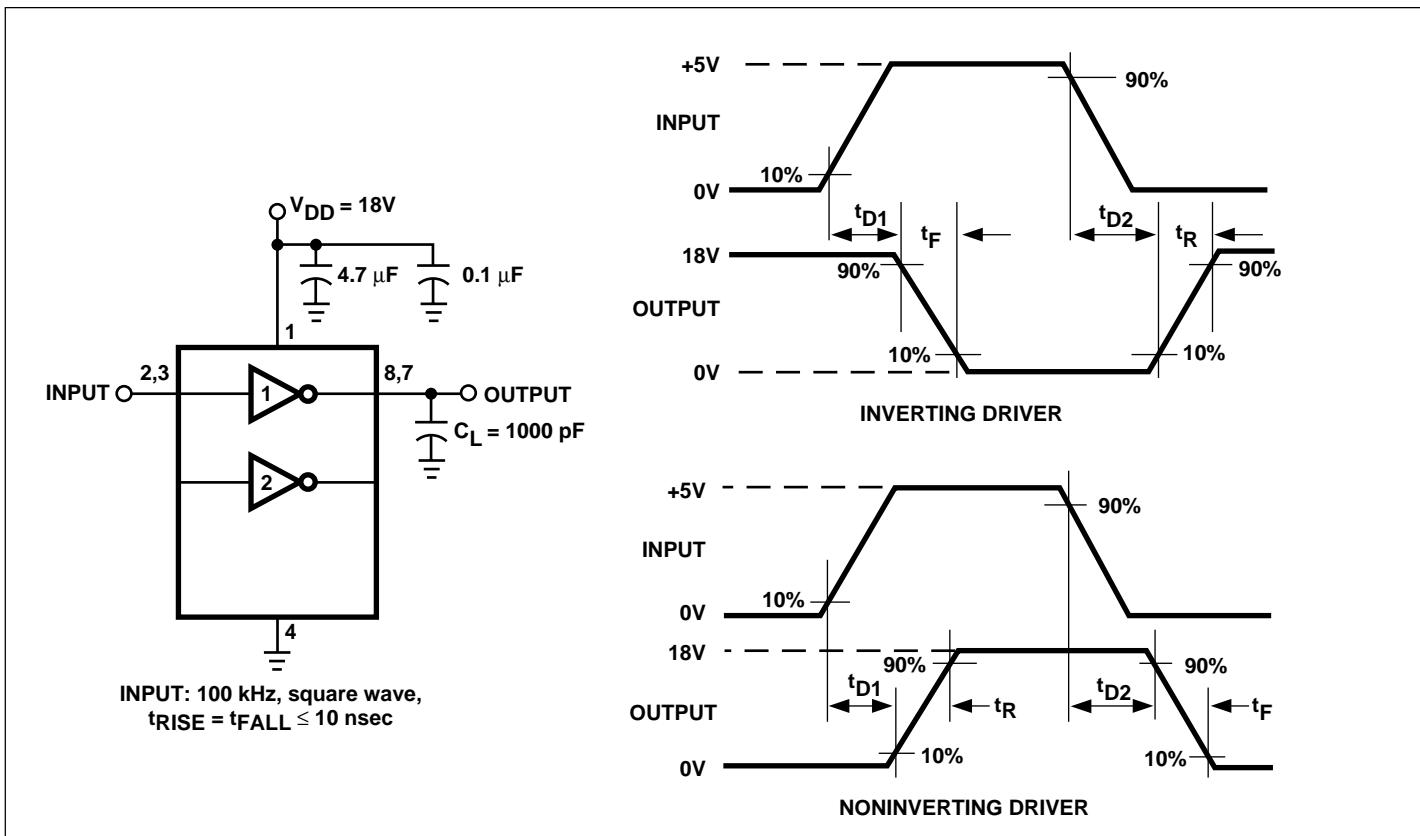
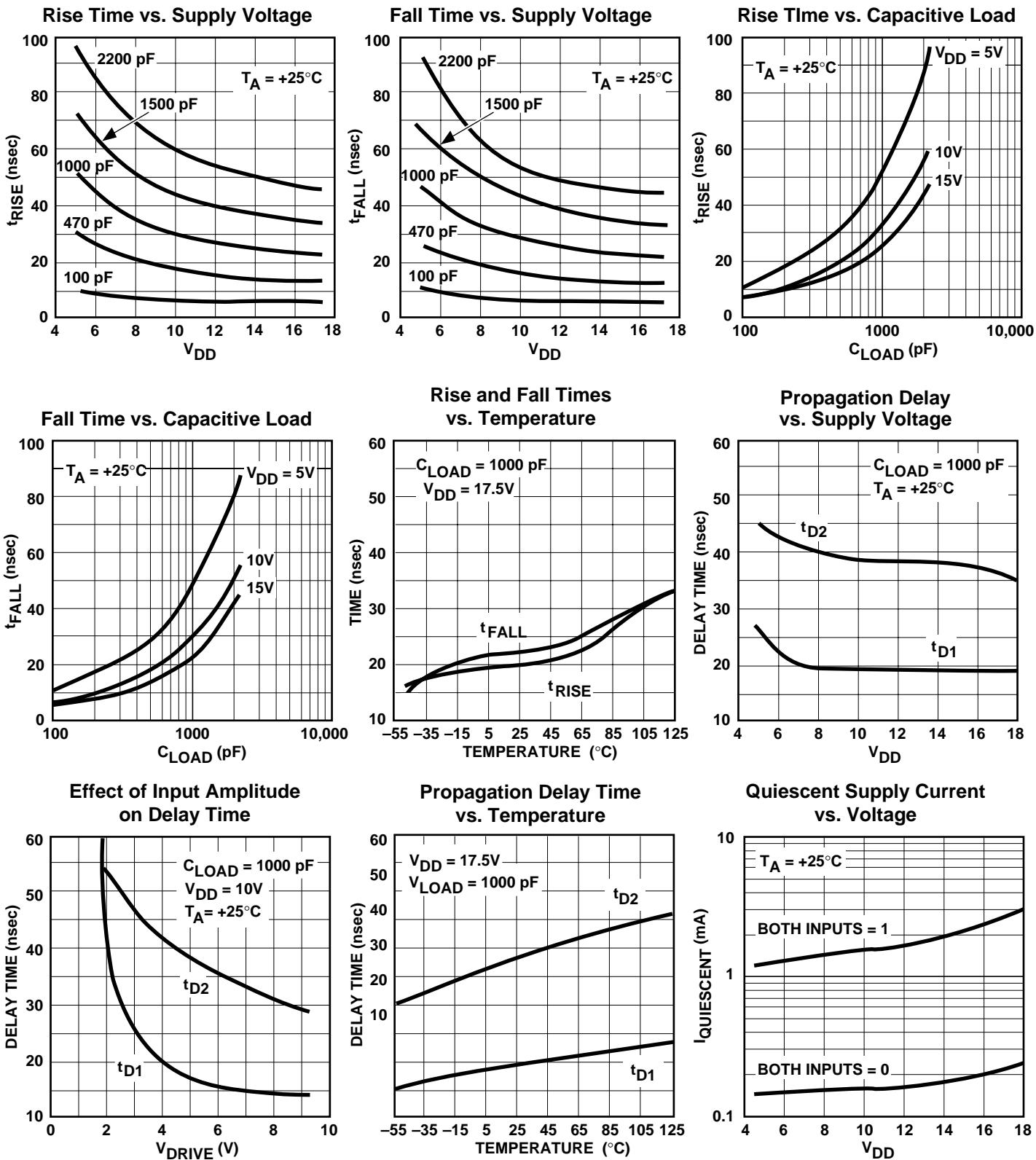


Figure 1. Switching Time Test Circuit

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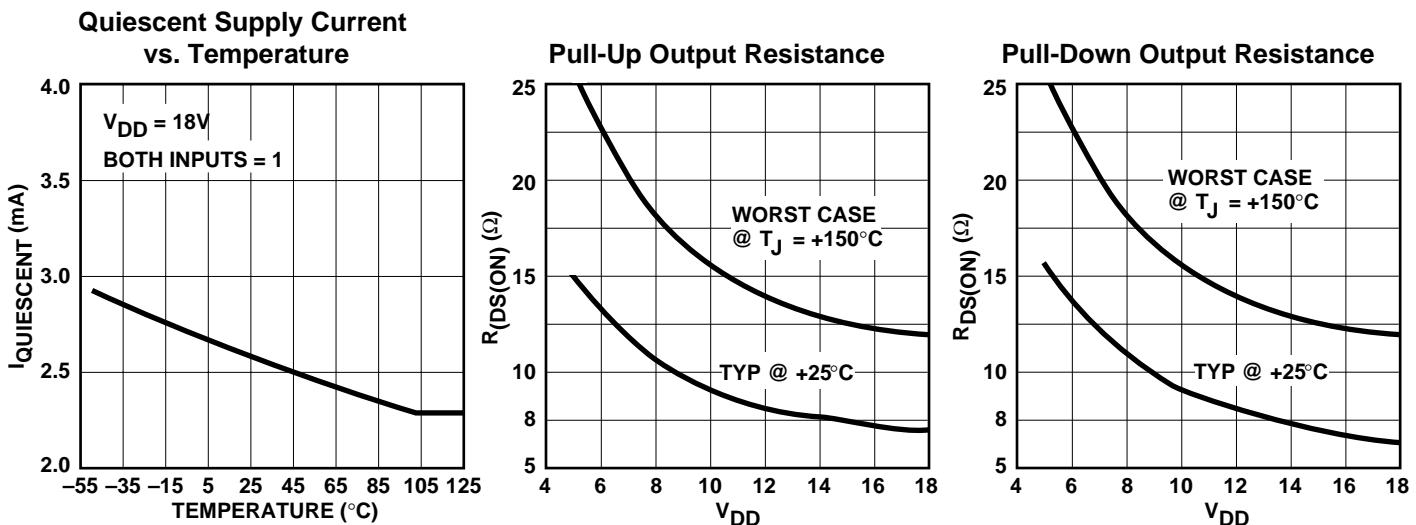
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TYPICAL CHARACTERISTICS

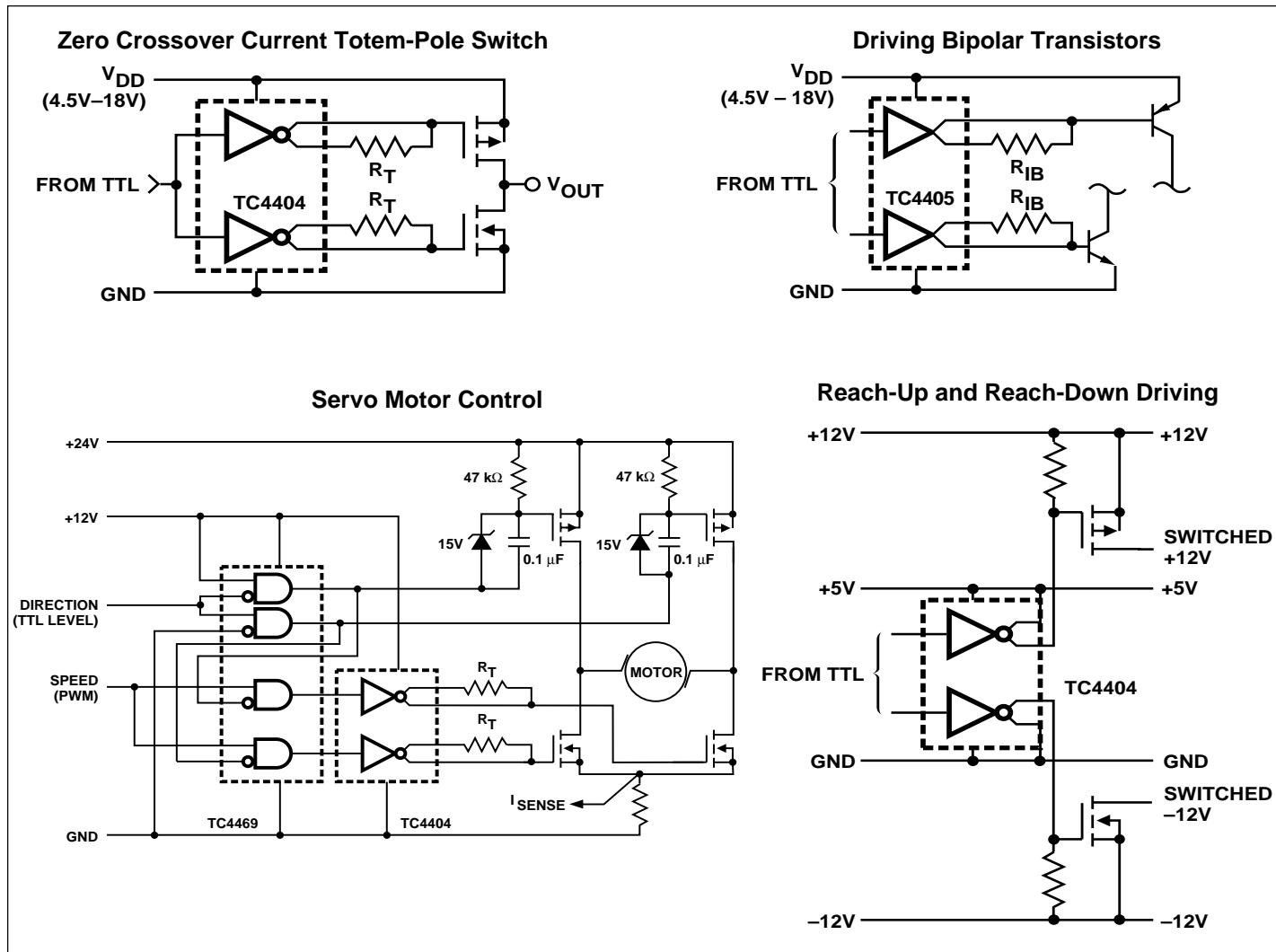


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TYPICAL CHARACTERISTICS (Cont.)



TYPICAL APPLICATIONS

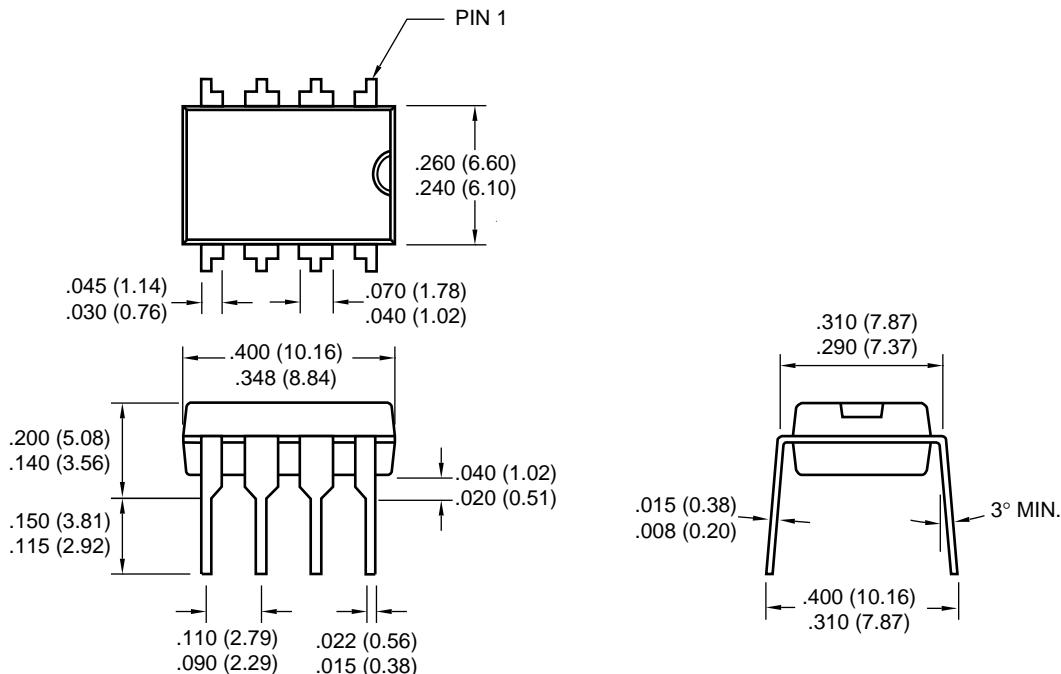


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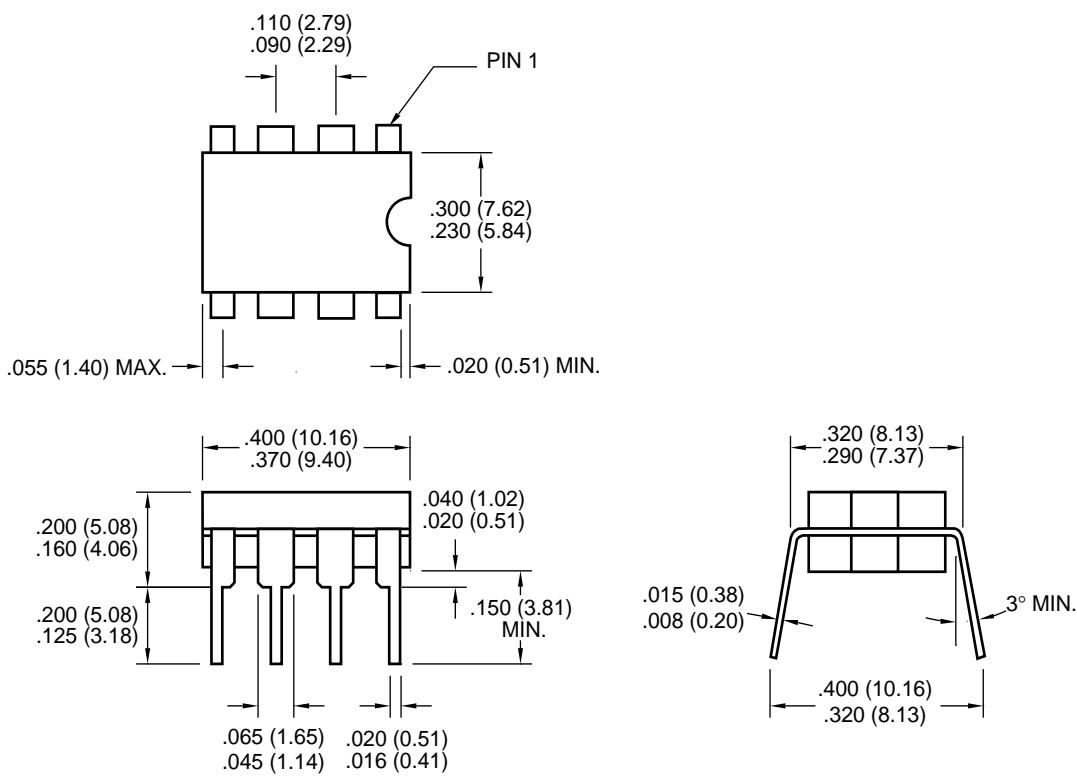
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PACKAGE DIMENSIONS

8-Pin Plastic DIP



8-Pin CerDIP



Dimensions: inches (mm)

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