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Product Brief

TC358860 Display Bridge

Highlights

- Display bridge performs protocol translation from embedded DisplayPort™ to MIPI® Display Serial Interface (DSI).
- Embedded DisplayPort receiver features VESA® Embedded DisplayPort (eDP™) 1.4 standard that supports multiple bitrates at 1.62, 2.16, 2.43, 2.7, 3.24, 4.32, 4.86, or 5.4 Gbps per lane; and is configurable to one, two or four lanes on the Main Link.
- Supports dual DSI transmitter ports based on MIPI DSI 1.10 with data rates of up to 1 Gbps per lane, enabling a total bandwidth of 8 Gbps.
- Supports high-resolution MIPI DSI panels up to Ultra HD (4K/2K) 3840 x 2160.
- Supports a 2:1 compression engine to enable 60 frames per second (fps) refresh rate for 4K streams.
- Applicable to products such as tablets, phablets and handheld gaming.

Description

The Toshiba TC358860 display bridge enables 4K Ultra HD (3840 x 2160) tablet/phablet with a thin MIPI display and low-power consumption. It is optimized for high-end handheld devices using a Host Processor with laptop computing power and embedded DisplayPort (eDP) interface. The TC358860 functions as a protocol bridge enabling the video stream from the Host Processor eDP link to drive a high-resolution and power-efficient DSI panel. This display bridge has an eDP receiver based on VESA eDP version 1.4, with 4 configurable lanes on the Main Link. The eDP receiver supports multiple bitrates with a maximum bitrate of 5.4 Gbps per lane, to receive up to 17.28 Gbps of video stream. The TC358860 has dual DSI port transmitters that can support eight DSI lanes with data rates of 1 Gbps per lane, for a maximum total bandwidth of 8 Gbps.

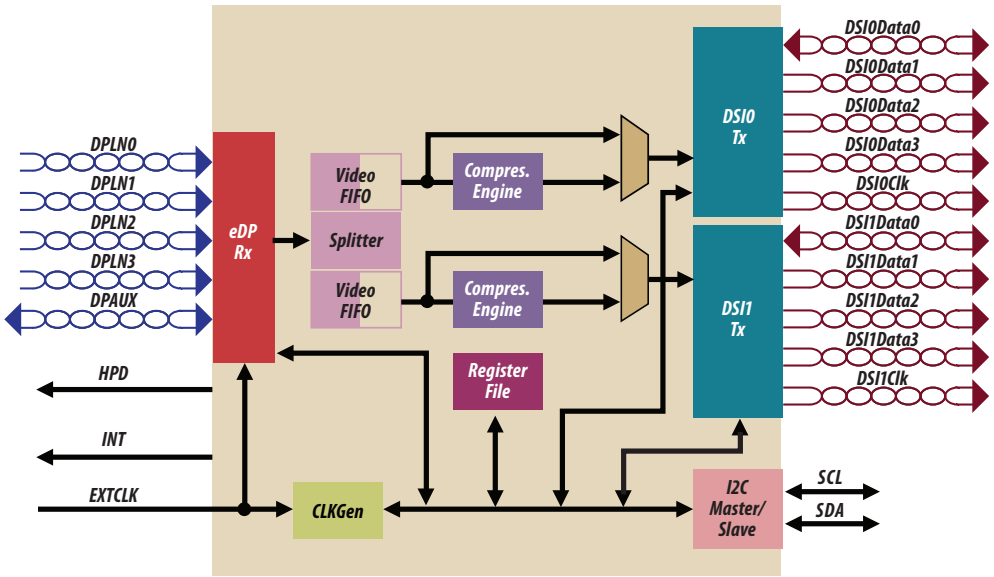
Since MIPI displays are low-power and are available with chip-on-glass technology for high-resolution Ultra HD 4K, MIPI panels are migrating from smartphone applications to phablet/tablets as well as handheld gaming devices. The Toshiba TC358860 display bridge can support MIPI displays with resolutions up to 4K (Ultra HD) at 24 bits per pixel, with a refresh rate of 60 fps using 2 to 1 compression. The corresponding decompression engine is expected in the DSI panel to support 4K at 60 fps. Lower than 4K resolutions such as WQXGA (2560 x 1600) can be realized without enabling the compression engine of the bridge.

The TC358860 is a 65-pin device, in a small package size of 5 mm x 5 mm, 0.50 mm ball pitch designed for portable products.

Features

- TC358860 follows the following standards:
  - MIPI Alliance Specification for Display Serial Interface (DSI) version 1.1, Nov 22 2011
  - MIPI Alliance Specification for D-PHY Version 1.1, Nov. 7, 2011
  - VESA DisplayPort Standard version 1.2a, May 23, 2012.
  - VESA Embedded DisplayPort Standard version 1.4, Feb. 28, 2013
- eDP Sink (Receiver)
  - Bitrates @ 1.62, 2.16, 2.43, 2.7, 3.24, 4.32, 4.86 or 5.4 Gbps, voltage swing @ 0.2 to 1.2V, pre-emphasis level @ 3.5 dB.

TC358860 Block Diagram



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- There are four lanes available in the eDP Main Link, which can operate in a 1-, 2- or 4 lane configuration.
- Supports Single-Stream Transport (SST), not Multi-Stream Transport (MST).
- Capable of Full and Fast Link Training.
- AUX channel with nominal bit rate at 1 Mbps.
- Supports RGB666 and RGB888 video input data formats.
- Alternate Scrambler Seed Reset (ASSR) is used for content protection.
- Supports REFCLK from 25 MHz to 40 MHz with 1.0 MHz step.

• DSI Transmitter
- Dual 4-Data Lane DSI Links with bi-direction support at Data Lane 0. Each link can be used in a 1-, 2-, 3- or 4-data lane configuration. Maximum speed is 1.0 Gbps/lane.
- Supports RGB666 and RGB888 video input data formats.
- Dual links with left-right split: DSI0 carries the left half data of eDP Rx video stream and DSI1 carries the right half data.
- Provides a path for an eDP host/transmitter to control the TC358860 and the attached panel.
- Built in color bar generator to verify the Dual DSI links without eDP input.

• Video function
- Compression engine: 2 to 1 compression can be enabled or disabled to support 4K stream at 60 fps refresh rate.

• I^2C Slave Port
- Support for normal (100 kHz) and fast (400 kHz or 1 MHz, if SysClk is running at 25 MHz) modes.
- External I^2C master can access TC358860 internal and DPCD registers and read/write DSI panel registers (via DSI link).

• Power Supply

– IPI D-PHY	1.2V
– Core	1.1V
– eDP-PHY	1.8V
– I/O	1.8V or 3.3V (all IO pins must be the same power level)
– HPD Output Pad	1.8V or 3.3V

• Package
- TC358860XBG: 65-pin, 0.5 mm ball pitch, 5 x 5 mm2 package