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Product Brief — TC358774/5 Display Bridge (MIPI® DSI to LVDS)

Highlights

- Display bridge for connectivity of LVDS panels to the Baseband or Application Processors with a Mobile Industry Processor Interface (MIPI) Display Serial Interface.

- Solutions are based on the latest versions of the industry-standard MIPI DSI 1.01 interface to ensure high-speed data rates of up to 1 Gbps per lane. It can be configured to support 1, 2, 3 or up to four DSI lanes.

- LVDS link transmitter supports maximum clock frequency of 135 MHz per link, and total bandwidth of 3.24 Gbps per link.

- The TC358774 supports panels up to 1600 x 1200, with 24 bits per pixel. The TC358775 supports WUXGA 1920 x 1200, 24-bit/pixel or QXGA 2048 x 1536, 18-bit/pixel panel resolutions.

- Applicable to a range of handheld product platforms such as tablets, laptops, thin notebooks, and eBooks.

Description

The Toshiba TC358774/5 display bridge is optimized for handheld devices using a Host processor with MIPI DSI (Display Serial Interface) connectivity. The TC358774/5 functions as a protocol bridge enabling the video data stream from the Host processor DSI link to drive LVDS display panels. The TC358774/5 bridge can be configured to have up to a 4-lane MIPI DSI with data rates up to 1 Gbps per lane, for maximum total bandwidth of 4 Gbps. The TC358774 bridge has a single-link LVDS transmitter and can support up to UXGA 1600 x 1200, 24-bit/pixel panel resolution. The TC358775 bridge has a dual-link LVDS transmitter and can support up to WUXGA 1920 x 1200, 24-bit/pixel or QXGA 2048 x 1536, 18-bit/pixel panel resolutions. A video FIFO is used to buffer the burst video data received from the DSI link before transmitting out from the LVDS link.

The TC358774/5 is a follow on to the existing Toshiba's similar devices TC358764/5 with improvements such as higher bandwidth on both the DSI side and the LVDS side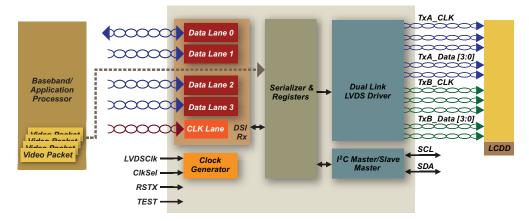, and lower power consumption as LVDS TX block operates at 1.8V instead of 3.3V. Additional management of power consumption via a STBY pin is added.

The TC358774XBG is a 49-pin device and is pin compatible with TC358764XBG. The TC358775XBG is a 64-pin device and is pin compatible with TC358765XBG. Both devices have 0.65mm ball pitch suitable for lower cost printed circuit boards.

Features

- MIPI standard implemented
  - MIPI DSI version 1.01, Feb 2008
  - MIPI D-PHY version 0.9, Oct 2007
  - MIPI DCS version 1.02, Dec 2008
- DSI Receiver
  - MIPI DSI-RX Data 4-lane, CLK 1-lane with data rates up to 1 Gbps/lane
  - Video input frame sizes: Up to UXGA 1600 x 1200, 24-bit/pixel on single-link LVDS; Up to WUXGA 1920 x 1200, 24-bit/pixel or QXGA 2048 x 1536, 18-bit/pixel on dual link LVDS
  - Video input data formats: RGB888, RGB666 and RGB565

Block Diagram

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- LVDS Transmitter
  - Supports single-link or dual-link LVDS
  - Maximum pixel clock frequency of 135 MHz per link, total bandwidth of 3.24 Gbps per link. If dual link is used, the total bandwidth is limited by the maximum DSI bandwidth of 4Gpbs
  - Supports display up to 1600 x 1200 24 bit/pixel resolution for single-link, or up to 1920 x 1200 24-bit resolutions for dual-link
  - Supports the following pixel formats:
    - RGB666 18-bits per pixel
    - RGB565 16-bits per pixel
    - RGB666 loosely packed 24-bits per pixel
    - RGB888 24-bits per pixel
  - Supports two power saving states
    - Sleep state when receiving DSI ULPS signaling
    - Standby state entered by STBY pin assertion
- Peripheral control ports
  - I^2C Master/Slave ports with data rates up to 400 KHz. External I^2C master can access TC358774/5 internal registers via this port.

- Clock Source
  - LVDS pixel clock source is either from external clock EXTCLK or derived from DSICLK
  - Built-in PLL is used to generate the high speed LVDS serializing clock
- Power supply
  - CORE: 1.2V
  - MIPI DSI D-PHY: 1.2V
  - LVDS PHY: 1.8V
  - I/O: 1.8V to 3.3V
- Package
  - TC358775: P-TFBGA 64-pin, 6 mm x 6 mm, 1.2 mm height, 0.65 mm ball pitch
  - TC358774: P-TFBGA 49-pin, 5 mm x 5 mm, 1.2 mm height, 0.65 mm ball pitch
- Power supply:
  - Analog = 2.6 to 3.0V
  - Digital = 1.7 to 1.9V
  - I/O = 1.7 to 3.0V
- Operating temperature: –30 to +85°C
- Storage temperature: –40 to +85°C

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