

## 300mA CMOS LDO with Shutdown, Bypass and Independent Delayed Reset Function

### FEATURES

- LDO with Integrated Microprocessor Reset Monitor Functionality
- Extremely Low Supply Current (80 $\mu$ A typ.) for Longer Battery Life!
- Stable with Any Type of Capacitor
- Very Low Dropout Voltage
- 10 $\mu$ sec (typ.) Wake Up Time from  $\overline{\text{SHDN}}$
- Guaranteed 300mA Output Current
- Standard or Custom Output and Detected Voltages
- Power-Saving Shutdown Mode
- Bypass Input for Ultra-Quiet Operation
- Separate Input and Detected Voltage
- 140msec Guaranteed Minimum  $\overline{\text{RESET}}$  Output Duration
- Space-Saving MSOP Package

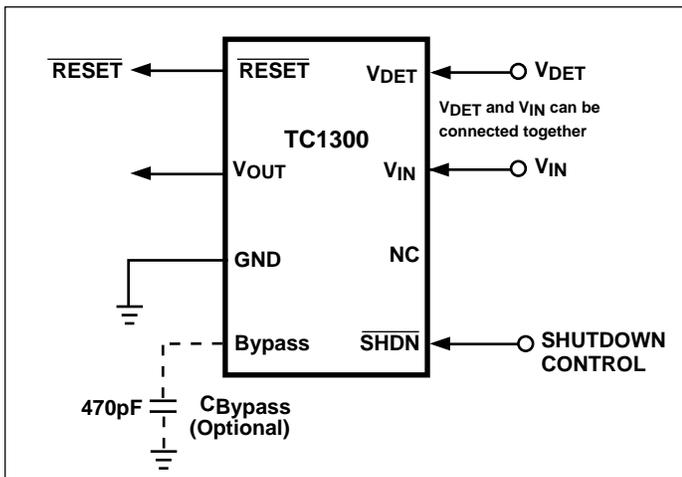
### APPLICATIONS

- Battery-Operated Systems
- Portable Computers
- Medical Instruments
- Pagers
- Cellular / GSM / PHS Phones

### RELATED LITERATURE

- Application Notes: 41, 47 and 66
- Article: "TelCom's CMOS LDOs Exhibit Excellent Stability While Offering the Advantages of Low-Value Ceramic Capacitors"

### TYPICAL APPLICATION



### GENERAL DESCRIPTION

The TC1300 combines a Low Dropout Regulator and a Microprocessor Reset Monitor in a space-saving 8-Pin MSOP package. Total supply current is 80 $\mu$ A (typical), 20 to 60 times lower than in bipolar regulators.

The TC1300 has an extremely precise output with a typical accuracy of  $\pm 0.5\%$ . Other key features include ultra low noise operation, very low dropout voltage and internal feed-forward compensation for fast response to step changes in load. The TC1300 incorporates both over-temperature and over-current protection. When the shutdown control ( $\overline{\text{SHDN}}$ ) is low, the regulator output voltage falls to zero,  $\overline{\text{RESET}}$  output remains valid and supply current is reduced to 30 $\mu$ A (typical). The TC1300 is stable with an output capacitor of only 1 $\mu$ F and has a maximum output current of 300mA.

An active low  $\overline{\text{RESET}}$  is asserted when the detected voltage ( $V_{\text{DET}}$ ) falls below the reset voltage threshold. The  $\overline{\text{RESET}}$  output remains low for 300msec (typical) after  $V_{\text{DET}}$  rises above reset threshold. The TC1300 also has a fast wake up response time (10 $\mu$ sec typically) when released from shutdown.

### ORDERING INFORMATION

Part Number	Package	Junction Temp. Range
TC1300R-xxVUA	8-Pin MSOP	-40°C to +125°C

NOTE: The "R" denotes the suffix for the 2.63V  $V_{\text{DET}}$  threshold

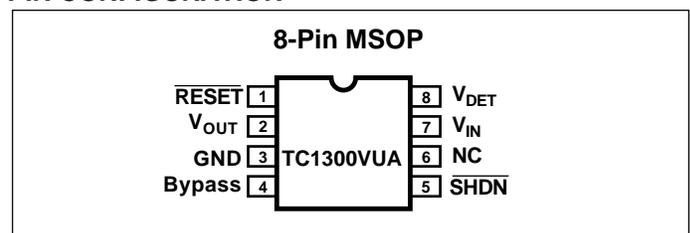
#### Available Output Voltages:

2.5, 2.8, 2.85, 3.0, 3.3

xx indicates output voltages

Other output voltages and threshold voltages are available. Please contact Microchip Technology Inc. for details.

### PIN CONFIGURATION



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## TC1300

### ABSOLUTE MAXIMUM RATINGS\*

Input Voltage ..... 6.5V  
 Output Voltage ..... ( $V_{SS} - 0.3$ ) to ( $V_{IN} + 0.3$ )  
 Power Dissipation ..... Internally Limited (Note 6)  
 Operating Temperature .....  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$

Storage Temperature .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
 Maximum Voltage on Any Pin .....  $V_{IN} + 0.3\text{V}$  to  $-0.3\text{V}$   
 Lead Temperature (Soldering, 10 Sec.) .....  $+300^{\circ}\text{C}$   
 \*Absolute Maximum Ratings indicate device operation limits beyond damage may occur. Device operation beyond the limits listed in is not recommended.

**ELECTRICAL CHARACTERISTICS:**  $V_{IN} = V_{OUT} + 1\text{V}$ ,  $I_L = 0.1\text{mA}$ ,  $C_L = 3.3\mu\text{F}$ ,  $\text{SHDN} > V_{IH}$ ,  $T_A = 25^{\circ}\text{C}$ , unless otherwise noted.  
**BOLDFACE** type specifications apply for junction temperatures of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{IN}$	Input Operating Voltage		—	—	<b>6.0</b>	V
$I_{OUTMAX}$	Maximum Output Current		<b>300</b>	—	—	mA
$V_{OUT}$	Output Voltage	Note 1	— <b><math>V_R - 2.5\%</math></b>	$V_R \pm 0.5\%$	— <b><math>V_R + 2.5\%</math></b>	V
$\Delta V_{OUT}/\Delta T$	$V_{OUT}$ Temperature Coefficient	Note 2	—	<b>25</b>	—	ppm/ $^{\circ}\text{C}$
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$(V_R + 1\text{V}) \leq V_{IN} \leq 6\text{V}$	—	0.02	<b>0.35</b>	%
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	$I_L = 0.1\text{mA}$ to $I_{OUTMAX}$ (Note 3)	—	0.5	<b>2.0</b>	%
$V_{IN} - V_{OUT}$	Dropout Voltage (Note 4)	$I_L = 0.1\text{mA}$ $I_L = 100\text{mA}$ $I_L = 300\text{mA}$	—	1 70 210	<b>30</b> <b>130</b> <b>390</b>	mV
$I_{SS1}$	Supply Current	$\text{SHDN} = V_{IH}$	—	80	<b>160</b>	$\mu\text{A}$
$I_{SS2}$	Shutdown Supply Current	$\text{SHDN} = 0\text{V}$	—	30	<b>60</b>	$\mu\text{A}$
PSRR	Power Supply Rejection Ratio	$f \leq 1\text{kHz}$	—	60	—	dB
$I_{OUTSC}$	Output Short Circuit Current	$V_{OUT} = 0\text{V}$	—	800	1200	mA
$\Delta V_{OUT}/\Delta P_D$	Thermal Regulation	Note 5	—	0.04	—	%/W
eN	Output Noise	$f = 1\text{kHz}$ , $C_{OUT} = 1\mu\text{F}$ , $R_{LOAD} = 50\Omega$	—	900	—	nV/ $\sqrt{\text{Hz}}$
$t_{WK}$	Wake Up Time (from Shutdown Mode)	$V_{IN} = 5\text{V}$ $C_{IN} = 1\mu\text{F}$ , $C_{OUT} = 4.7\mu\text{F}$ $I_L = 30\text{mA}$ , (See Fig. 2)	—	10	20	$\mu\text{sec}$
$t_S$	Settling Time (from Shutdown Mode)	$V_{IN} = 5\text{V}$ $C_{IN} = 1\mu\text{F}$ , $C_{OUT} = 4.7\mu\text{F}$ $I_L = 30\text{mA}$ , (See Fig. 2)	—	50	—	$\mu\text{sec}$
$T_{SD}$	Thermal Shutdown Die Temperature		—	150	—	$^{\circ}\text{C}$
$T_{HYS}$	Thermal Shutdown Hysteresis		—	10	—	$^{\circ}\text{C}$

### SHDN Input

$V_{IH}$	$\overline{\text{SHDN}}$ Input High Threshold	<b>45</b>	—	—	% $V_{IN}$
$V_{IL}$	$\overline{\text{SHDN}}$ Input Low Threshold	—	—	<b>15</b>	% $V_{IN}$

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TC1300

## ELECTRICAL CHARACTERISTICS: (CONT.)

**ELECTRICAL CHARACTERISTICS:**  $V_{IN} = V_{OUT} + 1V$ ,  $I_L = 0.1mA$ ,  $C_L = 3.3\mu F$ ,  $SHDN > V_{IH}$ ,  $T_A = 25^\circ C$ , unless otherwise noted. **BOLDFACE** type specifications apply for junction temperatures of  $-40^\circ C$  to  $+125^\circ C$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>RESET Output</b>						
$V_{DET}$	$V_{DET}$ Voltage Range	$T_A = 0^\circ C$ to $+70^\circ C$	1.0	—	6.0	V
		$T_A = -40^\circ C$ to $+125^\circ C$	1.2	—	6.0	
$V_{TH}$	Reset Threshold	$T_A = +25^\circ C$	2.59	2.63	2.66	V
		$T_A = -40^\circ C$ to $+125^\circ C$	2.55	—	2.70	
	Reset Threshold Tempco		—	30	—	ppm/ $^\circ C$
	$V_{DET}$ to Reset Delay	$V_{DET} = V_{TH}$ to $(V_{TH} - 100mV)$	—	160	—	$\mu sec$
	Reset Active Timeout Period		140	300	560	msec
$V_{OL}$	$\overline{RESET}$ Output Voltage Low	$V_{DET} = V_{TH}$ min, $I_{SINK} = 1.2mA$	—	—	0.3	V
$V_{OH}$	$\overline{RESET}$ Output Voltage High	$V_{DET} > V_{TH}$ max, $I_{SOURCE} = 500\mu A$	$0.8 V_{DET}$	—	—	V

- NOTES:**
- $V_R$  is the regulator output voltage setting.
  - $T_C V_{OUT} = \frac{(V_{OUTMAX} - V_{OUTMIN}) \times 10^6}{V_{OUT} \times \Delta T}$
  - Regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 0.1mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.
  - Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at a 1V differential.
  - Thermal Regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to  $I_{LMAX}$  at  $V_{IN} = 6V$  for  $t = 10msec$ .
  - The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature, and the thermal resistance from junction-to-air (i.e.  $T_A$ ,  $T_J$ ,  $\theta_{JA}$ ). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown. Please see **Thermal Considerations** section of this data sheet for more details.

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## TC1300

### DETAILED DESCRIPTION

The TC1300 is a combination of a fixed output, low drop-out regulator and a microprocessor monitor. Unlike bipolar regulators, the TC1300 supply current does not increase with load current. In addition,  $V_{OUT}$  remains stable and within regulation at very low load currents (an important consideration in RTC and CMOS RAM battery back-up applications) as well as with any type of capacitor (see \* below). TC1300 pin functions are detailed below:

### PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ output remains low while $V_{DET}$ is below the reset voltage threshold, and for 300msec after $V_{DET}$ rises above reset threshold.
2	$V_{OUT}$	Regulated Voltage Output
3	GND	Ground Terminal
4	Bypass	Reference Bypass Input. Connecting a 470pF to this input further reduces output noise.
5	$\overline{\text{SHDN}}$	Shutdown Control Input. The regulator is fully enabled when a logic high is applied to this input. The regulator enters shutdown when a logic low is applied to this input. During shutdown, regulator output voltage falls to zero, $\overline{\text{RESET}}$ output remains valid and supply current is reduced to 30 $\mu\text{A}$ (typ.).
6	NC	No connect
7	$V_{IN}$	Power Supply Input
8	$V_{DET}$	Detected Input Voltage. $V_{DET}$ and $V_{IN}$ can be connected together.

Figure 1 shows a typical application circuit. The regulator is enabled any time the shutdown input ( $\overline{\text{SHDN}}$ ) is above  $V_{IH}$ , and shutdown (disabled) when  $\overline{\text{SHDN}}$  is at or below  $V_{IL}$ .  $\overline{\text{SHDN}}$  may be controlled by a CMOS logic gate, or I/O port of a microcontroller. If the  $\overline{\text{SHDN}}$  input is not required, it should be connected directly to the input supply. While in shutdown, supply current decreases to 30 $\mu\text{A}$  (typical),  $V_{OUT}$  falls to zero and  $\overline{\text{RESET}}$  remains valid.

### RESET Output

The  $\overline{\text{RESET}}$  output is driven active low within 160  $\mu\text{sec}$  of  $V_{DET}$  falling through the reset voltage threshold.  $\overline{\text{RESET}}$  is maintained active for a minimum of 140msec after  $V_{DET}$  rises above the reset threshold. The TC1300 has an active-low  $\overline{\text{RESET}}$  output. The output of the TC1300 is guaranteed valid down to  $V_{DET} = 1\text{V}$  and is optimized to reject fast transient glitches on the  $V_{DET}$  line.

\* Article: "TelCom's CMOS LDOs Exhibit Excellent Stability While Offering the Advantage of Low-Value Ceramic Capacitors"

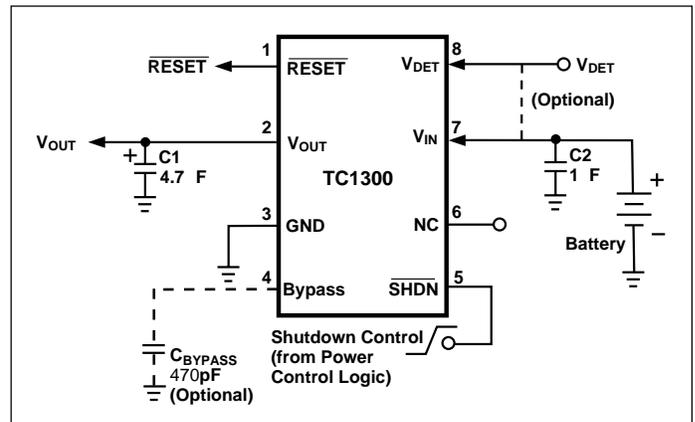


Figure 1: Typical Application Circuit

### Output Capacitor

A 1 $\mu\text{F}$  (min) capacitor from  $V_{OUT}$  to ground is required. A 1 $\mu\text{F}$  capacitor should also be connected from  $V_{IN}$  to GND if there is more than 10 inches of wire between the regulator and the AC filter capacitor, or if a battery is used as the power source. Aluminum electrolytic, ceramic or tantalum capacitor types can be used (since many aluminum electrolytic capacitors freeze at approximately  $-30^{\circ}\text{C}$ , solid tantalums are recommended for applications operating below  $-25^{\circ}\text{C}$ ). When operating from sources other than batteries, supply-noise rejection and transient response can be improved by increasing the value of the input and output capacitors and employing passive filtering techniques.

### Bypass Input (optional)

A 470pF capacitor connected from the Bypass input to ground reduces noise present on the internal reference, which in turn significantly reduces output noise. This input may be left unconnected. Larger capacitor values may be used, but results in a longer time period to rated output voltage when power is initially applied.

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## Turn On Response

The turn on response is defined as two separate response categories, **Wake Up Time ( $t_{WK}$ )** and **Settling Time ( $t_s$ )**.

The TC1300 has a fast Wake Up Time (10 $\mu$ sec typical) when released from shutdown. See Figure 2 for the **Wake Up Time** designated as  $t_{WK}$ . The **Wake Up Time** is defined as the time it takes for the output to rise to 2% of the  $V_{OUT}$  value after being released from shutdown.

The total turn on response is defined as the **Settling Time ( $t_s$ )**, see Figure 2. **Settling Time** (inclusive with  $t_{WK}$ ) is defined as the condition when the output is within 2% of its fully enabled value (50 $\mu$ sec typical) when released from shutdown. The settling time of the output voltage is dependent on load conditions and output capacitance on  $V_{OUT}$  (RC response).

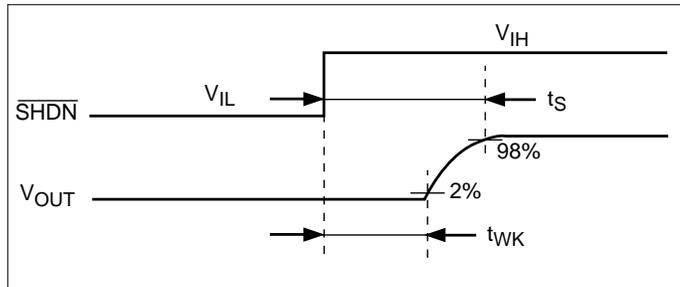


Figure 2: Wake Up Response Time

## Thermal Considerations

### Thermal Shutdown

Integrated thermal protection circuitry shuts the regulator off when die temperature exceeds 150°C. The regulator remains off until the die temperature drops to approximately 140°C.

### Power Dissipation

The amount of power the regulator dissipates is primarily a function of input and output voltage, and output current. The following equation is used to calculate worst case *actual* power dissipation:

$$P_D \approx (V_{INMAX} - V_{OUTMIN})I_{LOADMAX}$$

Where:  $P_D$  = worst case actual power dissipation  
 $V_{INMAX}$  = maximum voltage on  $V_{IN}$   
 $V_{OUTMIN}$  = minimum regulator output voltage  
 $I_{LOADMAX}$  = maximum output (load) current

Equation 1.

The maximum **allowable** power dissipation (Equation 2) is a function of the maximum ambient temperature ( $T_{AMAX}$ ), the maximum allowable die temperature (125°C), and the thermal resistance from junction-to-air ( $\theta_{JA}$ ). The

SOIC-8 package has a  $\theta_{JA}$  of approximately **160°C/Watt**, while the MSOP-8 package has a  $\theta_{JA}$  of approximately **200°C/Watt**; both when mounted on a single layer FR4 dielectric copper clad PC board.

$$P_{DMAX} = \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}}$$

Where all terms are previously defined.

Equation 2.

Equation 1 can be used in conjunction with Equation 2 to ensure regulator thermal operation is within limits. For example:

GIVEN:  $V_{INMAX} = 4.0V \pm 10\%$   
 $V_{OUTMIN} = 3.3V \pm 2.5\%$   
 $I_{LOADMAX} = 200mA$   
 $T_{JMAX} = 125^\circ C$   
 $T_{AMAX} = 55^\circ C$   
 $\theta_{JA} = 200^\circ C/W$   
 MSOP-8 Package

FIND: 1. Actual power dissipation

Actual power dissipation:

$$\begin{aligned} P_D &\approx (V_{INMAX} - V_{OUTMIN})I_{LOADMAX} \\ &= [(4.0 \times 1.1) - (3.03 \times .975)]200 \times 10^{-3} \\ &= \underline{236.5mW} \end{aligned}$$

Maximum allowable power dissipation:

$$\begin{aligned} P_D &\approx \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}} \\ &= \frac{(125 - 55)}{200} \\ &= \underline{350mW} \end{aligned}$$

In this example, the TC1300 dissipates a maximum of only 236.5mW; far below the allowable limit of 350mW. In a similar manner, Equation 1 and Equation 2 can be used to calculate maximum current and/or input voltage limits. For example, the maximum allowable  $V_{IN}$  is found by substituting the maximum allowable power dissipation of 350mW into Equation 1, from which  $V_{INMAX} = 4.1V$ .

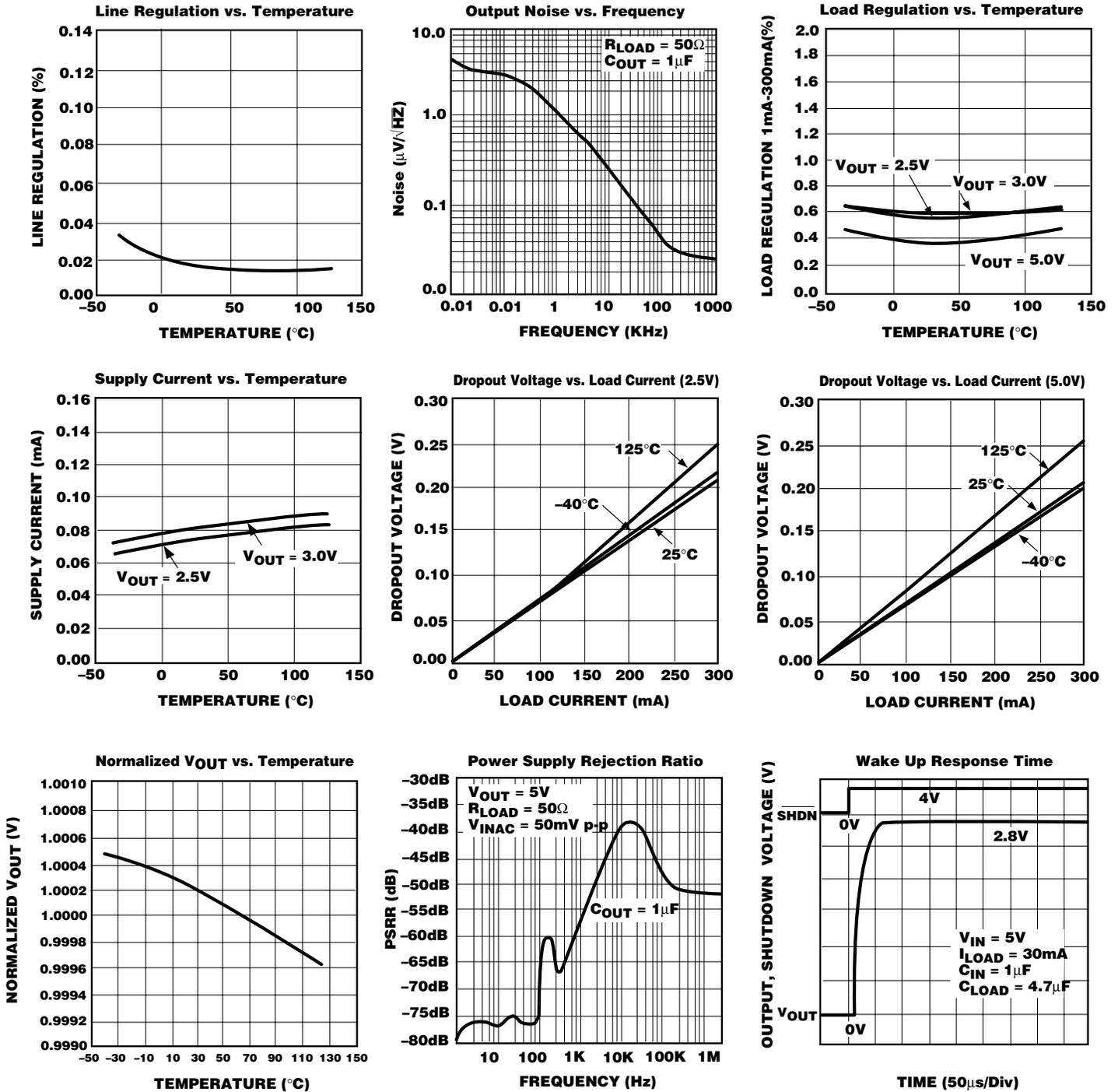
### Layout Considerations

The primary path of heat conduction out of the package is via the package leads. Therefore, layouts having a ground plane, wide traces at the pads, and wide power supply bus lines combine to lower  $\theta_{JA}$  and, therefore, increase the maximum allowable power dissipation limit.

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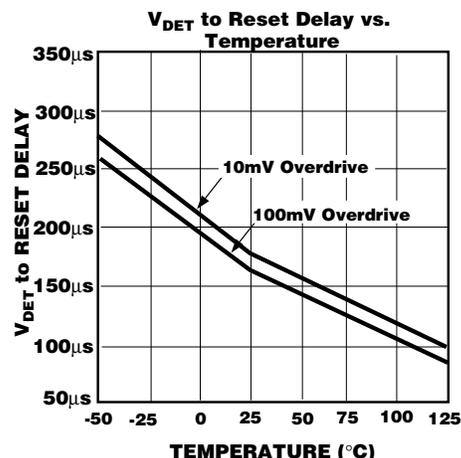
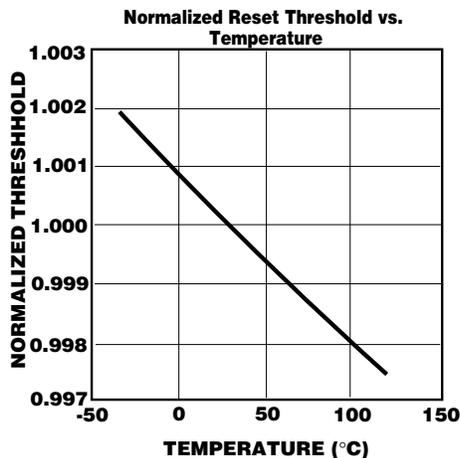
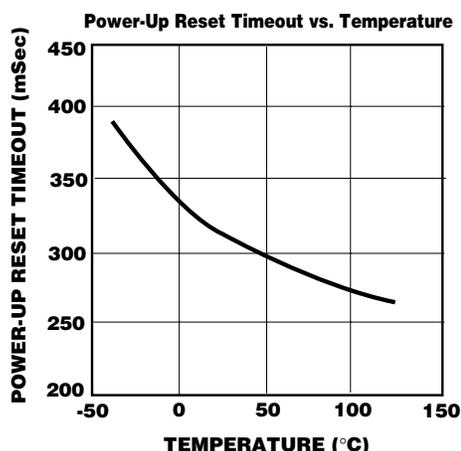
## TYPICAL CHARACTERISTICS



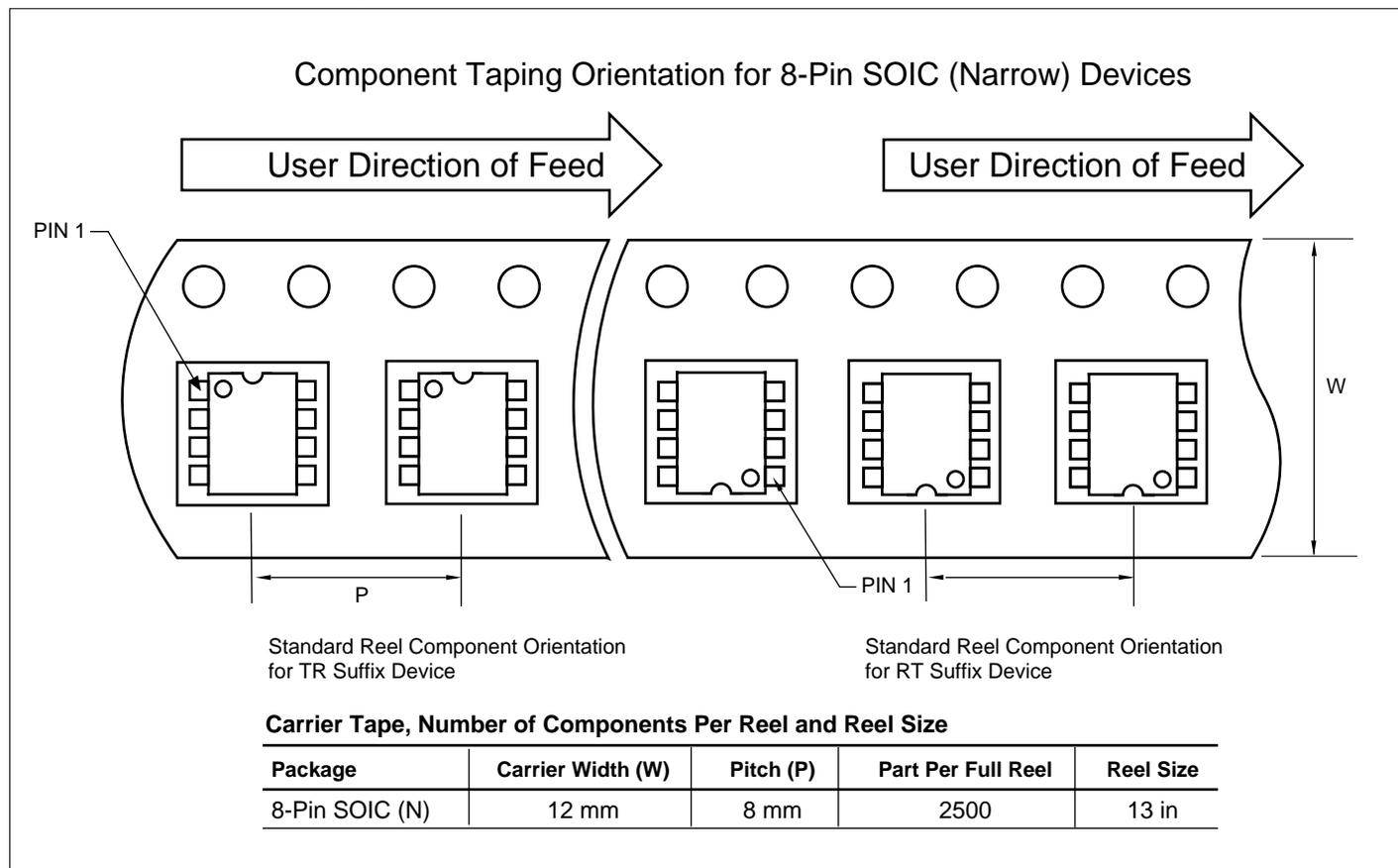
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## TYPICAL CHARACTERISTICS



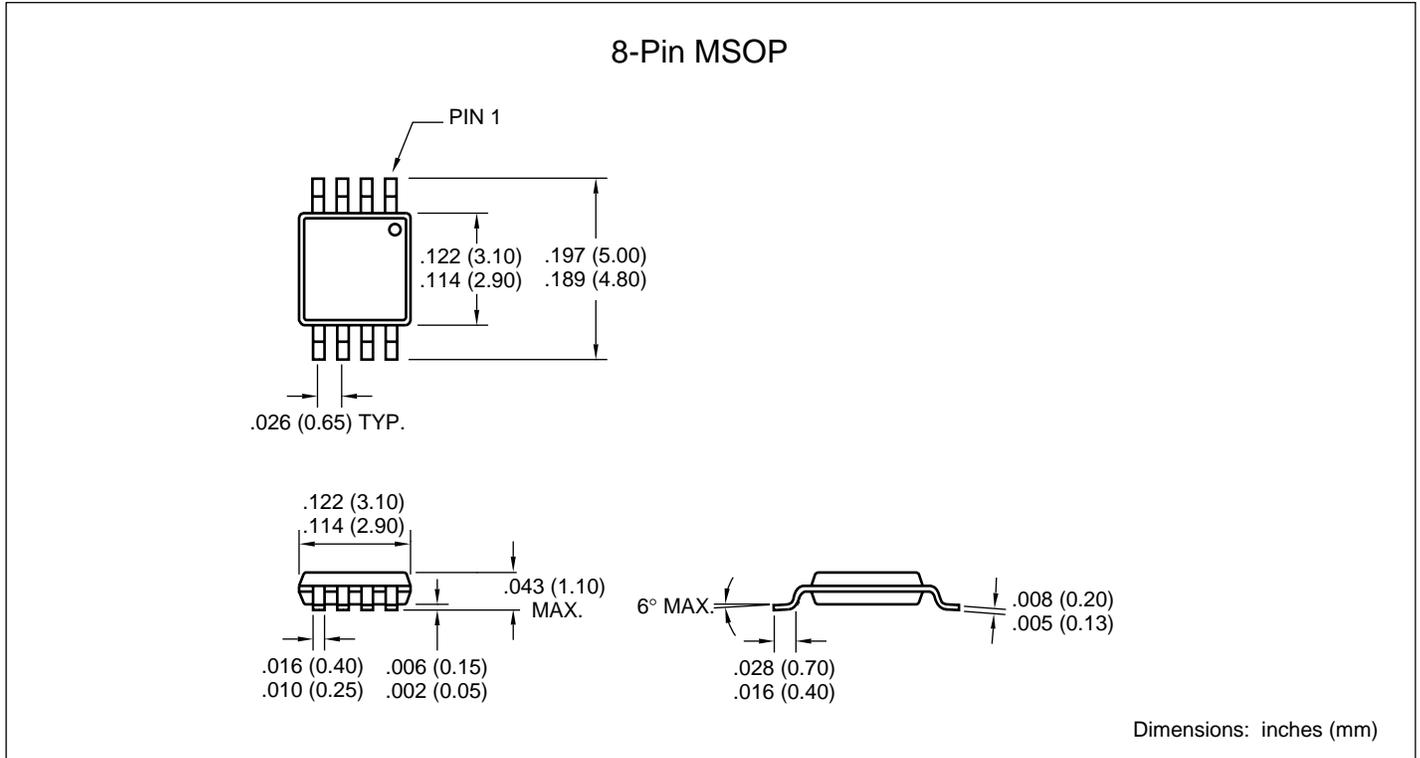
## TAPE AND REEL DIAGRAMS



# 300mA CMOS LDO with Shutdown, Bypass and Independent Delayed Reset Function

## TC1300

### PACKAGE DIMENSIONS





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