Features

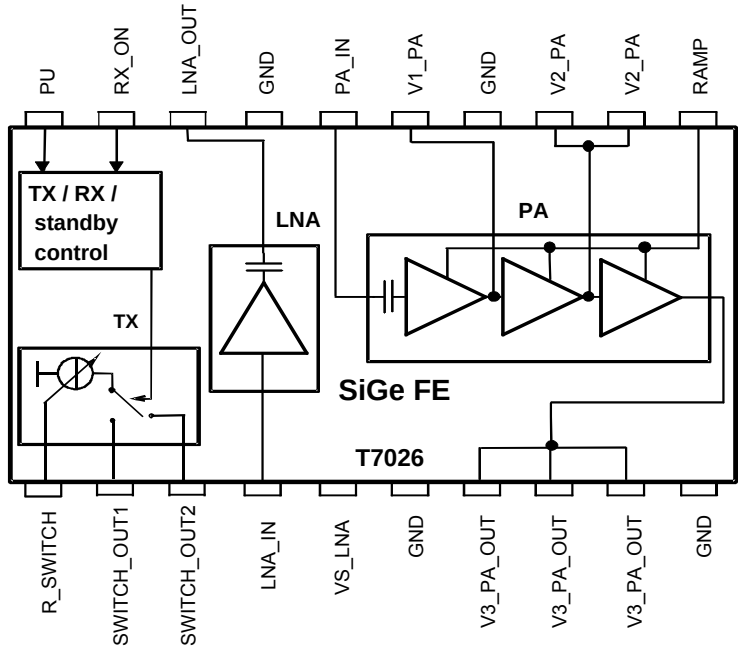
- **Single 3-V Supply Voltage**
- **High-power-added Efficient Power Amplifier (P_{out} Typically 28 dBm)**
- **Ramp-controlled Output Power**
- **Low-noise Preamplifier (NF Typically 2.1 dB)**
- **Biasing for External PIN Diode T/R Switch**
- **Current-saving Standby Mode**
- **Few External Components**
- **Package: HP-VFQFP-N20**

Description

The T7026 is a monolithic SiGe transmit/receive front-end IC with power amplifier, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like DECT, IEEE 802.11 FHSS WLAN, home RF and ISM proprietary radios. Due to the ramp-control feature and a very low quiescent current, an external switch transistor for V_S is not required.

Electrostatic sensitive device.
Observe precautions for handling.

Figure 1. Block Diagram



ISM 2.4 GHz Front End IC

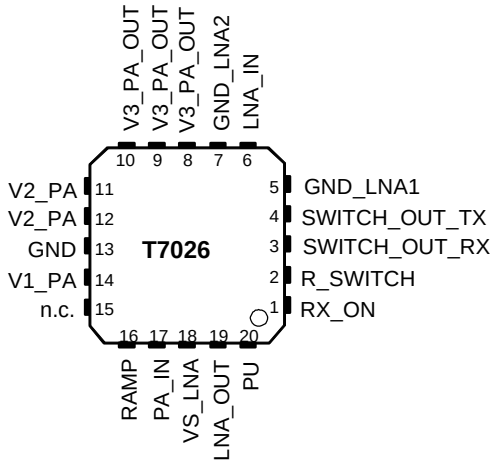
T7026

Preliminary

Rev. 4563A–ISM–11/02

Pin Configuration

Figure 2. Pinning HP-VFQFP-N20



Pin Description

Pin	Symbol	Function
1	RX_ON	RX active high
2	R_SWITCH	Resistor to GND sets the PIN diode current
3	SWITCH_OUT_RX	Switched current output for PIN diode (active in RX mode)
4	SWITCH_OUT_TX	Switched current output for PIN diode (active in TX mode)
5	GND_LNA1	Ground
6	LNA_IN	Low-noise amplifier input
7	GND_LNA2	Ground
8	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
9	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
10	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
11	V2_PA	Inductor to power supply for power amplifier
12	V2_PA	Inductor to power supply for power amplifier
13	GND	Ground
14	V1_PA	Supply voltage for power amplifier
15	n.c.	Not connected
16	RAMP	Power ramping control input
17	PA_IN	Power amplifier input
18	VS_LNA	Supply voltage input for low-noise amplifier
19	LNA_OUT	Low-noise amplifier output
20	PU	Power-up active high
Slug	GND	Ground

Absolute Maximum Ratings

All voltages are referred to ground (Pins GND and slug)

Parameters	Symbol	Value	Unit
Supply voltage Pins VS_LNA, V1_PA, V2_PA and V3_PA_OUT, no RF	V_S	5	V
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-40 to +125	°C
RF input power LNA	P_{inLNA}	-5 dBm	dBm
RF input power PA	P_{inPA}	10 dBm	dBm

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient HP-VFQFP-N20, slug soldered on PCB	R_{thJA}	27	K/W

Operating Range

All voltages are referred to ground (Pins GND and slug). Power supply points are VS_LNA, V1_PA, V2_PA, V3_PA_OUT. The following table represents the sum of all supply currents depending on the TX/RX mode.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage Pins V1_PA, V2_PA and V3_PA_OUT	V_S	2.7	3.6	4.6	V
Supply voltage Pin VS_LNA	V_S	2.7	3.0	5.5	V
Supply current TX RX	I_S I_S		470 8		mA mA
Standby current PU = 0	I_S		10		µA
Ambient temperature	T_{amb}	-25	+25	+70	°C

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 3.6 V, T_{amb} = 25°C

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Power Amplifier (1)						
Supply voltage	Pins V1_PA, V2_PA and V3_PA_OUT	V_S	2.7	3.0	4.6	V
Supply current	TX	I_{S_TX}		470		mA
	RX (PA off), $V_{RAMP} \leq 0.1$ V	I_{S_RX}			10	µA
Standby current	Standby for $V_{RAMP} \leq 0.1$ V	$I_{S\_standby}$			10	µA
Frequency range	TX	f	2.4		2.5	GHz

Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true cw operation, maximum load mismatch and duration TBD.
2. With external matching network, load impedance 50 Ω.
3. Low-noise amplifier shall be unconditionally stable.
4. With external matching components.

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_S = 3.6 V, T_{amb} = 25°C

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Gain-control range	TX	ΔGp	60	42		dB
Power gain maximum	TX Pin PA_IN to V3_PA_OUT	Gp	28	30	33	dB
Power gain minimum		Gp	-40		-17	dB
Ramping voltage maximum	TX, power gain (max), Pin RAMP	$V_{RAMP\ max}$	1.7	1.75	1.83	V
Ramping voltage minimum	TX, power gain (min), Pin RAMP	$V_{RAMP\ min}$		1		V
Ramping current maximum	TX, V_{RAMP} = 1.75 V, Pin RAMP	$I_{RAMP\ max}$			0.5	mA
Power-added efficiency	TX	PAE	33	37		%
Saturated output power	TX, input power = 0 dBm referred to Pins V3_PA_OUT	P_{sat}	27.5	28	28.5	dBm
Input matching (2)	TX Pin PA_IN	Load VSWR		<1.5:1	1.5 : 1	
Output matching (2)	TX Pins V3_PA_OUT	Load VSWR		<1.5:1	1.5 : 1	
Harmonics at P 1dBCP	TX Pins V3_PA_OUT	2 fo			-30	dBc
Harmonics at P 1dBCP	TX Pins V3_PA_OUT	3 fo			-30	dBc
T/R-switch Driver (Current Programming by External Resistor from R_SWITCH to GND)						
Switch-out current output	Standby, Pin SWITCH_OUT	$I_{S\_O\_standby}$			1	µA
	RX	$I_{S\_O\_RX}$			1	µA
	TX at 100 Ω	$I_{S\_O\_100}$		1.7		mA
	TX at 1.2 kΩ	$I_{S\_O\_1k2}$		7		mA
	TX at 33 kΩ	$I_{S\_O\_33k}$		17		mA
	TX at R switch open	$I_{S\_O\_R}$		19		mA
Low-noise Amplifier (3)						
Supply voltage	All, Pin VS_LNA	V_S	2.7	3.0	5.5	V
Supply current	RX	I_S		8	9	mA
Supply current (LNA and control logic)	TX (control logic active) Pin VS_LNA	I_S			0.5	mA
Standby current	Standby, Pin VS_LNA	$I_{S\_standby}$		1	10	µA
Frequency range	RX	f	2.4		2.5	GHz
Power gain	RX, Pin LNA_IN to LNA_OUT	Gp	15	16	19	dB
Noise figure	RX	NF		2.1	2.3	dB
Gain compression	RX, referred to Pin LNA_OUT	O1dB	-9	-7	-6	dBm
Third-order input interception point	RX	IIP3	-16	-14	-13	dBm
Input matching (4)	RX, Pin LNA_IN	VSWRin		<2:1	2:1	
Output matching (4)	RX, Pin LNA_OUT	VSWRout		<2:1	2:1	
Logic Input Levels (RX_ON, PU)						
High input level	= '1', Pins RX_ON and PU	V_{iH}	2.4		$V_{S,\ LNA}$	V

Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true cw operation, maximum load mismatch and duration TBD.
2. With external matching network, load impedance 50 Ω.
3. Low-noise amplifier shall be unconditionally stable.
4. With external matching components.

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_S = 3.6 V, T_{amb} = 25°C

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Low input level	= '0'	V_{iL}	0		0.5	V
High input current	= '1', V_{iH} = 2.4 V	I_{iH}		40	60	µA
Low input current	= '0'	I_{iL}			0.2	µA

Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true cw operation, maximum load mismatch and duration TBD.
2. With external matching network, load impedance 50 Ω.
3. Low-noise amplifier shall be unconditionally stable.
4. With external matching components.

Control Logic for LNA and T/R-switch Driver

Operation Mode	PU	RX_ON
Standby	0	0
TX	1	0
RX	1	1

Input/Output Circuits

Figure 3. Internal Circuitry; PA_IN, V1_PA

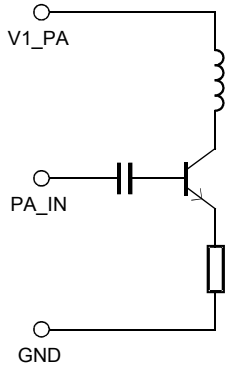


Figure 4. Internal Circuitry; RAMP, V1_PA

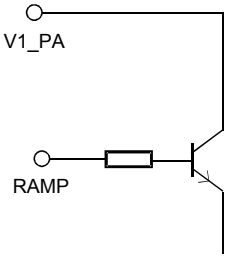


Figure 5. Internal Circuitry V2_PA

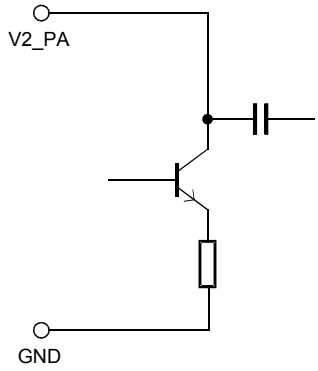


Figure 6. Internal Circuitry V3_PA_OUT

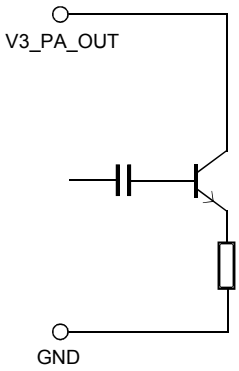


Figure 7. Internal Circuitry SWITCH_OUT_RX, SWITCH_OUT_TX, R_SWITCH, V1_PA

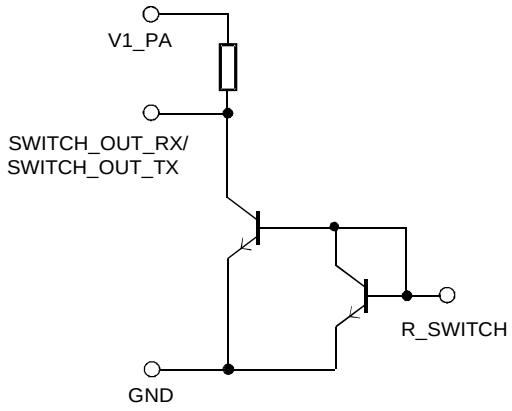


Figure 8. Internal Circuitry LNA_IN, VS_LNA

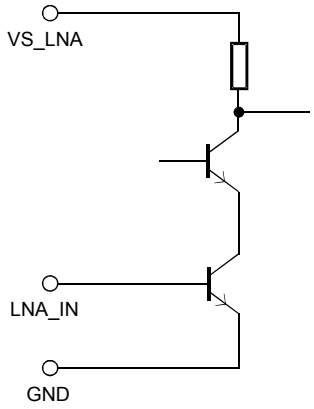


Figure 9. Internal Circuitry PU, RX_ON, VS_LNA

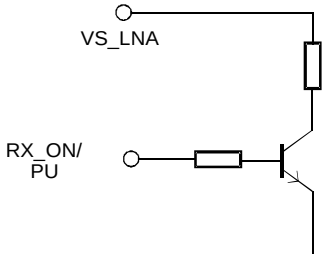
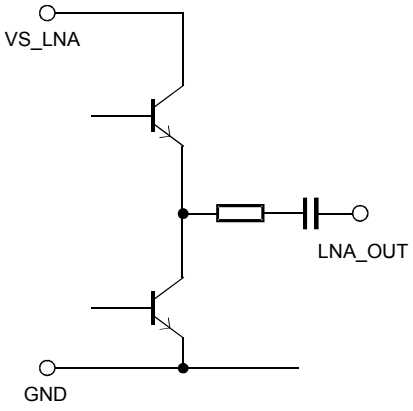


Figure 10. Internal Circuitry LNA_OUT, VS_LNA



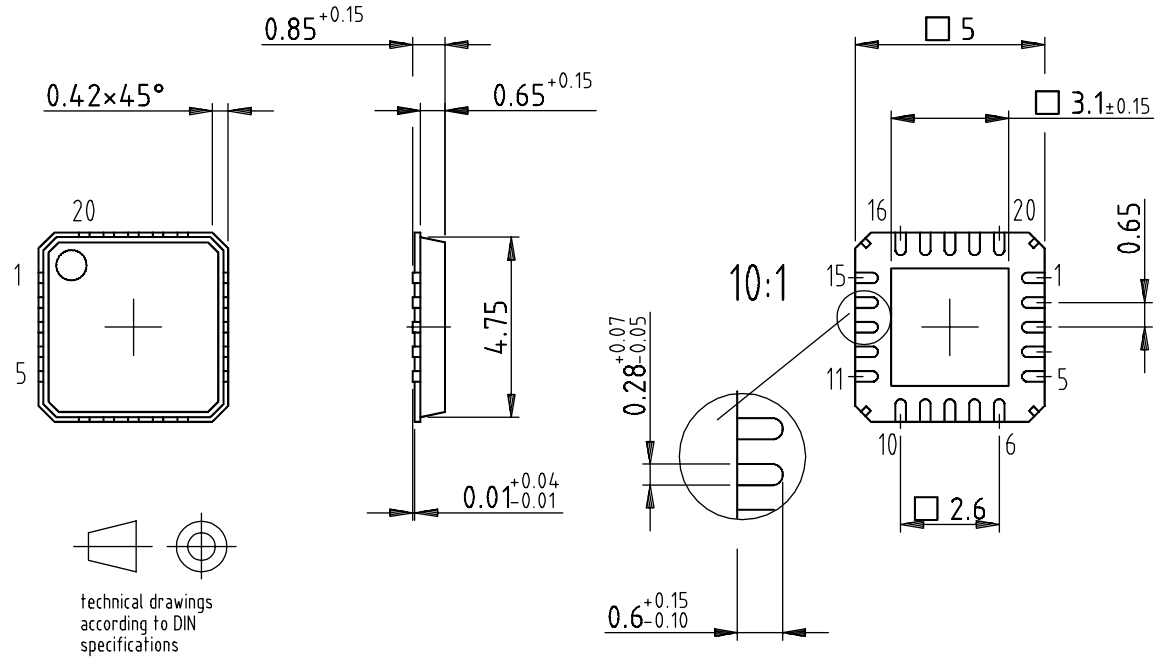
Ordering Information

Extended Type Number	Package	Remarks
T7026-PGS	HP-VFQFP-N20	Tube
T7026-PGQ	HP-VFQFP-N20	Taped and reeled

Package Information

Package: HP-VFQFP-N20
Exposed pad Var. A
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm



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