TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6K17

COLUMN AND ROW DRIVER LSI FOR A DOT MATRIX GRAPHIC LCD

The T6K17 is a driver for small−to−medium−sized dot matrix Liquid Crystal Display (LCD). This driver combines the functions of the T9841B (column driver) and the T9842B (row driver) into a more functionally advanced single−chip device.
The T6K17 can be interfaced with 8−bit general MPU; it operates asynchronously with the MPU. The T6K17 contains an RC oscillator circuit to generate the timing signal required for display and has a built−in RAM to store the display data. Each cell in this RAM corresponds to each dot on the dot matrix LCD. Therefore, the display data written to the RAM is corresponded one to one to the LCD as the LCD drive signal output. The T6K17 has 80 outputs for LCD drive signals (columns) that are equivalent to display data and 18 outputs for LCD drive signals (rows) that are equivalent to scan signals. Consequently, this single chip can drive up to 80 × 18 dots of LCD display with minimal power.
In addition, the T6K17 has the LCD power supply regulator, a voltage quadrupler, and a contrast control circuit enabling the LCD to be driven by a single power supply. To minimize current consumption in the oscillator, the T6K17 has an oscillator regulator.

Unit: mm

T6K17	User Area Pitch	
	IN	OUT
(UAM, 5NS)	0.7	0.26

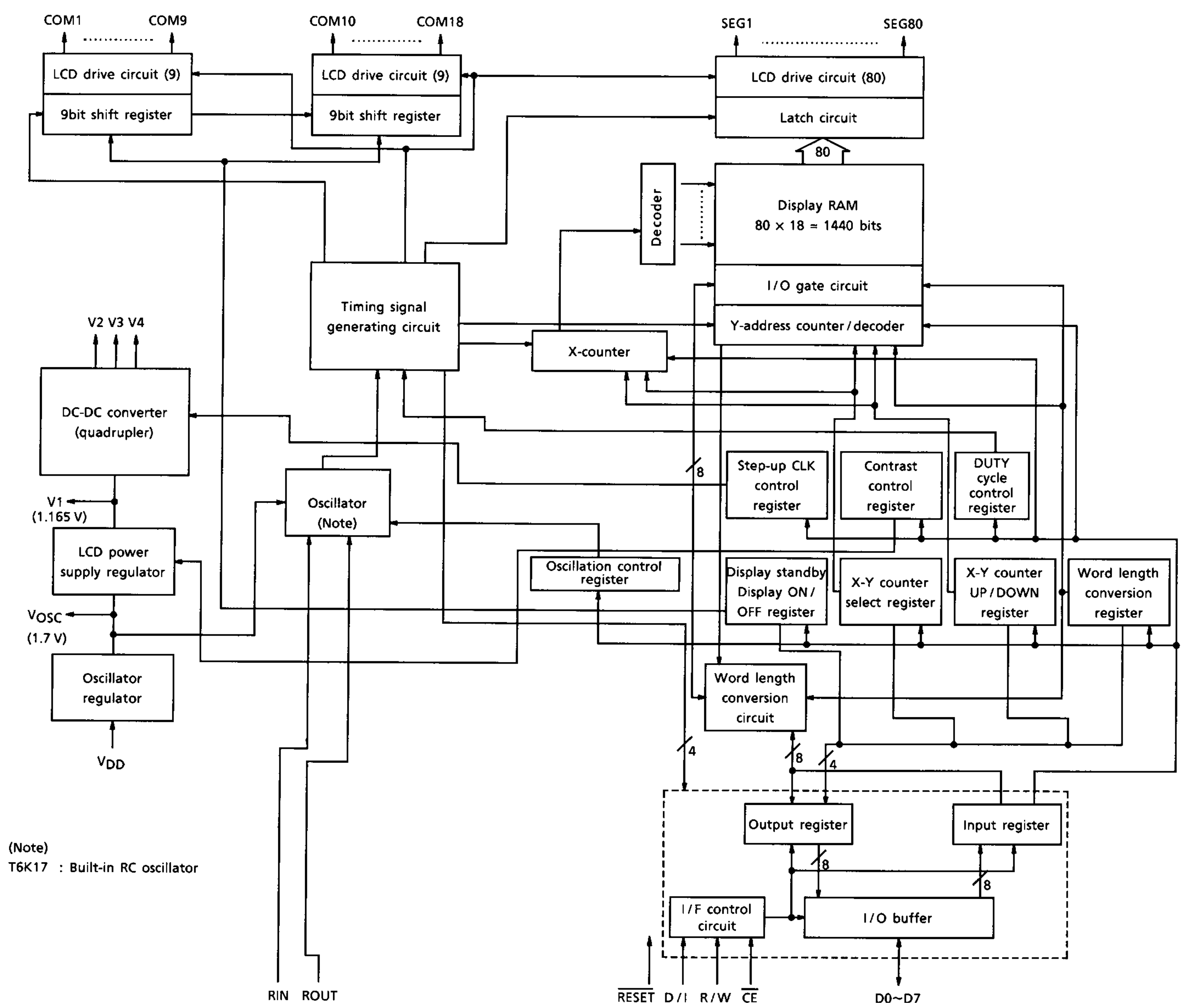
Please contact Toshiba or its distributor for information about the latest TCP specification and product lineup.

TCP (Tape Carrier Package)

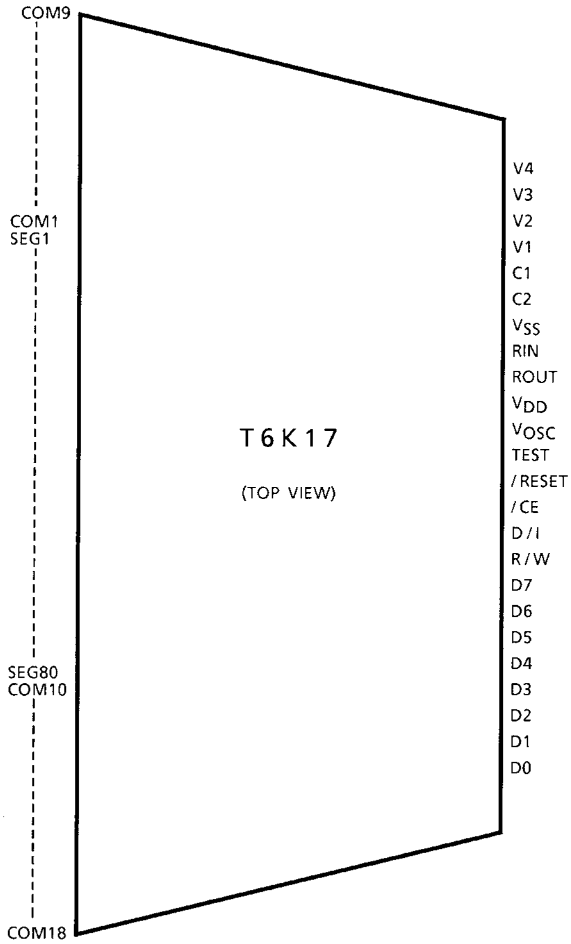
Features

- Built−in display RAM with 80 × 18 = 1440 bits of capacity.
- Direct RAM data display
  Dots are turned on when bit data in RAM = 1.
  Dots are not turned on when bit data in RAM = 0.
- Display duty cycle : 1/18 or 1/16 duty (switchable)
- Display data word length can be switched between 8 bits and 6 bits according to character font.
- LCD display drive circuit
  Segment output : 80 lines
  Common output : 18 or 16 lines (switchable)
- Can be interfaced with 8−bit general MPU (operated asynchronously).
- Data interface: Parallel data interface.
- Built−in oscillator circuit regulator (oscillator unit only is operated with 1.7 V).
- Built−in RC oscillator (T6K17: capacitor internal and resistor external to the chip)
  T6K17 is able to switch to external clock input by software.
- Built−in LCD power supply regulator, voltage quadrupler, and contrast control circuit (16−gradation). (4.1 to 5.3 V, 0.08 V / step)
- Low power consumption (8 μA during display without data access when operating at 3.0 V).
- CMOS process.
- Low−voltage operation : 1.8 to 5.5 V
- Operating voltage of LCD drive signal
  : (1) V4 = 4 times the LCD power supply regulator output V1.
  (2) 1 / 4 bias
- Package : Bump chip and 122 pins TCP

Block Diagram



Pin Assignment



Note: The above TCP pin assignment is shown for reference purposes only.

Pin Function

Pin Name	I / O	Function
SEG1 to SEG80	Ourput	Column drive output
COM1 to COM18	Ourput	Row driver output
D0 to D7	I / O	Data bus
D / I	Input	Data / instruction select signal input pin ● When D / I = High → The data on D0 to D7 is assumed to be display data. ● When D / I = Low → The data on D0 to D7 is assumed to be instruction data.
R / W	Input	Write select signal ● When R / W = High → The device is readied to read data. ● When R / W = Low → The device is readied to write data.
/ CE	Input	Chip enable signal input pin ● When writing the D0 to D7 data, drive /CE from low to high when R / W = low. ● When reading the D0 to D7 data, the data is output while /CE is held low when R / W = high.
/ RESET	Input	Reset signal input pin
RIN, ROUT	—	Connect an external resistor between these pins to use the built−in RC oscillator. If you want an external clock input, use RIN for clock input and leave ROUT open.
V_{OSC}	—	Oscillator circuit regulator output pin
C1, C2	—	External capacitor connecting pins
V1	—	LCD power supply regulator output pin
V2	—	×2 step−up voltage output pin
V3	—	×3 step−up voltage output pin
V4	—	×4 step−up voltage output pin
V_{DD}, V_{SS}	—	Power supply pins
TEST	Input	LSI test pin ● Leave this pin open or connect to V_{SS}.

Functional Specification and Device Operation

● Interface logic

The T6K17 can be interfaced with 8−bit general MPU.
Figure 1 shows an example of how the device is interfaced with the MPU.

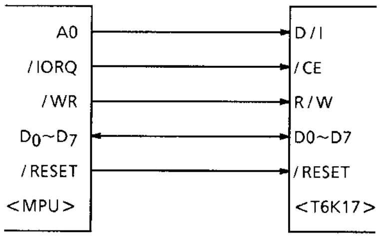


Figure 1

● Input register

This register holds the 8−bit data from the MPU.
The data held in this register is discriminated between instruction and display data by the D / I signal.

● Output register

This register holds the 8−bit data to the MPU.
The data in this register came from the display RAM or STRD register is discriminated between display data and instruction by D / I signal.

● X−address counter

This counter is an 18−up / down−counter used to hold the address in the column direction of the display RAM.
When X−counter is selected by a command, the counter is automatically incremented or decremented by 1 each time the MPU reads or writes to the display RAM.

● Y (Page) −address counter

This counter has its count values changed depending on the word length of display data.
If the word length is 8 bits, the Y (page) −address counter is a 10−up / down-counter. If the word length is 6 bits, the Y (page) −address counter is a 14−up / down−counter. In either case, the counter holds the address in the row direction of the display RAM. When a Y (page) −counter is selected by a command, the counter is automatically incremented or decremented by 1 each time the MPU reads or writes to the display RAM.

● X and Y−counter UP / DOWN register

This register holds data to determine whether the X−and Y−counters function as an up−or down−counter.

● X and Y−counter select register

This register holds data to determine which counter is enabled, X−or Y−counter.

● Display standby and display ON / OFF registers

The display standby register (1 bit) holds the standby status of display. When display is in standby state, the LCD drive signal is disabled (V_{SS}). In active state, the LCD drive signal is enabled for output.
The display ON / OFF register (1 bit) holds the ON / OFF status of display. When display is in OFF state, the output from the display RAM is reset. In ON state, the display data is output from the display RAM. The data in the display RAM is not affected by the ON / OFF status of display.

● Word length change register

This register holds data to determine whether the display data is read and written in 8 bits per word or 6 bits per word.

- **Word length change circuit**

This circuit is controlled by the data held in the word length conversion register.
If the word length is 8 bits, the 8 bit data is read and written directly as is. If the word length is 6 bits, the 8−bit display data held in the input register has had its two MSB bits nullified as the data is written to the display RAM as shown in Figure 2. When reading data, the 6−bit data from the display RAM has had 0s added in its two MSB bits so that it is stored in the output register as 8−bit data.

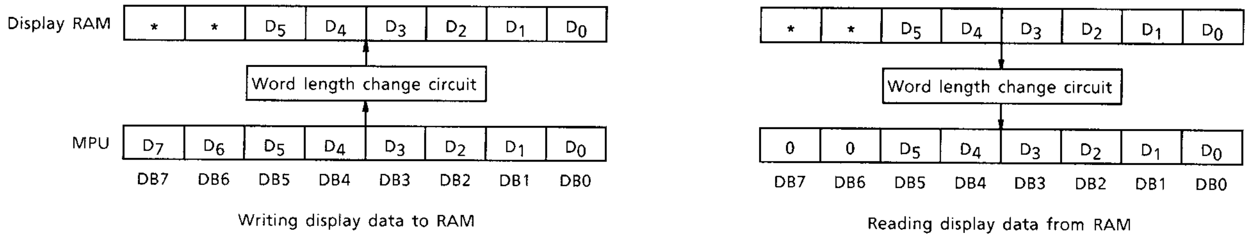


Figure 2

- **Oscillator**

The oscillator in the T6K17 can be an RC oscillator. In T6K17 case, connect an external resistor between the RIN and ROUT pins. When using external clock for the device, use RIN to supply the clock.

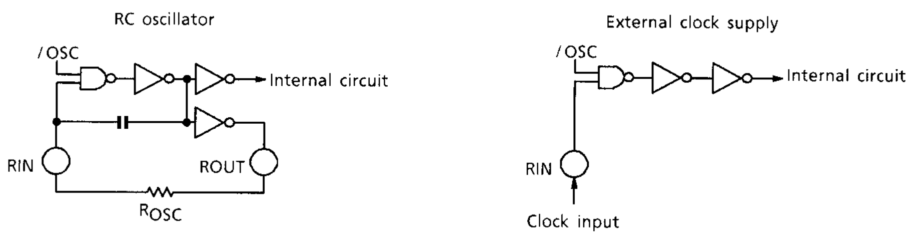


Figure 3

- **Oscillation control register**

This register holds the active / inactive status of the oscillator.
When the oscillator is in inactive state, the internal logic of the device is stopped entirely because the oscillator is disabled. In active state, the oscillator is enabled supplying clock to the device. The oscillator circuit can be selected according to the type of oscillator (RC or external clock as described above).

- **Oscillator regulator**

This regulator generates V_{OSC} to drive the oscillator.
Connect a capacitor to V_{OSC} in order to stabilize the regulator voltage.

- **Timing signal generation circuit**

This circuit generates the necessary display timing signals and operating clock by dividing the source clock from the oscillator.

- **Shift register**

The T6K17 has two channels of 9−bit shift registers to shift the turn−on data that is required for common signals to drive the LCD.

- **Display latch circuit**

This circuit latches display data as it is fed from the display RAM.

- **Column driver circuit**

The column driver circuit consists of 80 driver circuits. Each driver circuit outputs one of the three LCD drive voltages that derive from a combination of the display data from the latch circuit and the M signal as shown in Figure 4.
The diagram below depicts the column driver circuit.

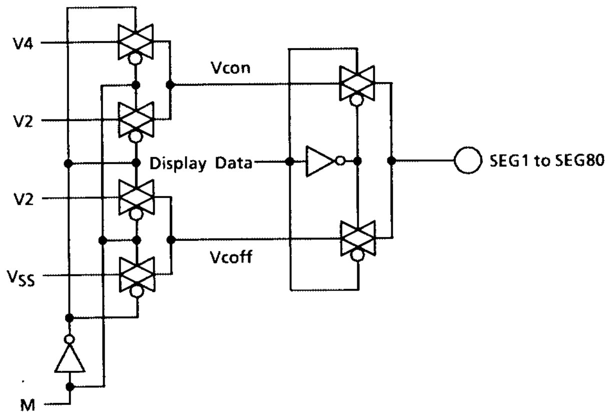


Figure 4

- **Row driver circuit**

The row driver circuit consists of 18 driver circuits. Each driver circuit outputs one of the four LCD drive voltages that derive from a combination of the shift register data and the M signal as shown in Figure 5.
The diagram below depicts the row driver circuit.

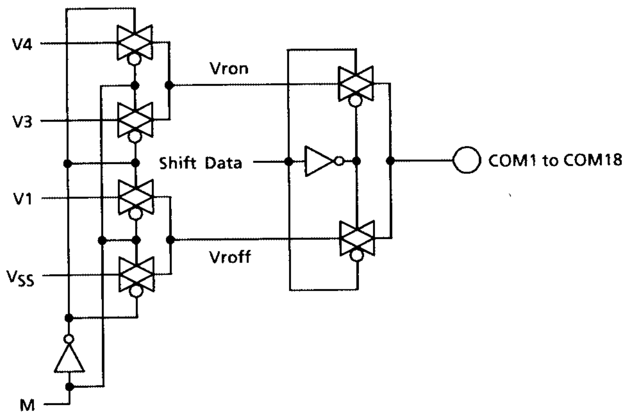


Figure 5

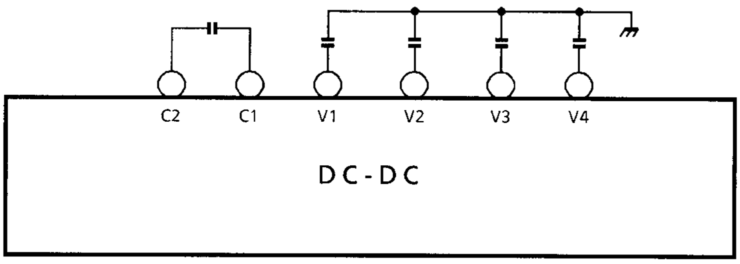
- **LCD power supply regulator**

This regulator generates the reference voltage V1 for the voltage quadrupler circuit that generates the power to LCD.
Connect a capacitor to V1 in order to stabilize the regulator output.

- **DC−DC converter (Voltage quadrupler)**

This circuit boosts the V1 voltage generated by the LCD power supply regulator four−fold by using a step−up capacitor. Insert a step−up capacitor between C1 and C2 and connect smoothing capacitors to V2, V3 and V4. Normally use capacitors of about 0.1μF here.

Connecting Capacitors to the Voltage Quadrupler Circuit



- **Contrast control circuit**

The T6K17 contains a contrast control circuit in their LCD power supply regulator.
Contrast is varied in 16 steps by data from the contrast control register. This is done by changing the output voltage V1 of the LCD power supply regulator by using data from the contrast control register. The voltage quadrupler circuit generates the V4 voltages listed in the table below from the V1 reference voltage. (Refer to command definitions for details about CONT3 to CONT0.)

CONT3	CONT2	CONT1	CONT0	V4 Output Voltage
1	1	1	1	5.30 V ± 0.2 V
1	1	1	0	5.22 V ± 0.2 V
1	1	0	1	5.14 V ± 0.2 V
1	1	0	0	5.06 V ± 0.2 V
1	0	1	1	4.98 V ± 0.2 V
1	0	1	0	4.90 V ± 0.2 V
1	0	0	1	4.82 V ± 0.2 V
1	0	0	0	4.74 V ± 0.2 V
0	1	1	1	4.66 V ± 0.2 V
0	1	1	0	4.58 V ± 0.2 V
0	1	0	1	4.50 V ± 0.2 V
0	1	0	0	4.42 V ± 0.2 V
0	0	1	1	4.34 V ± 0.2 V
0	0	1	0	4.26 V ± 0.2 V
0	0	0	1	4.18 V ± 0.2 V
0	0	0	0	4.10 V ± 0.2 V

Table 1

Note: The voltage range in the above table 1 are reference value, not specification.

● Duty cycle control register

This 1−bit register holds the selected status of the duty cycle.
The display duty cycle can be selected from 1/16 duty and 1/18 duty.

● Display RAM

The display RAM consists of an array of 80 cells in the segment (column) direction and 18 cells in the common (row) direction providing a total of 1,440 bits of storage capacity. The dot matrix LCD (i.e., the display screen) and the display RAM have a relationship that each dot on the display screen corresponds to one bit in the display RAM as shown in Figure 8. If the data written to RAM = 1, the dot on the display screen corresponding to that RAM cell is turned on (black). If the data written to RAM = 0, the corresponding dot on the display screen is turned off (white).

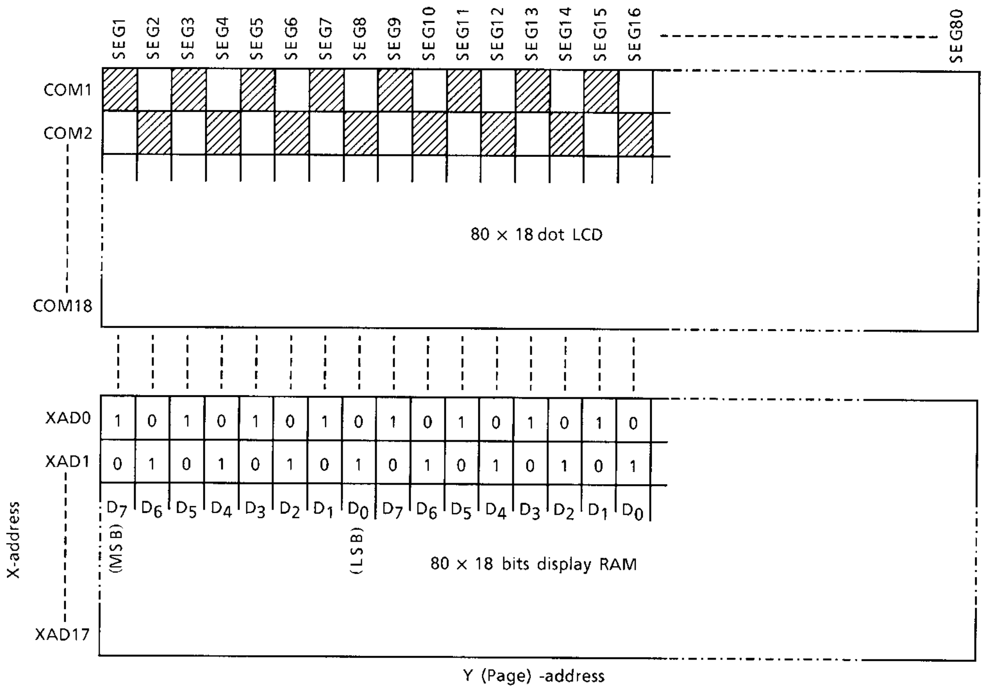
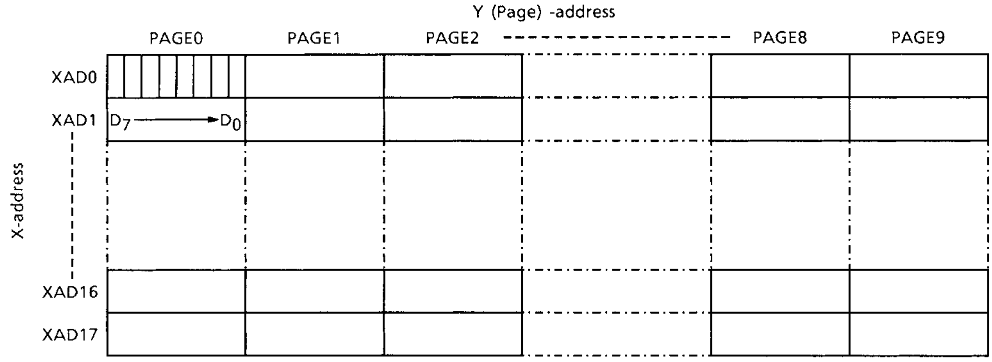


Figure 8

Furthermore, the display RAM addresses change with the word length setting. If the word length is set to 8 bits / WORD by executing command 86BS, the Y (page) −address is assigned YAD0 to YAD9, with one page configured with 8 bits. If the word length is set to 6 bits / WORD, the Y (page) −address is assigned YAD0 to YAD13, with one page configured with 6 bits.

8 bits per word mode



6 bits per word mode

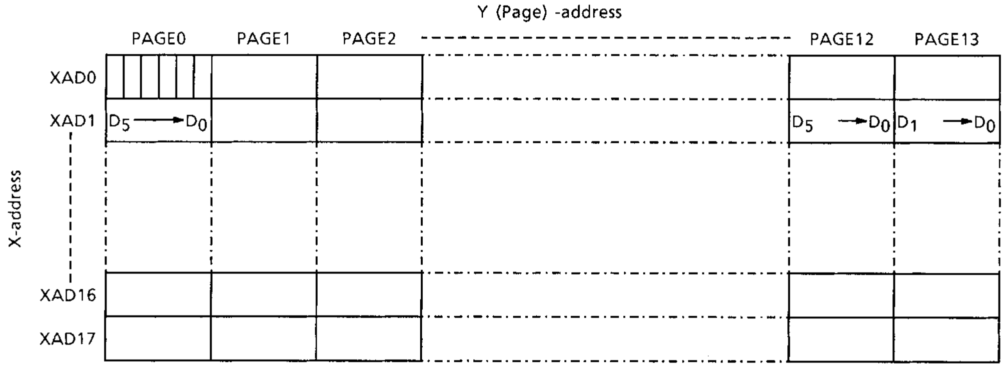


Figure 9

- **Command definitions**

Command Name	R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	Function
DISP	0	0	0	0	0	0	0	0	1 / 0	1 / 0	● Display ON / OFF (DISPON): D1 Display ON (1) / Display OFF (0) ● Display standby (DISPST): D0 Active (1) / Standby (0)
BSDT	0	0	0	0	0	0	1	0	1 / 0	1 / 0	● Word length (86BS): D1 8 bits (1) / 6 bits (0) ● Duty cycle (DUTY): D0 1/18 duty (1) / 1/16 duty (0)
OSC	0	0	0	0	0	1	0	0	0	1 / 0	● Oscillator enable (OSC) : Oscillation enabled (1) : Oscillation disabled (0)
OSCM	0	0	0	0	1	0	0	0	0	1 / 0	Oscillation mode select
PUMP	0	0	0	1	0	0	0	0	1 / 0	1 / 0	Voltage quadrupler clock select
CONT	0	0	0	1	1	1 / 0	Contrast (0 to 15)				● Voltage quadrupler enable (4BION) : D4 Enabled (1) / Disabled (0) ● Contrast set (CONT0 to CONT3) : D0 to D3
UDE	0	0	1	0	0	0	0	0	1 / 0	1 / 0	● Count select (Y / X): D1 Y (1) / X (0) ● Mode select (U / D): D0 UP (1) / DOWN (0)
SXE	0	0	1	1	0	X−address (0 to 17)					X−address set
SYE	0	0	1	1	1	0	Y−address (0 to 13)				Y (Page) −address set
STRD	1	0	0	86BS	DISP ON	R	0	0	Y / X	U / D	Status read
DAWR	0	1	Write Data								Display data write
DARD	1	1	Read Data								Display data read

- **Display standby select (DISP: DISPST)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	*	1	Display active (03H, 01H)
0	0	0	0	0	0	0	0	0	0	Display standby (00H)

The DISPST bit of command DISP controls display by making it active and standby. When "Display active" is selected, the DISPON bit is enabled, turning display ON or OFF.

Note: If "Display standby" is selected, the LCD drive signal is fixed to V_{SS}.

Note: When using "Display standby", make sure that display is turned OFF (D1 = 0).
When the device is reset, the display is placed in standby state by default.

- **Display ON / OFF select (DISP: DISPON)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	1	1	Display ON (03H)
0	0	0	0	0	0	0	0	0	1	Display OFF (01H)

The DISPON bit of command DISP controls display by turning it ON and OFF. Since the display data in RAM is not affected by the DISP command, the display data in RAM is not cleared to 0s even when display is turned OFF by this command.

Note: Display is turned OFF when the device is reset (by pulling / RESET low).

Display state (DISPON, DISPST)

D1	D0	Display State
0	0	COM / SEG: Fixed to V_{SS}
0	1	Outputs a display OFF level waveform.
1	1	Outputs a display ON level waveform.

- **Word length 8 bits / 6 bits select (BSDT: 86BS)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	1	0	1	*	Word length 8−bit / Word mode
0	0	0	0	0	0	1	0	0	*	Word length 6−bit / Word mode

The 86BS bit of command BSDT sets the word length of the display data stored in display RAM to 8 bits or 6 bits.

Note: When the device is reset, the word length is set to 8 bit / Word mode by default.

- **Duty select (BSDT: DUTY)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	1	0	*	1	1/18 duty
0	0	0	0	0	0	1	0	*	0	1/16 duty

The DUTY bit of command BSDT sets the display duty cycle to 1/18 or 1/16.

Note: When the device is reset, the display duty cycle is set to 1/16 by default.

- **X / Y counter and UP / DOWN mode select (UDE: X / Y and U / D)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	1	0	0	0	0	0	0	0	X−counter DOWN mode	(80H)
0	0	1	0	0	0	0	0	0	1	X−counter UP mode	(81H)
0	0	1	0	0	0	0	0	1	0	Y−counter DOWN mode	(82H)
0	0	1	0	0	0	0	0	1	1	Y−counter UP mode	(83H)

The UDE command selects the display RAM address counter from X−counter or Y−counter when reading and writing display data and specifies whether the selected counter counts the address up or down. Therefore, if you select X−counter UP mode, for example, the X−address is incremented each time the MPU reads or writes to the RAM. On the other hand, the Y−counter is disabled, so the Y (page) −address is set by executing the command SYE.

Note: When the device is reset, the Y−counter UP mode is selected by default.

- **Y (Page) −address set (SYE)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	A	A	A	A

Set up range 8−bit / WORD: E0H to E9H (Page 0 to Page 9)
6−bit / WORD: E0H to EDH (Page 0 to Page 13)

The SYE command selects one page from 0 to 9 page display RAM when the word length of display data is set to 8−bit / WORD by the BSDT command or from 0 to 13 page display RAM when the word length is set to 6−bit / WORD. When the selected word length is 8−bit / WORD, make sure that address is always set within 9 pages. When the selected word length is 6−bit / WORD, make sure that address is always set within 13 pages.

Note: When the device is reset, the Y (page) −address is set to page 0 by default.

- **X−address set (SXE)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	A	A	A	A	A

Set up range: C0H to D1H (XAD0 to XAD17)
The SXE command sets an X−address.

Note: When the device is reset, the X−address is set to 0 by default.

- **Contrast set (CONT: CONT0 to CONT3)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	*	A	A	A	A

Set up range: 60H to 6FH or 70H to 7FH
The CONT0 to CONT3 bits of command CONT set the display density of the LCD screen. The display density is set in 16 steps, with 60H / 70H the lightest, and 6FH / 7FH the darkest.

Note: When the device is reset, the display density is set to the lightest level of 60H by default.

- **Voltage quadrupler circuit enable (CONT: 4BION)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	1	0	*	*	*	*	Voltage quadrupler circuit disabled
0	0	0	1	1	1	*	*	*	*	Voltage quadrupler circuit enabled

The 4BION bit of command CONT controls the voltage quadrupler circuit. When the voltage quadrupler circuit is enabled by this command, its operation is activated, outputting boosted voltage to V1 through V4.

Note: When the device is reset, the voltage quadrupler circuit is disabled by default.

- **Oscillator enable (OSC)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	1	0	0	0	1	Oscillation enabled (11H)
0	0	0	0	0	1	0	0	0	0	Oscillation disabled (10H)

The OSC command controls the operation of the oscillator circuit by enabling or disabling it.
When the oscillator circuit is disabled, the oscillator stops oscillating, so it stops clocking the internal logic of the device.

Note: When the device is reset, the oscillator circuit is enabled by default.

- **Oscillation mode select (OSCM)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	1	0	0	0	0	0	External clock supply mode	(20H)
0	0	0	0	1	0	0	0	0	1	RC oscillator mode using external resistor	(21H)
0	0	0	0	1	0	0	0	1	0	Usage inhibited	(22H)
0	0	0	0	1	0	0	0	1	1	Usage inhibited	(23H)

The OSCM command determines the operating mode of the oscillator circuit.
Choose the appropriate mode of operation depending on the type of oscillator (RC oscillator with external resistor or external clock).

Note: When the device is reset, the oscillator mode is set to “External clock supply mode” by default.

- **Voltage quadrupler clock select (PUMP)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	0	0	0	0	0	0	Voltage quadrupler clock 1/2 f_{OSC} (40H)
0	0	0	1	0	0	0	0	0	1	Voltage quadrupler clock 1/4 f_{OSC} (41H)
0	0	0	1	0	0	0	0	1	0	Voltage quadrupler clock 1/8 f_{OSC} (42H)
0	0	0	1	0	0	0	0	1	1	Voltage quadrupler clock f_{OSC} (43H)

The PUMP command selects the operating clock for the voltage quadrupler circuit.

Note: When the device is reset, the 1/2 f_{OSC} clock is selected for the voltage quadrupler circuit by default.

- **Status read (STRD)**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	86BS	DISPON	R	0	0	Y / X	U / D

The STRD command lets you know the status of the T6K17.

86BS (word length) : The word length is 8 bit / WORD when 86BS = 1.
The word length is 6 bit / WORD when 86BS = 0.

DISPON (Display) : Display is turned ON when DISPON = 1.
Display is turned OFF when DISPON = 0.

R (Reset) : The device is reset when R = 1.
The device is active (reset deasserted) when R = 0.

Y / X (Counter) : Y (page) −counter is selected when Y / X = 1.
X−counter is selected when Y / X = 0.

U / D (UP / DOWN) : The X / Y counter functions as an up−counter when U / D = 1
The X / Y counter functions as a down−counter when U / D = 0.

- **Write / Read display data**

R / W	D / I	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	D	D	D	D	D	D	D	D	DAWR : display data write
1	1	D	D	D	D	D	D	D	D	DARD : display data read

The DAWR command writes display data to the predefined address in RAM. The DARD command reads display data from the specified address in RAM.

Detailed Description of Functions

● X−address counter and Y (page) −address counter

The following explains how the X−address counter and Y (page) −address counter operate when each specific command is issued. Figure 11 shows a typical operation of the X−address counter.
After a reset on the device is deasserted, the X−address (XAD) is initialized to XAD = 0. Use the UDE command to select the X−counter UP mode. Next, issue the SXE command to set the X−address to 16. Then read or write data, at which time the X−address counter will be automatically incremented as it counts up. When data is read or written at XAD = 17, the X−address recycles to XAD = 0. Use the UDE command again to select the X−counter DOWN mode this time. Then read or write data, at which time the X−address will be decremented as the counter counts down. When data is read or written at XAD = 0, the X−address recycles to XAD = 17.
At this time, the Y (page) −address counter does not operate.

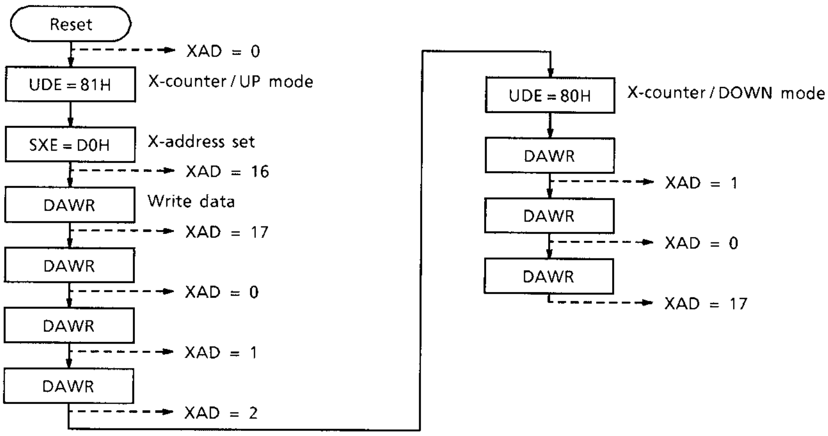


Figure 11

Figure 12 shows a typical operation of the Y (page) −address counter when the word length is 8 bit / WORD.
After a reset on the device is deasserted, the Y (page) −address (PAGE) is initialized to Page = 0.
Use the UDE command to select the Y−counter UP mode and the BSDT command to select the 8 bit / WORD mode. Then read or write data, at which time the Y (page) −address counter will be incremented. When data is read or written at Page = 9, the Y (page) −address recycles to Page = 0.
Conversely, if data is read or written when the Y−counter DOWN mode is selected by the UDE command, the Y (page) −address is automatically decremented as the Y (page) −address counter counts down. Then when data is read or written at Page = 0, the Y (page) −address recycles to Page = 9.
At this time, the X−address counter does not operate.

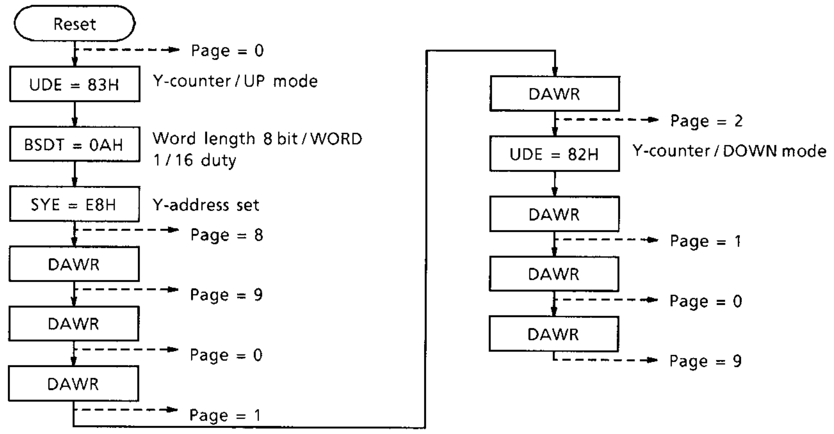


Figure 12

If the word length is 6−bit / WORD, the Y (page) −address counter is tetra decimal Up / Down counter. Therefore, when data is read or written at Page = 13 in UP mode, the Y (page) −address recycles to Page = 0. When data is read or written at Page = 0 in DOWN mode, the Y (page) −address recycles to Page = 13.

- **Data read**

T6K17 can read display data directly from the display RAM after executing the SYE and SXE commands to set addresses. See Figure 13.

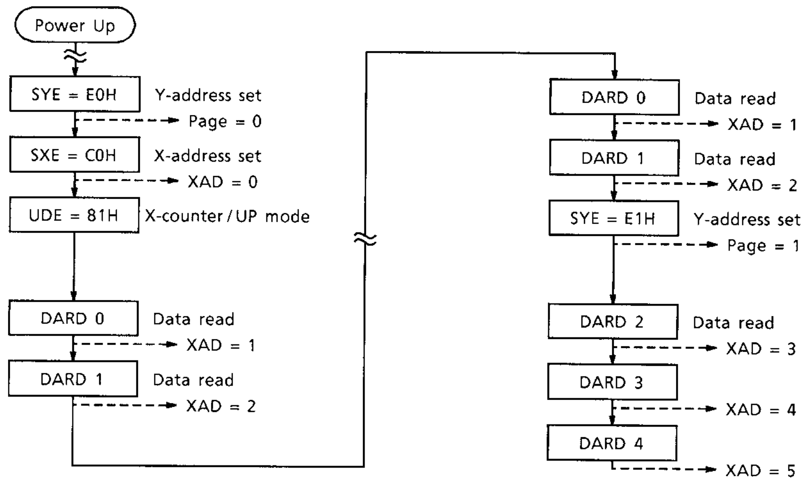


Figure 13

● Reset function

The T6K17 has a reset input pin designated as / RESET. A low on this input resets the T6K17 and its internal circuits are initialized as follows

- Display .... Standby
- Duty cycle .... 1/16 duty
- Word length .... 8 bit / WORD
- Counter .... Y−counter / UP mode
- Y (Page) −address counter .... Page = 0
- X−address counter.......................... Xad = 0
- Voltage step−up circuit .... Disabled; step−up clock = 1/2 f_{OSC}
- Contrast .... Minimum
- Oscillation....................................... External clock is fed to the device.

* Please be sure to execute Reset Function at the time of a power−supply.

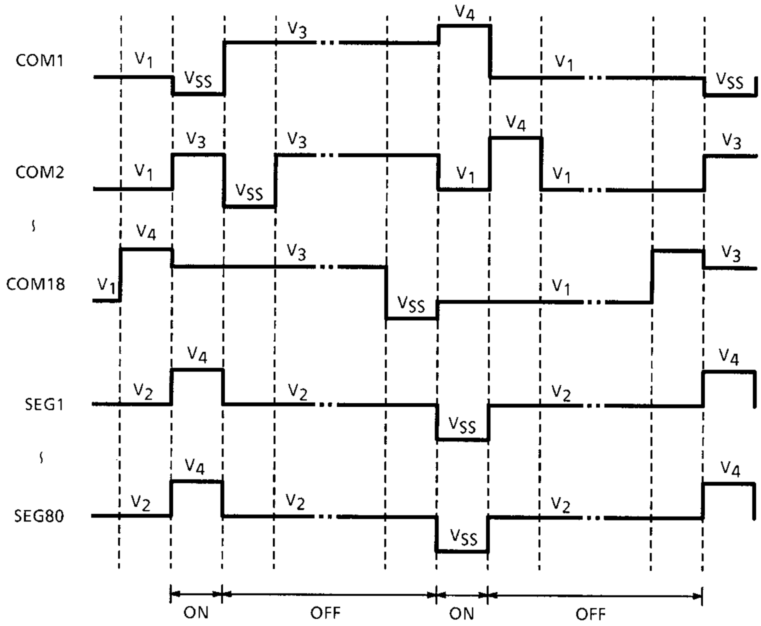
● About oscillation frequency

The T6K17 has a command named OSCM that allows you to choose the operating clock for the device from the built−in RC oscillator (using an external resistor) or an external clock source.
The equations below show the relationship between the oscillation frequency (f_{OSC}) and frame frequency (f_F):

$$f_{F[Hz]} = f_{OSC} \times \frac{1}{432}$$ (when operating with 1/18 duty)

$$f_{F[Hz]} = f_{OSC} \times \frac{1}{384}$$ (when operating with 1/16 duty)

- **LCD Driver Waveform**



LCD drive timing chart (1 /18 duty)

Maximum Ratings

Characteristic	Symbol	Rating	Unit
Power Supply Voltage	V_{DD} (Note)	−0.3 to 6.5	V
Input Voltage	V_{IN} (Note)	−0.3 to V_{DD} + 0.3	V
Operating Temperature	Topr	−20 to 75	°C
Storage Temperature	T_{stg}	−40 to 125	°C

Note: Referred to V_{SS} = 0 V.

Electrical Characteristics
(Unless Otherwise Notes, V_{SS} = 0 V and V_{DD} = 1.8 ~ 5.5 V at Ta = 25°C)

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Voltage		V_{DD}	—	—	1.8	3.0	5.5	V	V_{DD}
Input Voltage	H Level	V_{IH}	—	—	V_{DD} × 0.75	—	V_{DD}	V	D0 to D7 / CE, R / W D / I, TEST
	L Level	V_{IL}	—	—	V_{SS}	—	V_{DD} × 0.25		
Output Current	H Level	I_{OH}	—	V_{OUT} = V_{DD} − 0.5 V	—	—	−0.8	mA	D0 to D7
	L Level	I_{OL}	—	V_{OUT} = 0.5 V	0.8	—	—		
Input Leakage Current		I_{IH} I_{IL}	—	V_{IN} = V_{DD} to GND	−1	—	1	μA	D0 to D7 / CE, R / W D / I, / RESET TEST
Operating Frequency		f_{OSC}	—	—	28	33	66	kHz	RIN
External Clock Frequency		f_{ex}	—	—	28	33	66	kHz	RIN
External Clock Duty Cycle		f_{duty}	—	—	45	50	55	%	RIN
External Clock Rise / Fall Times		t_r / t_f	—	—	—	—	50	ns	RIN
Current Consumption (1)		I_{HALT} (1)	—	Display turned off, V_{DD} = 3.0 V using RC ROSC = 620 kΩ	—	5.0	10.0	μA	V_{DD}
Current Consumption (2)		I_{HALT} (2)	—	Display turned on, V_{DD} = 3.0 V f_{OSC} = 33 kHz, V−quad clock = 1/2 f_{OSC} select Contrast7	—	13.0	25.0	μA	V_{DD}
Current Consumption (3)		I_{STOP}	—	V_{DD} = 3.0 V	—	0.9	3.0	μA	V_{DD}
Current Consumption (4)		I_{RUN}	—	V_{DD} = 3.0 V Tcyc = 100 kHz During data access	—	35	80	μA	V_{DD}

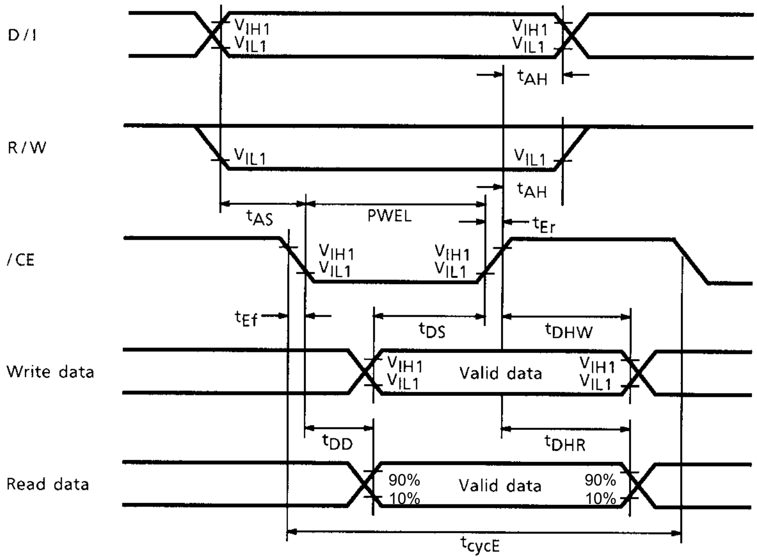
Note: RC oscillator frequency (typ. 33 kHz)
External resistance = 620 kΩ
Voltage limits = 1.8 to 5.5 V
V−quad: Voltage quadrupler

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Pull−Up Resistance	R_{PU}	—	V_{OUT} = 0 V	30	60	90	kΩ	/ RESET
Pull−Down Resistance	R_{PD}	—	V_{OUT} = V_{DD}	50	100	150	kΩ	TEST
Common Output Current	IOM1	—	V_{OUT} = V_3 − 0.5 V	—	—	−250	μA	COM1 to COM18
	IOM2	—	V_{OUT} = V_1 + 0.5 V	250	—	—		
	IOH	—	V_{OUT} = V_4 − 0.5 V	—	—	−250		
	IOL	—	V_{OUT} = 0.5 V	250	—	—		
Segment Output Current	IOM3	—	V_{OUT} = V_2 + 0.5 V	150	—	—	μA	SEG1 to SEG80
	IOM3	—	V_{OUT} = V_2 − 0.5 V	—	—	−150		
	IOH	—	V_{OUT} = V_4 − 0.5 V	—	—	−150		
	IOL	—	V_{OUT} = 0.5 V	150	—	—		
Step−up Output Voltage	VO	—	Select contrast 7 CONT [3: 0] = 0111	1.115	1.165	1.215	V	V1
		—	Select contrast 7 CONT [3: 0] = 0111	2.23	2.33	2.43		V2
		—	Select contrast 7 CONT [3: 0] = 0111	3.35	3.50	3.65		V3
		—	Select contrast 7 CONT [3: 0] = 0111	4.46	4.66	4.86		V4
RC Oscillator External Resistance	ROSC	—	When V_{DD} = 3.0 and f_{OSC} = 33kHz	—	560	—	kΩ	RIN, ROUT

Reference materials

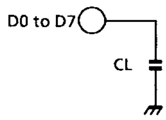
Characteristic	Symbol	Test Circuit	Test Condition	Voltage Quadrupler Clock			Unit
				1/8 f_{OSC}	1/4 f_{OSC}	f_{OSC}	
				Typ.	Typ.	Typ.	
Current Consumption (2)	I_{HALT} (2)	—	Display turned on, using RC ROSC = 620 KΩ Standard contrast V_{DD} = 3.0 (V)	8	9.5	18.5	μA

AC Characteristics (V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, V_4 = 4.66 V, Ta = 25°C)



Characteristic	Symbol	Min	Max	Unit
Enable Cycle Time	t_{cycE}	550	—	ns
Enable Pulse Width	PWEL	330	—	ns
Enable Rise / Fall Times	t_{Er}, t_{Ef}	—	25	ns
Address Set Up Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	0	—	ns
Data Set Up Time	t_{DS}	100	—	ns
Write Data Hold Time	t_{DHW}	20	—	ns
Data Delay Time	t_{DD} (Note)	—	200	ns
Read Data Hold Time	t_{DHR} (Note)	20	—	ns

Load Circuit



CL = 100 pF (including jig capacitance)

Note: Values for t_{DD} and t_{DHR} are measured after adding a load circuit like the one shown on the right.

● PRECATIONS FOR DESIGNING

When designing your system, please take the following precautions.

(1) Operation of this product is guaranteed when supply voltage V_{DD} = 1.8 to 5.5 V. If V_{DD} is set to the V_{SS} level or open (cut off), operation is not guaranteed.
(2) Operation of the product is guaranteed with supply voltage V_{DD} on. Power must not be set to off.
(3) After power is cut off, completely discharging the capacitors takes time. The capacitors retain middle voltage levels V1 to V4 used to drive the display. Thus, occasionally, voltage may be instantaneously output to the segment pins (SEG1 to 80) or common pins (COM1 to 18), lighting the display.
(4) To cut power off (0 V or open), set T6K17 as follows:
1 : Set all data in display RAM to 0.
2 : Set to PUMP OFF.
3 : Allow enough discharging time. (1 sec or more)
4 : Cut power off.

Even if the above steps are taken, the phenomenon described in (3) may occur. Please configure an adequate system and evaluate it carefully.

● PRECAUTIONS WHEN USED IN COMBINATION WITH LCD PANEL

When using the device in combination with an LCD panel, please take the following precautions.
In general, the lit voltage Vop of the LCD panel and the lit voltage V4 of the device are subject to variations in manufacture. When the worst possible voltages are combined, the display may be lighter or darker.
TOSHIBA recommends you check the display quality of actual displays as well as comparing Vop and V4 with standards. The worst possible combinations are as follows:
Vop (mix) −V4 (max): Display may be dark.
Vop (max) −V4 (min): Display may be light.
For V4 reference variation values, see the contrast values (CONT15 to CONT0) in Table 1.

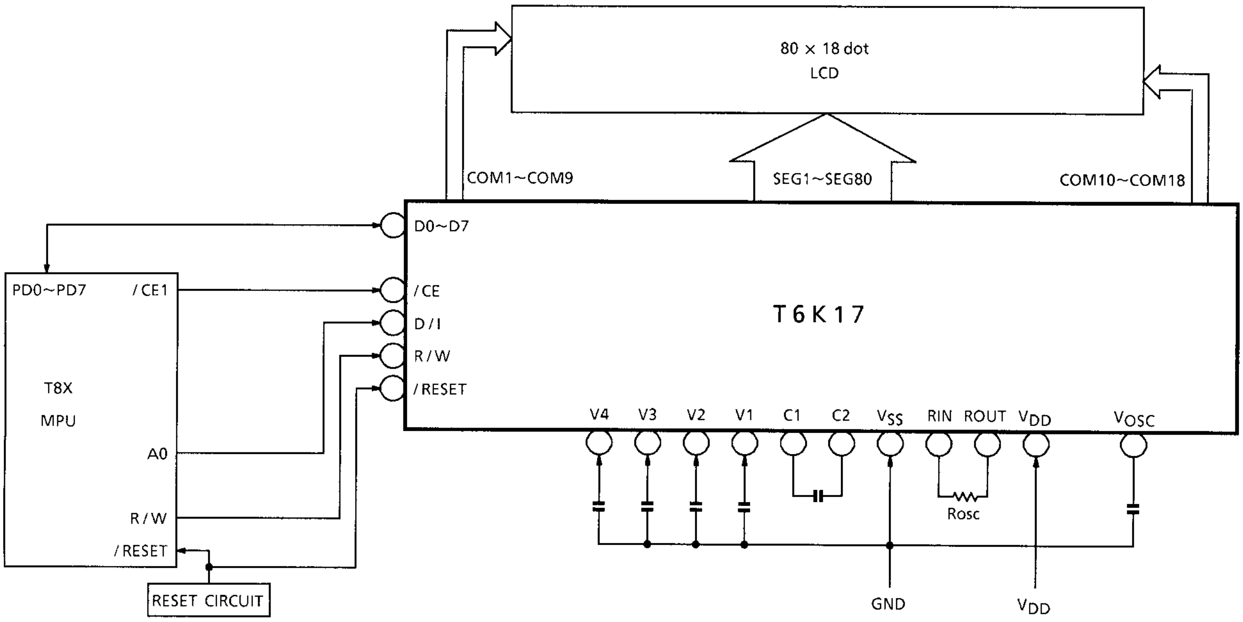
● INSTRUCTION FOR OPERATING CIRCUMSTANCES

If light is given to semiconductor devices, electromotive force is generated due to photoelectric effect, and they may malfunction.
Especially, devices whose dies are seen from outside are easily influenced. Please make sure with your design that external light does not come inside.
Please note semiconductors other than optical devices and EPROM may also be influenced.

Example of Application Circuit

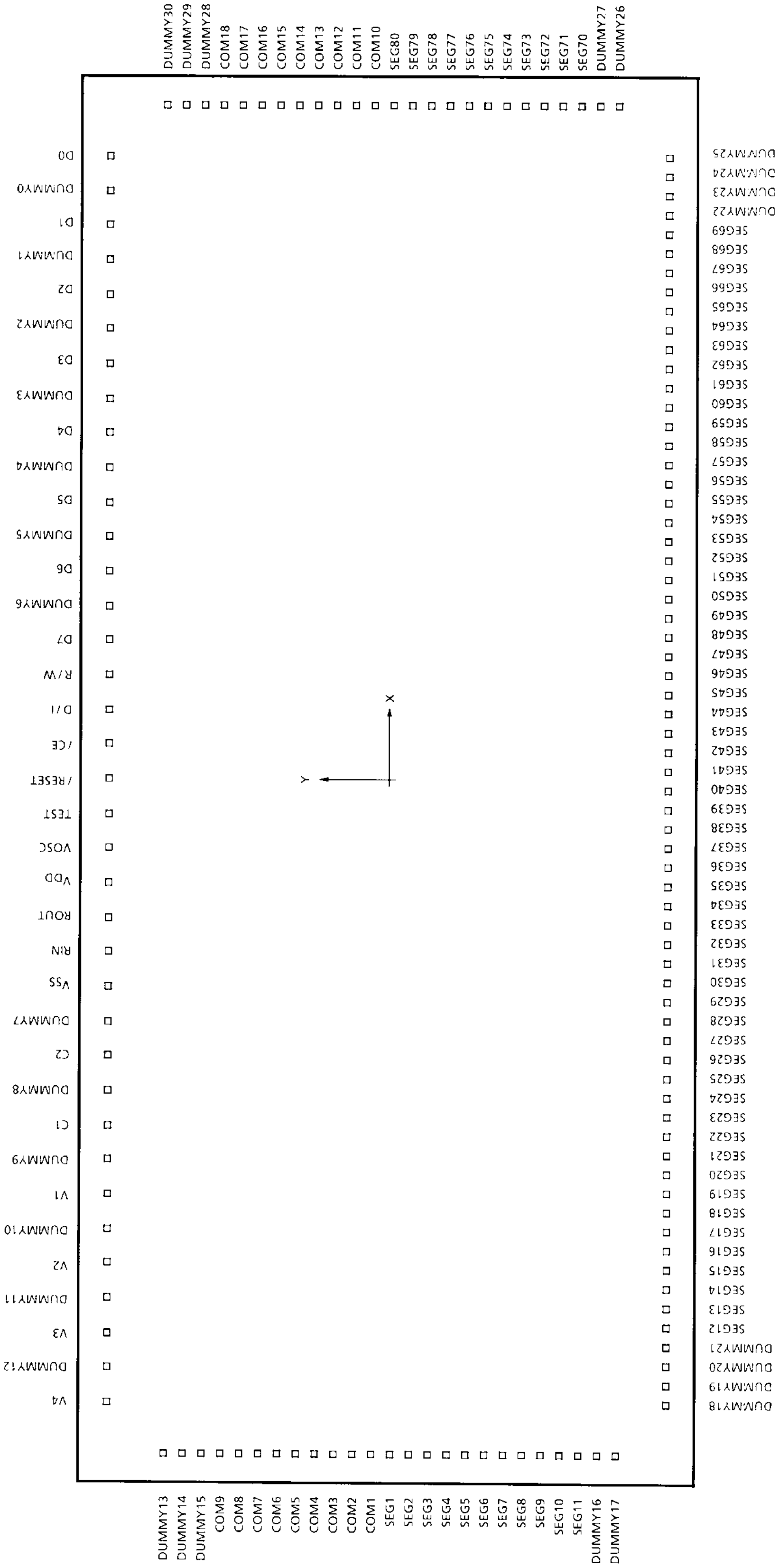
This application circuit for the T6K17 uses

- RC oscillator using an external resistor
- Using DC−DC converter (Quadrupler)



C = 0.1 μF (± 20%)
Rosc = 560 kΩ

Pad Layout


DUMMY30
DUMMY29
DUMMY28
COM18
COM17
COM16
COM15
COM14
COM13
COM12
COM11
COM10
SEG80
SEG79
SEG78
SEG77
SEG76
SEG75
SEG74
SEG73
SEG72
SEG71
SEG70
DUMMY27
DUMMY26
D0
DUMMY0
D1
DUMMY1
D2
DUMMY2
D3
DUMMY3
D4
DUMMY4
D5
DUMMY5
D6
DUMMY6
D7
R/W
D/I
/CE
/RESET
TEST
VOSC
VDD
ROUT
RIN
VSS
DUMMY7
C2
DUMMY8
C1
DUMMY9
V1
DUMMY10
V2
DUMMY11
V3
DUMMY12
V4
X
Y
DUMMY25
DUMMY24
DUMMY23
DUMMY22
SEG69
SEG68
SEG67
SEG66
SEG65
SEG64
SEG63
SEG62
SEG61
SEG60
SEG59
SEG58
SEG57
SEG56
SEG55
SEG54
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SEG52
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SEG33
SEG32
SEG31
SEG30
SEG29
SEG28
SEG27
SEG26
SEG25
SEG24
SEG23
SEG22
SEG21
SEG20
SEG19
SEG18
SEG17
SEG16
SEG15
SEG14
SEG13
SEG12
DUMMY21
DUMMY20
DUMMY19
DUMMY18
DUMMY13
DUMMY14
DUMMY15
COM9
COM8
COM7
COM6
COM5
COM4
COM3
COM2
COM1
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG8
SEG9
SEG10
SEG11
DUMMY16
DUMMY17

Pad Arrangement Diagram

Scribe width : (80 140) µm
Chip size : 6360 × 2540 µm
Chip thickness : 450 ± 50 µm

(µm)

No.	Pad Name	X Point	Y Point
1	D0	2880	1081
2	DUMMY0	2720	1081
3	D1	2560	1081
4	DUMMY1	2400	1081
5	D2	2240	1081
6	DUMMY2	2080	1081
7	D3	1920	1081
8	DUMMY3	1760	1081
9	D4	1600	1081
10	DUMMY4	1440	1081
11	D5	1280	1081
12	DUMMY5	1120	1081
13	D6	960	1081
14	DUMMY6	800	1081
15	D7	640	1081
16	R / W	480	1081
17	D / I	320	1081
18	/ CE	160	1081
19	/ RESET	0	1081
20	TEST	−160	1081
21	VOSC	−320	1081
22	V_{DD}	−528	1081
23	ROUT	−688	1081
24	RIN	−848	1081
25	V_{SS}	−1008	1081
26	DUMMY7	−1168	1081
27	C2	−1328	1081
28	DUMMY8	−1488	1081
29	C1	−1648	1081
30	DUMMY9	−1808	1081
31	V1	−1968	1081
32	DUMMY10	−2128	1081
33	V2	−2288	1081
34	DUMMY11	−2448	1081
35	V3	−2608	1081
36	DUMMY12	−2768	1081
37	V4	−2928	1081
38	DUMMY13	−3060	947
39	DUMMY14	−3060	867
40	DUMMY15	−3060	787
41	COM9	−3060	707
42	COM8	−3060	627
43	COM7	−3060	547
44	COM6	−3060	467
45	COM5	−3060	387
46	COM4	−3060	307
47	COM3	−3060	227
48	COM2	−3060	147
49	COM1	−3060	67
50	SEG1	−3060	−13
51	SEG2	−3060	−93
52	SEG3	−3060	−173
53	SEG4	−3060	−253
54	SEG5	−3060	−333
55	SEG6	−3060	−413
56	SEG7	−3060	−493

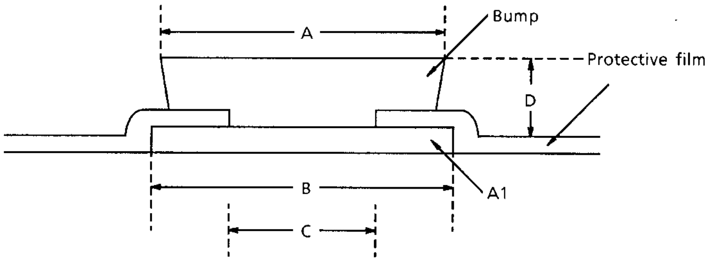
No.	Pad Name	X Point	Y Point
57	SEG8	−3060	−573
58	SEG9	−3060	−653
59	SEG10	−3060	−733
60	SEG11	−3060	−813
61	DUMMY16	−3060	−893
62	DUMMY17	−3060	−973
63	DUMMY18	−2893	−1116
64	DUMMY19	−2804	−1116
65	DUMMY20	−2715	−1116
66	DUMMY21	−2626	−1116
67	SEG12	−2537	−1116
68	SEG13	−2448	−1116
69	SEG14	−2359	−1116
70	SEG15	−2270	−1116
71	SEG16	−2181	−1116
72	SEG17	−2092	−1116
73	SEG18	−2003	−1116
74	SEG19	−1914	−1116
75	SEG20	−1825	−1116
76	SEG21	−1736	−1116
77	SEG22	−1647	−1116
78	SEG23	−1558	−1116
79	SEG24	−1469	−1116
80	SEG25	−1380	−1116
81	SEG26	−1291	−1116
82	SEG27	−1202	−1116
83	SEG28	−1113	−1116
84	SEG29	−1024	−1116
85	SEG30	−935	−1116
86	SEG31	−846	−1116
87	SEG32	−757	−1116
88	SEG33	−668	−1116
89	SEG34	−579	−1116
90	SEG35	−490	−1116
91	SEG36	−401	−1116
92	SEG37	−312	−1116
93	SEG38	−223	−1116
94	SEG39	−134	−1116

No.	Pad Name	X Point	Y Point
95	SEG40	−45	−1116
96	SEG41	45	−1116
97	SEG42	134	−1116
98	SEG43	223	−1116
99	SEG44	312	−1116
100	SEG45	401	−1116
101	SEG46	490	−1116
102	SEG47	579	−1116
103	SEG48	668	−1116
104	SEG49	757	−1116
105	SEG50	846	−1116
106	SEG51	935	−1116
107	SEG52	1024	−1116
108	SEG53	1113	−1116
109	SEG54	1202	−1116
110	SEG55	1291	−1116
111	SEG56	1380	−1116
112	SEG57	1469	−1116
113	SEG58	1558	−1116
114	SEG59	1647	−1116
115	SEG60	1736	−1116
116	SEG61	1825	−1116
117	SEG62	1914	−1116
118	SEG63	2003	−1116
119	SEG64	2092	−1116
120	SEG65	2181	−1116
121	SEG66	2270	−1116
122	SEG67	2359	−1116
123	SEG68	2448	−1116
124	SEG69	2537	−1116
125	DUMMY22	2626	−1116
126	DUMMY23	2715	−1116
127	DUMMY24	2804	−1116
128	DUMMY25	2893	−1116
129	DUMMY26	3060	−973
130	DUMMY27	3060	−893
131	SEG70	3060	−813
132	SEG71	3060	−733

No.	Pad Name	X Point	Y Point
133	SEG72	3060	−653
134	SEG73	3060	−573
135	SEG74	3060	−493
136	SEG75	3060	−413
137	SEG76	3060	−333
138	SEG77	3060	−253
139	SEG78	3060	−173
140	SEG79	3060	−93
141	SEG80	3060	−13
142	COM10	3060	67
143	COM11	3060	147
144	COM12	3060	227
145	COM13	3060	307
146	COM14	3060	387
147	COM15	3060	467
148	COM16	3060	547
149	COM17	3060	627
150	COM18	3060	707
151	DUMMY28	3060	787
152	DUMMY29	3060	867
153	DUMMY30	3060	947

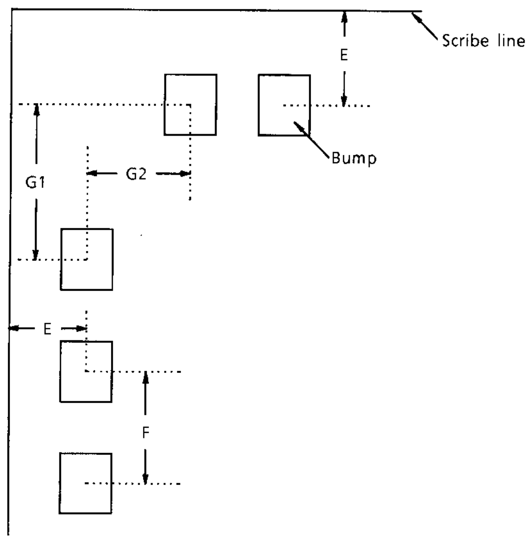
Shape of Bump Chip

1. Au bump shape



	Characteristics	Ratings
1	A (Bump size)	53 to 77 μm 65 μm (typ.)
2	B (A1 size)	70 μm (typ.)
3	C (Protective film aperture size)	35 μm (typ.)
4	D (Bump height)	16 μm (typ.) 12 to 20 μm
5	Gold bump height variation per chip	± 4 μm
6	Gold bump strength (Adhesive strength)	≥ 20 g
7	Gold bump hardness	30 to 80 HV (Vickers hardness tester)

2. Bump layout



	Characteristics	Ratings
8	E Bump center to scribe line distance	min 80 μm
9	F Bump pitch	min 80 μm
10	G Corner pad arrangement (either G1 or G2)	min 130 μm

RESTRICTIONS ON PRODUCT USE

000707EBE

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
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- Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do , that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.
- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.
  This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
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