Ordering number : EN*A1127A

Preliminary

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

STK672-430A-E — Thick-Film Hybrid IC 2-phase Stepping Motor Driver

Overview

The STK672-430A-E is a hybrid IC for use as a unipolar, 2-phase stepping motor driver with PWM current control.

Applications

- Office photocopiers, printers, etc.

Features

- Built-in overcurrent detection function (output current OFF).
- Built-in overheat detection function (output current OFF).
- If either over-current or overheat detection function is activated, the FAULT1 signal (active low) is output. The FAULT2 signal is used to output the result of activation of protection circuit detection at 2 levels.
- Built-in power on reset function.
- A micro-step sine wave-driven driver can be activated merely by inputting an external clock.
- External pins can be used to select 2, 1-2 (including pseudo-micro), W1-2, 2 W1-2, or 4W1-2 excitation.
- The switch timing of the 4-phase distributor can be switched by setting an external pin (MODE3) to detect either the rise and fall, or rise only, of CLOCK input.
- Phase is maintained even when the excitation mode is switched. Rotational direction switching function.
- Supports schmitt input for 2.5V high level input.
- Incorporating a current detection resistor (0.152Ω: resistor tolerance ±2%), motor current can be set using two external resistors.
- The ENABLE pin can be used to cut output current while maintaining the excitation mode.
- With a wide current setting range, power consumption can be reduced during standby.
- No motor sound is generated during hold mode due to external excitation current control.
- A external excitation system is used for PWM operations. Fixed current control for shifting the phase of Ach/Bch is used for the PWM phase.

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage 1	V_{CC} max	No signal	52	V
Maximum supply voltage 2	V_{DD} max	No signal	-0.3 to +6.0	V
Input voltage	V_{IN} max	Logic input pins	-0.3 to +6.0	V
Output current 1	I_{OP} max	10μs, 1 pulse (resistance load)	10	A
Output current 2	I_{OH} max	V_{DD}=5V, CLOCK≥200Hz	2.5	A
Allowable power dissipation 1	PdMF max	With an arbitrarily large heat sink. Per MOSFET	7.3	W
Allowable power dissipation 2	PdPK max	No heat sink	3.1	W
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=25°C

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage 1	V_{CC}	With signals applied	10 to 42	V
Operating supply voltage 2	V_{DD}	With signals applied	5±5%	V
Input high voltage	V_{IH}	Pins 10, 11, 12, 13, 14, 15, 17	2.5 to V_{DD}	V
Input low voltage	V_{IL}	Pins 10, 11, 12, 13, 14, 15, 17	0 to 0.8	V
Output current	I_{OH}	Tc=105°C, CLOCK≥200Hz	2.0	A
CLOCK frequency	f_{CL}	Minimum pulse width: at least 10μs	0 to 50	kHz
Phase driver withstand voltage	V_{DSS}	I_D=1mA (Tc=25°C)	100min	V
Recommended operating substrate temperature	Tc	No condensation	0 to 105	°C
Recommended Vref range	Vref	Tc=105°C	0.14 to 1.48	V

Electrical Characteristics at Tc=25°C, V_{CC}=24V, V_{DD}=5.0V *1

Parameter		Symbol	Conditions	min	typ	max	unit
V_{DD} supply current		I_{CCO}	V_{DD}=5.0V, ENABLE=Low		5.7	7.0	mA
Output average current *2		Ioave	R/L=1Ω/0.62mH in each phase	0.19	0.23	0.27	A
FET diode forward voltage		Vdf	If=1A (R_L=23Ω)		1	1.6	V
Output saturation voltage		Vsat	R_L=23Ω		0.35	0.50	V
Control input pin	Input voltage	V_{IH}	Pins 10, 11, 12, 13, 14, 15, 17	2.5		V_{DD}	V
		V_{IL}	Pins 10, 11, 12, 13, 14, 15, 17	-0.3		0.8	V
	5V level input current	I_{ILH}	Pins 10, 11, 12, 13, 14, 15, 17=5V		50	75	μA
	GND level input current	I_{ILL}	Pins 10, 11, 12, 13, 14, 15, 17=GND			10	μA
Vref input bias current		I_{IB}	Pin 19 =1.0V		10	15	μA
FAULT1 pin	Output low voltage	V_{OLF}	Pin 16 (I_O=5mA)		0.25	0.5	V
	5V level leakage current	I_{ILF}	Pin 16 =5V			10	μA
FAULT2 pin	Overcurrent detection output voltage	$V_{OF}2$	Pin 8 (when all protection functions have been activated)	2.4	2.5	2.6	V
	Overheat detection output voltage	$V_{OF}3$		3.1	3.3	3.5	
Overheat detection temperature		TSD	Design guarantee		144		°C
PWM frequency		fc		41	48	55	kHz

Notes

*1: A fixed-voltage power supply must be used.

*2: The value for Ioave assumes that the lead frame of the product is soldered to the mounting circuit board.

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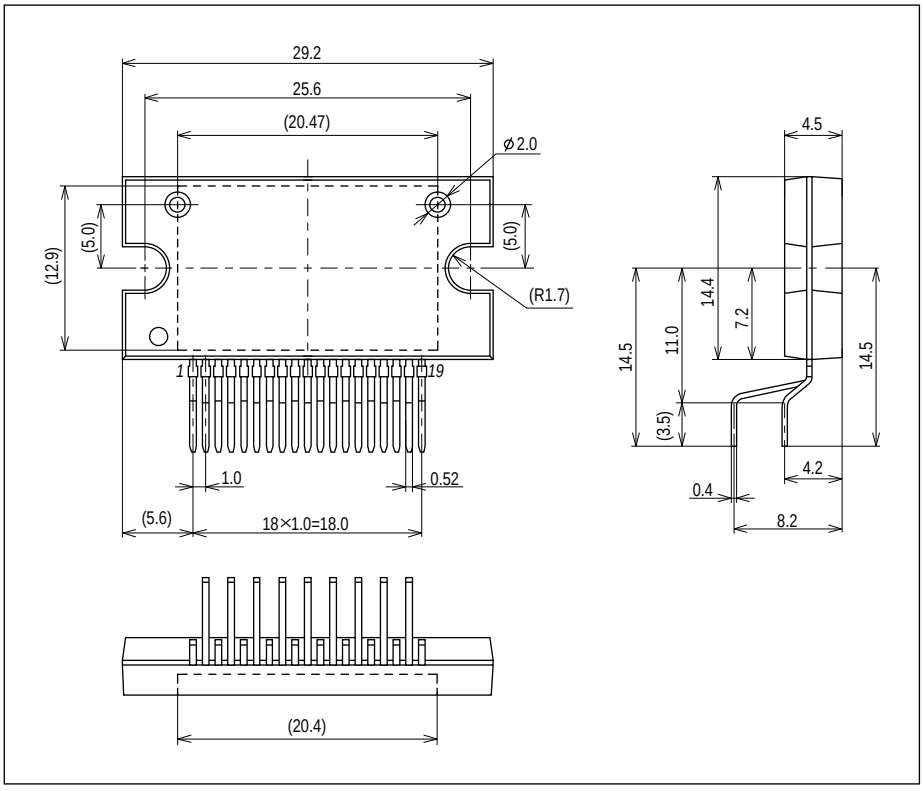
Parameter					Symbol	Conditions	min	typ	max	unit
A•B Chopper Current Ratio	4W1-2	2W1-2	W1-2	1-2	Vref *3	θ=15/16, 16/16		100		%
	4W1-2	2W1-2				θ=14/16		97		
	4W1-2					θ=13/16		95		
	4W1-2	2W1-2	W1-2			θ=12/16		93		
	4W1-2					θ=11/16		87		
	4W1-2	2W1-2				θ=10/16		83		
	4W1-2					θ=9/16		77		
	4W1-2	2W1-2	W1-2	1-2		θ=8/16		71		
	4W1-2					θ=7/16		64		
	4W1-2	2W1-2				θ=6/16		55		
	4W1-2					θ=5/16		47		
	4W1-2	2W1-2	W1-2			θ=4/16		40		
	4W1-2					θ=3/16		30		
	4W1-2	2W1-2				θ=2/16		20		
	4W1-2					θ=1/16		11		
	2							100		

Notes

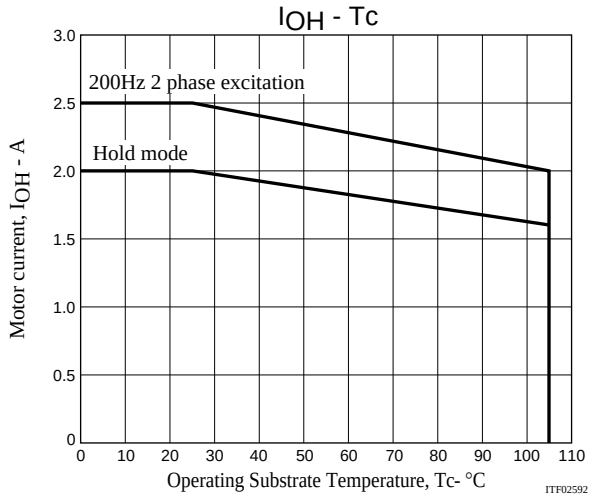
*3: The values given for Vref are design targets, no measurement is performed.

Package Dimensions

unit:mm (typ)



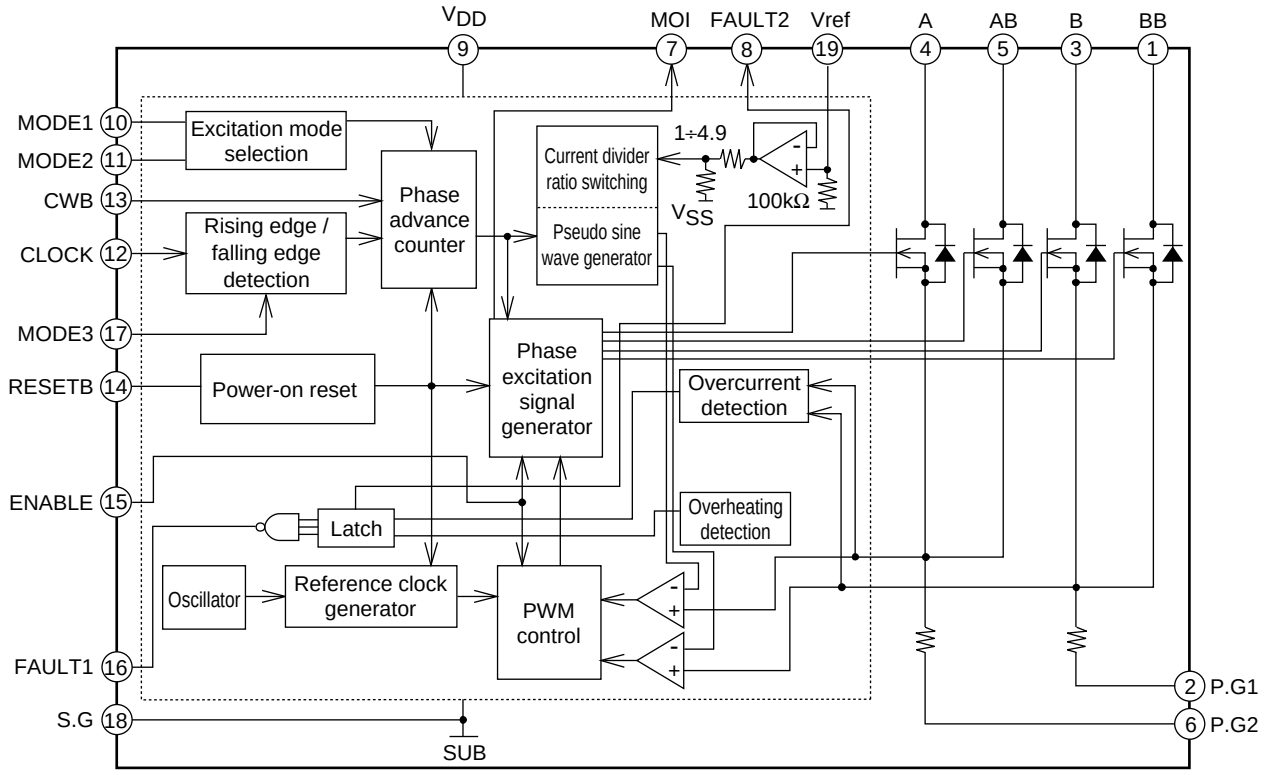
Derating Curve of Motor Current, I_{OH}, vs. STK672-430A-E Operating Substrate Temperature, Tc



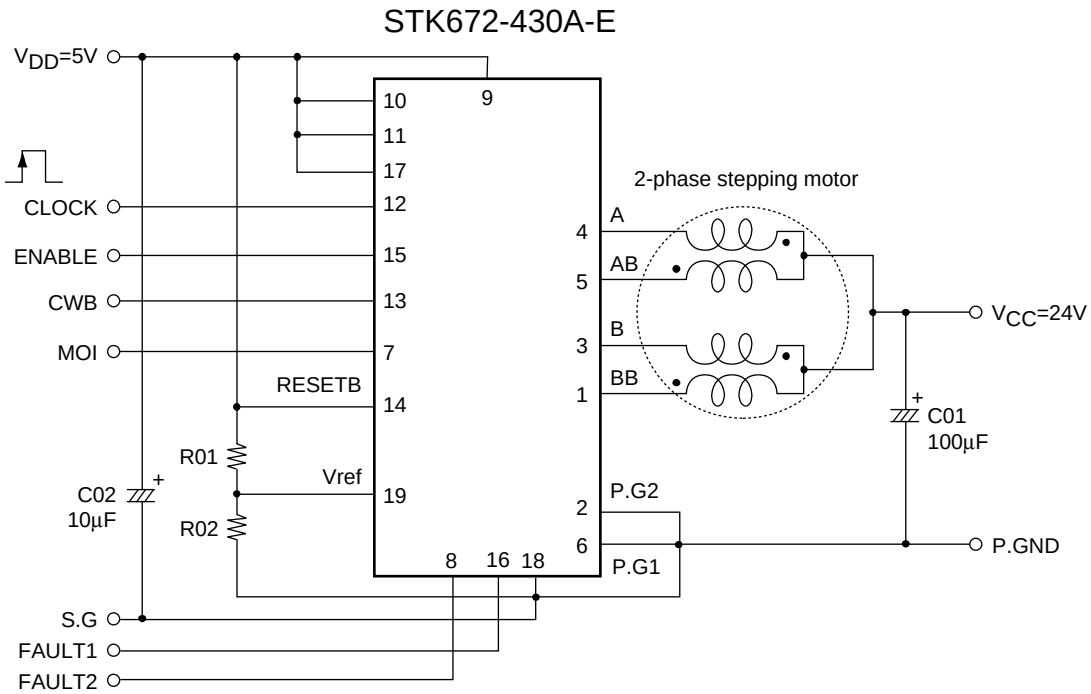
Notes

- The current range given above represents conditions when output voltage is not in the avalanche state.
- If the output voltage is in the avalanche state, see the allowable avalanche energy for STK672-4** series hybrid ICs given in a separate document.
- The operating substrate temperature, Tc, given above is measured while the motor is operating.
  Because Tc varies depending on the ambient temperature, Ta, the value of I_{OH}, and the continuous or intermittent operation of I_{OH}, always verify this value using an actual set.

Block Diagram



Sample Application Circuit



Precautions

[GND wiring]

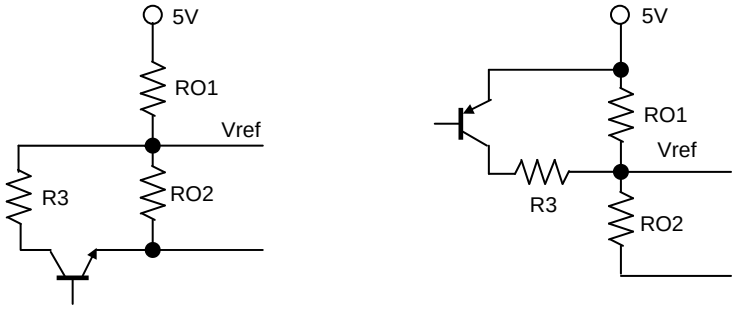
- To reduce noise on the 5V/24V system, be sure to place the GND of C01 in the circuit given above as close as possible to Pin 2 and Pin 6 of the hybrid IC.
  In addition, in order to set the current accurately, the GND side of RO2 of Vref must be connected to the shared ground terminal used by the Pin 18 (S.G) GND, P.G1 and P.G2.

[Input pins]

- When V_{DD} is being input, for each input pin, measures must be taken so that a negative voltage less than -0.3V is not applied to Pin 18. Measures must also be taken so that a voltage equal to or greater than V_{DD} is not input.
- High voltage input other than V_{DD}, MOI, FAULT1, and FAULT2 is 2.5V.
- Pull-up resistors are not connected to input pins. Pull-down resistors are attached. When controlling the input to the hybrid IC with the open collector type, be sure to connect a pull-up resistor (1 to 20kΩ).
  Be sure to use a device (0.8V or less, low level, when I_{OL}=5mA) for the open collector driver at this time that has an output voltage specification such that voltage is pulled to less than 0.8V at low level.
- When using the power on reset function built into the hybrid IC, be sure to directly connect Pin 14 to V_{DD}.
- We recommend attaching a 1,000pF capacitor to each input to prevent malfunction during high-impedance input. Be sure to connect the capacitor near the hybrid IC, between Pin 18 (S, G).
  When input is fixed low, directly connect to Pin 18. When input is fixed high, directly connect to V_{DD}.

[Current setting Vref]

- We recommend a resistance of 1kΩ or less for RO2 to reduce the effect of input bias current to the Vref pin.
- If the motor current is temporarily reduced, the circuit given below is recommended.
  The variable voltage range of Vref input is 0.14 to 1.48V.



[Setting the motor current]

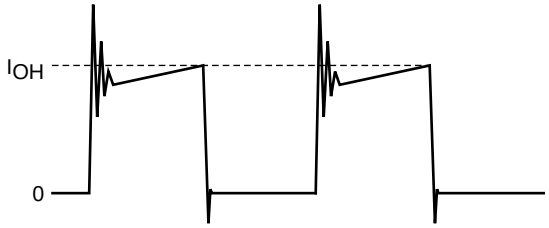
The motor current, I_{OH}, is set using the Pin 19 voltage, Vref, of the hybrid IC. Equations related to I_{OH} and Vref are given below.

$$Vref \approx (RO2 \div (RO2+RO1)) \times V_{DD}(5V) \quad \cdots\cdots (1)$$

$$I_{OH} \approx (Vref \div 4.9) \div Rs \quad \cdots\cdots (2)$$

The value of 4.9 in Equation (2) above represents the Vref voltage as divided by a circuit inside the control IC.
Rs: 0.152Ω (Current detection resistor inside the hybrid IC)

• Motor current peak value I_{OH} setting



[Smoke Emission Precuations]
If Pin 18 (S.G terminal) is attached to the PCB without using solder, overcurrent may flow into the MOSFET at V_{CC}ON (24V ON), causing the STK672-430A-E to emit smoke because 5V circuits cannot be controlled.
In addition, as long as one of the output Pins, 1, 3, 4, or 5, is open, inductance energy stored in the motor results in electrical stress on the driver, possibly resulting in the emission of smoke.

Function Table

M2	0	0	1	1	CLOCK Edge Timing for Phase Switching
M1 / M3	0	1	0	1	
1	2-phase excitation selection	1-2-phase excitation (I_{OH}=100%)	W1-2 phase excitation	2W1-2 phase excitation	CLOCK rising edge
0	1-2 phase excitation (I_{OH}=100%, 71%)	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	CLOCK both edges

I_{OH}=100% results in the Vref voltage setting, I_{OH}.
During 1-2 phase excitation, the hybrid IC operates at a current setting of I_{OH}=100% when the CLOCK signal rises. Conversely, pseudo micro current control is performed to control current at I_{OH}=100% or 71% at both edges of the CLOCK signal.

CWB pin

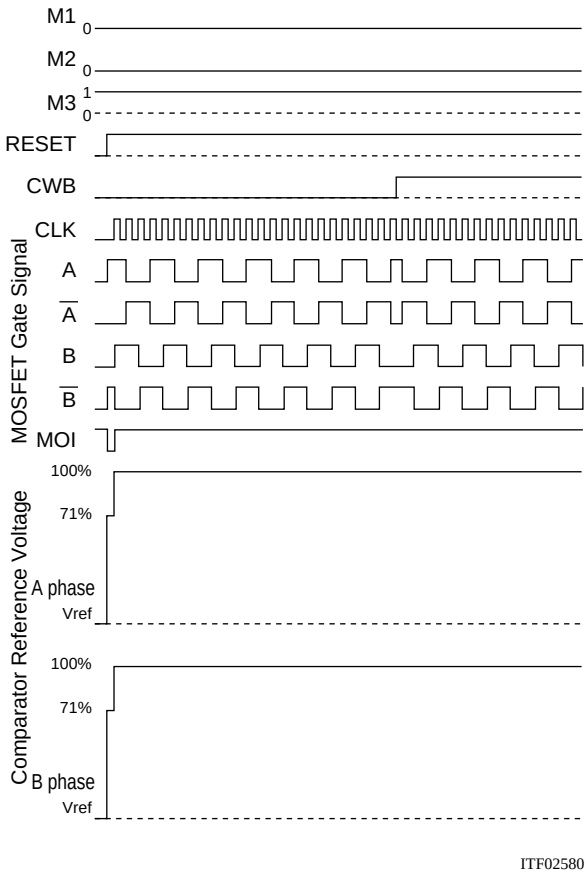
Forward/CW	0
Reverse/CCW	1

ENABLE • RESETB pin

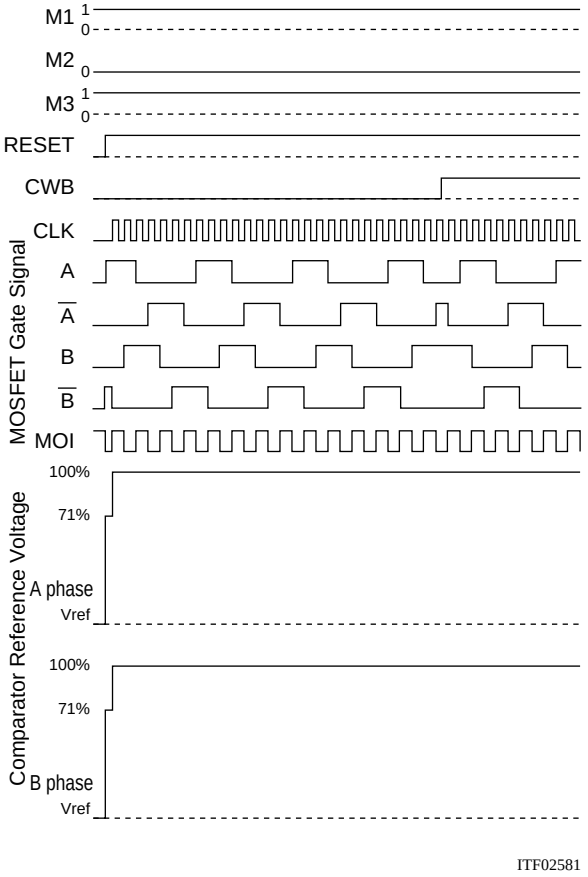
ENABLE	Motor current cut: Low
RESETB	Active Low

Timing Charts

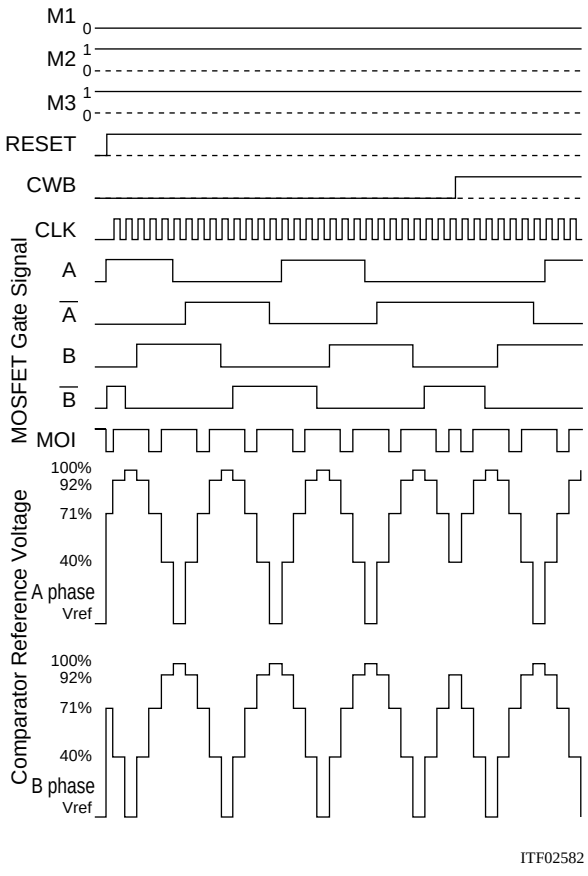
2-phase excitation timing charts (M3=1)



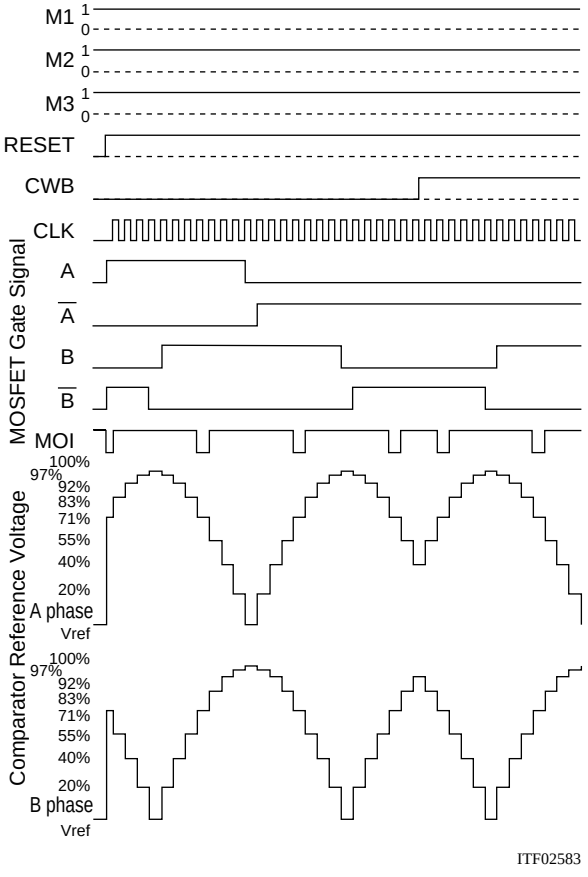
1-2-phase excitation timing charts (M3=1)



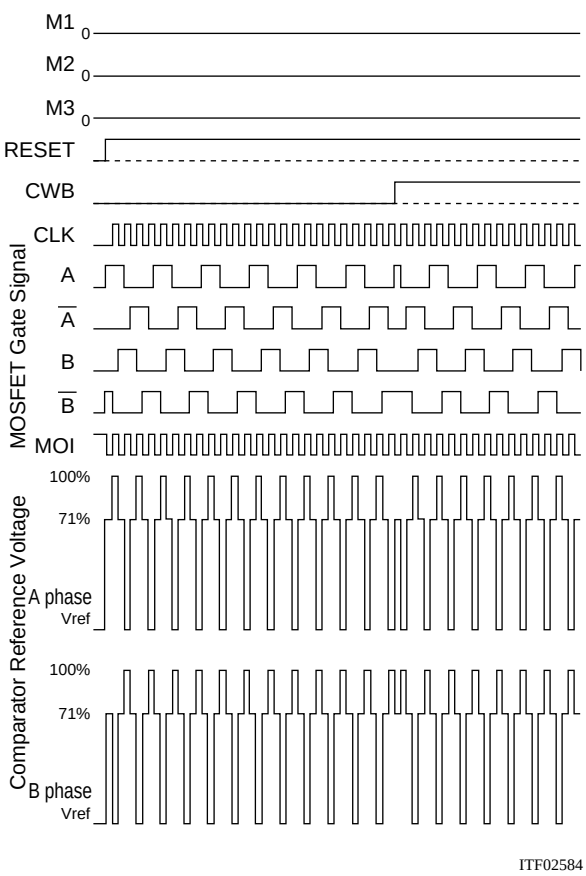
W1-2-phase excitation timing charts (M3=1)



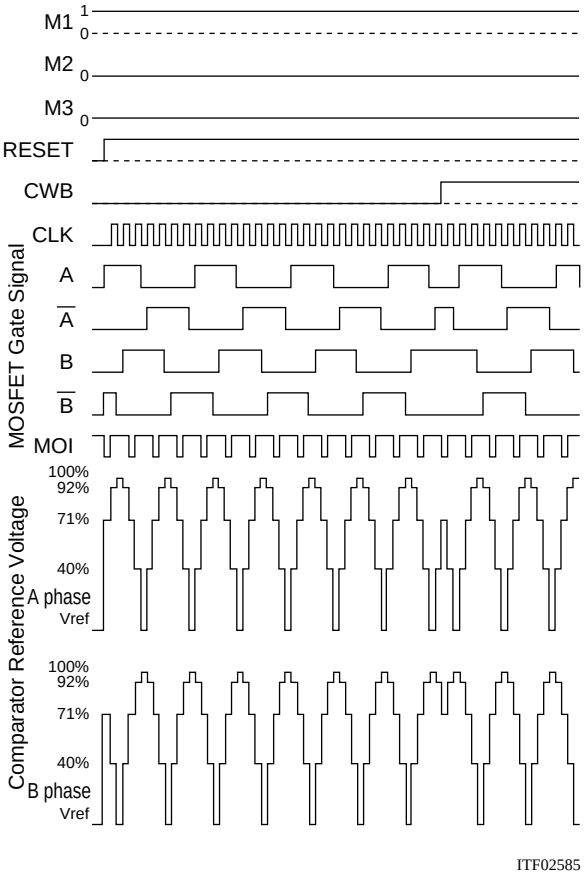
2W1-2-phase excitation timing charts (M3=1)



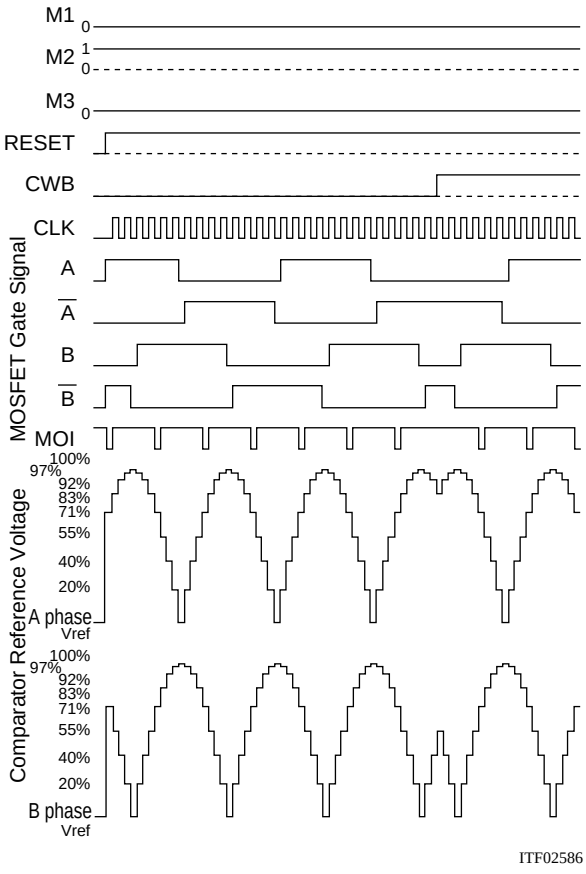
1-2-phase excitation timing charts (M3=0)



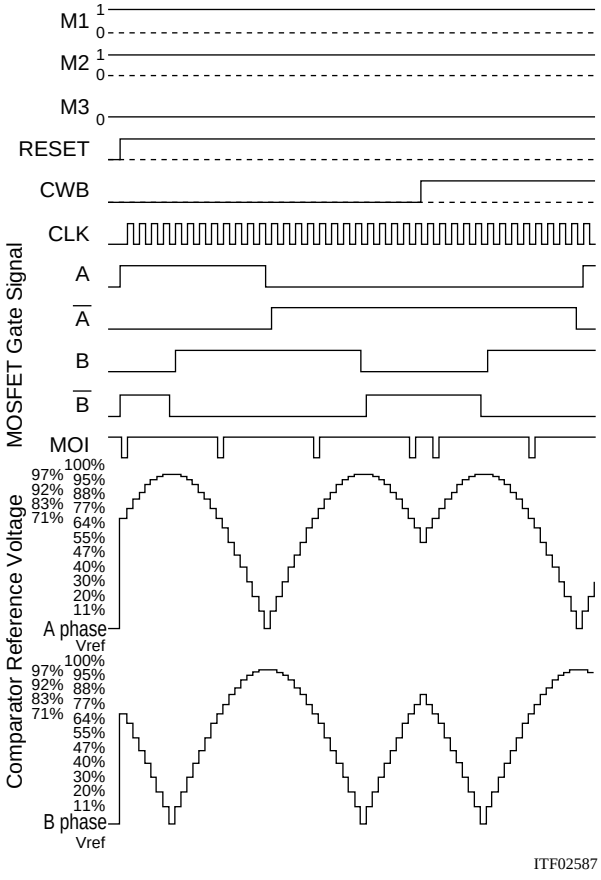
W1-2-phase excitation timing charts (M3=0)



2W1-2-phase excitation timing charts (M3=0)



4W1-2-phase excitation timing charts (M3=0)



Usage Notes

1. I/O Pins and Functions of the Control Block

[Pin description]

HIC pin	Pin Name	Function
7	MOI	Output pin for the excitation monitor
19	Vref	Current value setting
10	MODE1	Excitation mode selection
11	MODE2	
17	MODE3	
12	CLOCK	External CLOCK (motor rotation instruction)
13	CWB	Sets the direction of rotation of the motor axis
14	RESETB	System reset
15	ENABLE	Motor current OFF
16	FAULT1	Overcurrent/over-heat detection output
8	FAULT2	

Description of each pin

[CLOCK (Phase switching clock)]

Input frequency: DC-20kHz (when using both edges) or DC-50kHz (when using one edge)
Minimum pulse width: 20μs (when using both edges) or 10μs (when using one edge)
Pulse width duty: 40% to 50%
Both edge, single edge operation
M3:1 The excitation phase moves one step at a time at the rising edge of the CLOCK pulse.
M3:0 The excitation phase moves alternately one step at a time at the rising and falling edges of the CLOCK pulse.

[CWB (Motor direction setting)]

When CWB=0: The motor rotates in the clockwise direction.
When CWB=1: The motor rotates in the counterclockwise direction.
Do not allow CWB input to vary during the 7μs interval before and after the rising and falling edges of CLOCK input.

[ENABLE (Forcible OFF control of excitation drive output A, AB, B, and BB, and selecting operation/hold status inside the HIC)]

ENABLE=1: Normal operation
When ENABLE=0: Motor current goes OFF, and excitation drive output is forcibly turned OFF.
The system clock inside the HIC stops at this time, with no effect on the HIC even if input pins other than RESET input vary. In addition, since current does not flow to the motor, the motor shaft becomes free.
If the CLOCK signal used for motor rotation suddenly stops, the motor shaft may advance beyond the control position due to inertia. A SLOW DOWN setting where the CLOCK cycle gradually decreases is required in order to stop at the control position.

[MODE1, MODE2, and MODE3 (Selecting the excitation mode, and selecting one edge or both edges of the CLOCK)]

Excitation select mode terminal (See the sample application circuit for excitation mode selection), selecting the CLOCK input edge(s).
Mode setting active timing
Do not change the mode within 7μs of the input rising or falling edge of the CLOCK signal.

[RESETB (System-wide reset)]

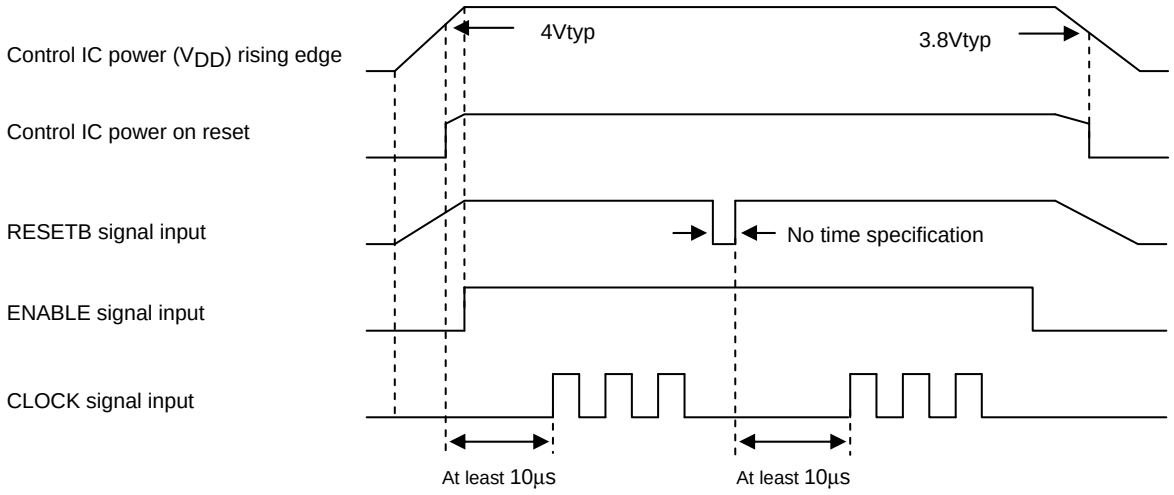
The reset signal is formed by the power-on reset function built into the HIC and the RESETB terminal.
When activating the internal circuits of the HIC using the power-on reset signal within the HIC, be sure to connect Pin 14 of the HIC to V_{DD}.

[Vref (Voltage setting to be used for the current setting reference)]

- Pin type: Analog input configuration, input pull-down resistor 100kΩ
  Input voltage is in the voltage range of 0.14V to 1.48V.

[Input timing]

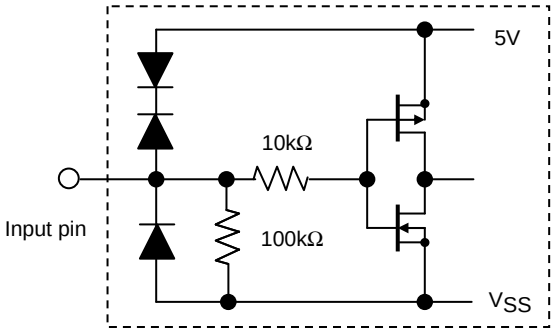
The control IC of the driver is equipped with a power on reset function capable of initializing internal IC operations when power is supplied. A 4V typ setting is used for power on reset. Because the specification for the MOSFET gate voltage is 5V±5%, conduction of current to output at the time of power on reset adds electromotive stress to the MOSFET due to lack of gate voltage. To prevent electromotive stress, be sure to set ENABLE=Low while V_{DD}, which is outside the operating supply voltage, is less than 4.75V.
In addition, if the RESETB terminal is used to initialize output timing, be sure to allow at least 10μs until CLOCK input.



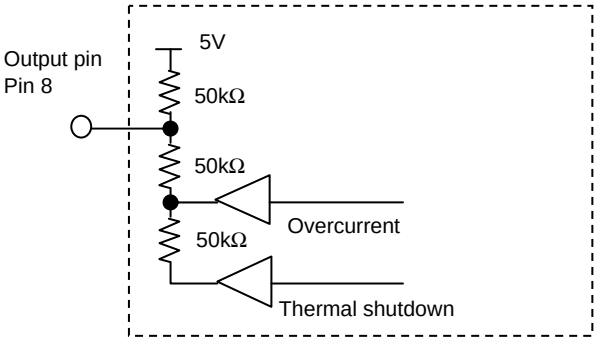
ENABLE, CLOCK, and RESETB Signals Input Timing

[Configuration of control block I/O pins]

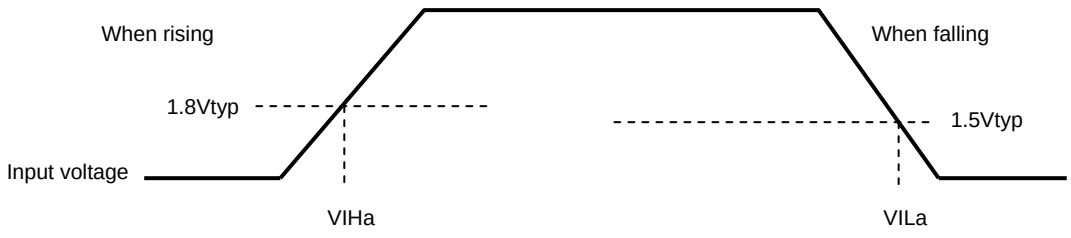
<Configuration of the MODE1, MODE2, MODE3, CLOCK, CWB, ENABLE, and RESETB input pins>



<Configuration of the FAULT2 pin>



The input pins of this driver all use Schmitt input. Typical specifications at Tc=25°C are given below. Hysteresis voltage is 0.3V (VIHa-VILa).

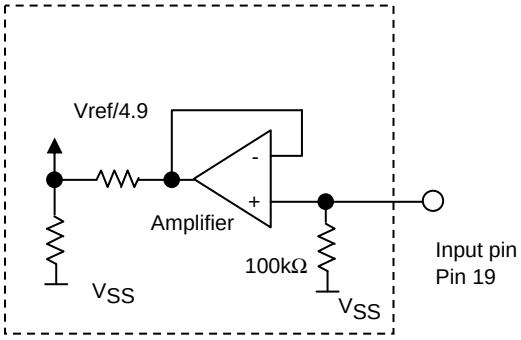


Input voltage specifications are as follows.

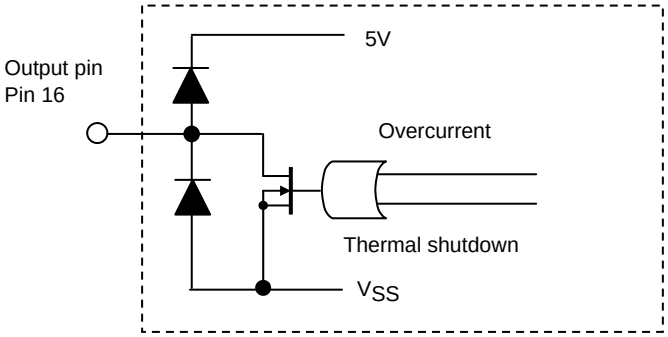
V_{IH}=2.5Vmin

V_{IL}=0.8Vmax

<Configuration of the Vref input pin>



<Configuration of the FAULT1 output pin>



(The buffer has an open drain configuration.)

<FAULT1, FAULT2 output>

FAULT1 Output

FAULT1 is an open drain output. Low is output if either overcurrent or overheating is detected.

FAULT2 output

Output is resistance divided (2 levels) and the type of abnormality detected is converted to the corresponding output voltage.

- Overcurrent: 2.5V(typ)
- Overheat: 3.3V(typ)

Abnormality detection can be released by a RESETB operation or turning V_{DD} voltage on/off.

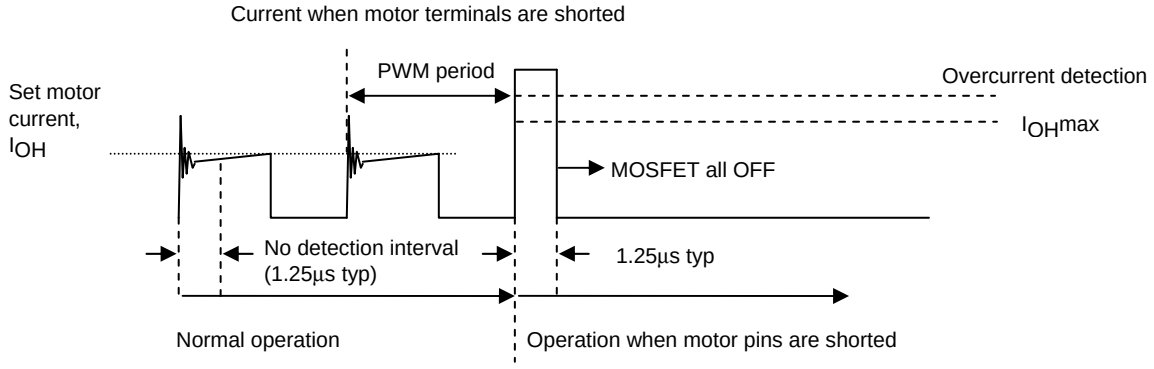
[MOI output]

The output frequency of this excitation monitor pin varies depending on the excitation mode. For output operations, see the timing chart.

2. Overcurrent Detection and Overheat Detection Functions of the STK672-430A-E and 440A-E

Each detection function operates using a latch system and turns output off. Because a RESET signal is required to restore output operations, once the power supply, V_{DD}, is turned off, you must either again apply power on reset with V_{DD}ON or apply a RESETB=High→Low→High signal.

[Overcurrent detection]
This hybrid IC is equipped with a function for detecting overcurrent that arises when the motor burns out or when there is a short between the motor terminals.
Overcurrent detection occurs at 3.4A typ with the STK672-430A-E and at 5.0A typ for the STK672-440A-E.



Overcurrent detection begins after an interval of no detection (a dead time of 1.25µs typ) during the initial ringing part during PWM operations. The no detection interval is a period of time where overcurrent is not detected even if the current exceeds I_{OH}.

[Overheat detection]
Rather than directly detecting the temperature of the semiconductor device, overheat detection detects the temperature of the aluminum substrate (144°C typ).
Within the allowed operating range recommended in the specification manual, if a heat sink attached for the purpose of reducing the operating substrate temperature, Tc, comes loose, the semiconductor can operate without breaking. However, we cannot guarantee operations without breaking in the case of operations other than those recommended, such as operations at a current exceeding I_{OH} max that occurs before overcurrent detection is activated.

3. STK672-430A-E Allowable Avalanche Energy Value

(1) Allowable Range in Avalanche Mode

When driving a 2-phase stepping motor with constant current chopping using an STK672-4** Series hybrid IC, the waveforms shown in Figure 1 below result for the output current, I_D, and voltage, V_{DS}.

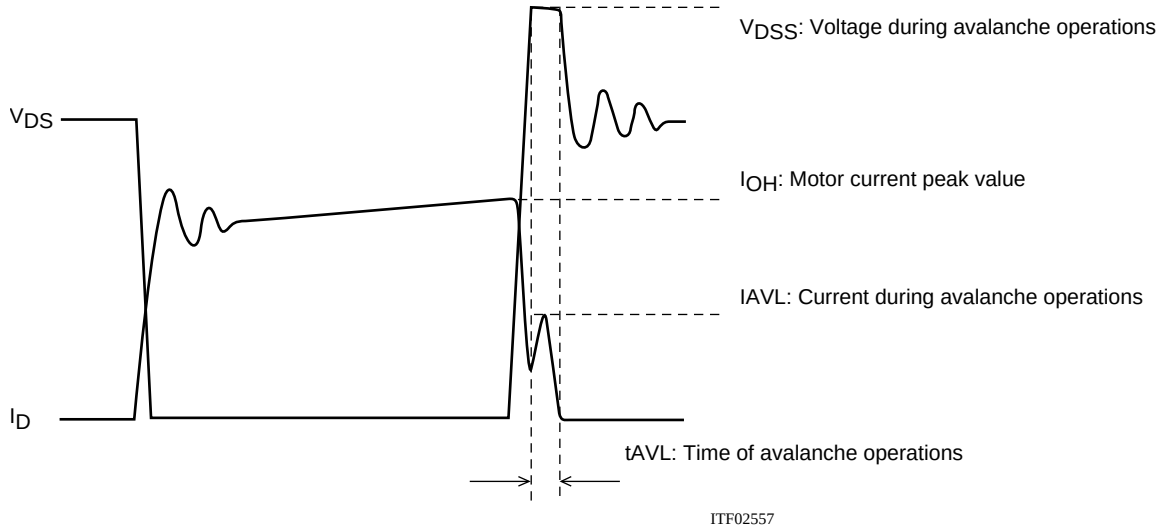


Figure 1 Output Current, I_D, and Voltage, V_{DS}, Waveforms 1 of the STK672-4** Series when Driving a 2-Phase Stepping Motor with Constant Current Chopping

When operations of the MOSFET built into STK672-4** Series ICs is turned off for constant current chopping, the I_D signal falls like the waveform shown in the figure above. At this time, the output voltage, V_{DS}, suddenly rises due to electromagnetic induction generated by the motor coil.

In the case of voltage that rises suddenly, voltage is restricted by the MOSFET V_{DSS}. Voltage restriction by V_{DSS} results in a MOSFET avalanche. During avalanche operations, I_D flows and the instantaneous energy at this time, EAVL1, is represented by Equation (3-1).

$$EAVL1=V_{DSS}\times IAVL\times 0.5\times tAVL \quad \text{---------- (3-1)}$$

V_{DSS}: V units, IAVL: A units, tAVL: sec units

The coefficient 0.5 in Equation (3-1) is a constant required to convert the IAVL triangle wave to a square wave.

During STK672-4** Series operations, the waveforms in the figure above repeat due to the constant current chopping operation. The allowable avalanche energy, EAVL, is therefore represented by Equation (3-2) used to find the average power loss, PAVL, during avalanche mode multiplied by the chopping frequency in Equation (3-1).

$$PAVL=V_{DSS}\times IAVL\times 0.5\times tAVL\times fc \quad \text{---------- (3-2)}$$

fc: Hz units (fc is set to the PWM frequency of 50kHz.)

For V_{DSS}, IAVL, and tAVL, be sure to actually operate the STK672-4** Series and substitute values when operations are observed using an oscilloscope.

Ex. If V_{DSS}=110V, IAVL=1A, tAVL=0.2μs when using a STK672-430A-E driver, the result is:

$PAVL=110\times 1\times 0.5\times 0.2\times 10^{-6}\times 50\times 10^{3}=0.55W$

V_{DSS}=110V is a value actually measured using an oscilloscope.

The allowable loss range for the allowable avalanche energy value, PAVL, is shown in the graph in Figure 3. When examining the avalanche energy, be sure to actually drive a motor and observe the I_D, V_{DSS}, and tAVL waveforms during operation, and then check that the result of calculating Equation (3-2) falls within the allowable range for avalanche operations.

(2) I_D and V_{DSS} Operating Waveforms in Non-avalanche Mode

Although the waveforms during avalanche mode are given in Figure 1, sometimes an avalanche does not result during actual operations.

Factors causing avalanche are listed below.

- Poor coupling of the motor's phase coils (electromagnetic coupling of A phase and AB phase, B phase and BB phase).
- Increase in the lead inductance of the harness caused by the circuit pattern of the P.C. board and motor.
- Increases in V_{DSS}, tAVL, and IAVL in Figure 1 due to an increase in the supply voltage from 24V to 36V.

If the factors above are negligible, the waveforms shown in Figure 1 become waveforms without avalanche as shown in Figure 2.

Under operations shown in Figure 2, avalanche does not occur and there is no need to consider the allowable loss range of PAVL shown in Figure 3.

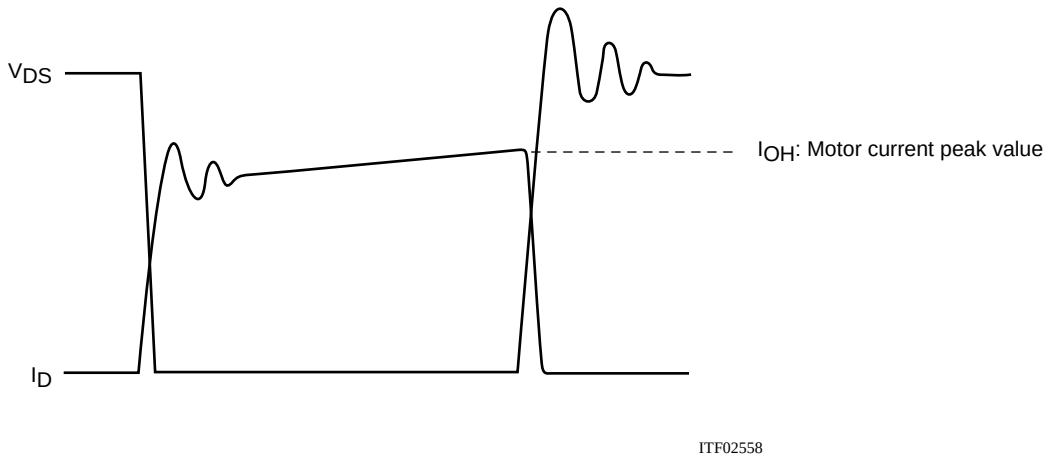
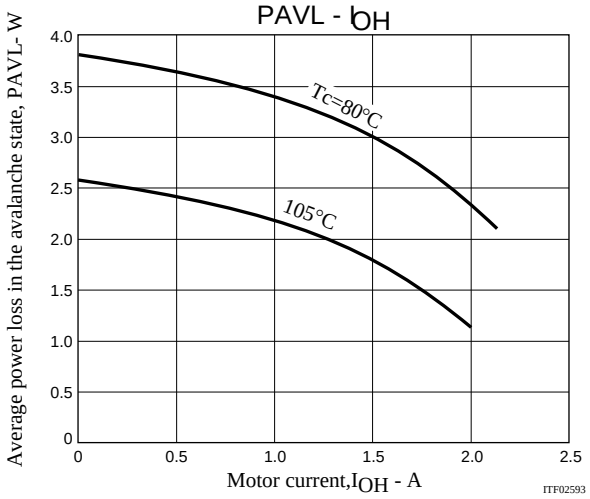


Figure 2 Output Current, I_D, and Voltage, V_{DS}, Waveforms 2 of the STK672-4** Series when Driving a 2-Phase Stepping Motor with Constant Current Chopping

Figure 3 Allowable Loss Range, PAVL-I_{OH} During STK672-430A-E Avalanche Operations



Note:

The operating conditions given above represent a loss when driving a 2-phase stepping motor with constant current chopping.

Because it is possible to apply 2.6W or more at I_{OH}=0A, be sure to avoid using the MOSFET body diode that is used to drive the motor as a zener diode.

4. Calculating STK672-430A-E HIC Internal Power Loss

The average internal power loss in each excitation mode of the STK672-430A-E can be calculated from the following formulas. *1

[Each excitation mode]
2-phase excitation mode
$2PdAVex = (Vsat+Vdf) \times 0.5 \times CLOCK \times I_{OH} \times t2 + 0.5 \times CLOCK \times I_{OH} \times (Vsat \times t1 + Vdf \times t3)$ ---------- (4-1)

1-2 Phase excitation mode
$1\text{-}2PdAVex = (Vsat+Vdf) \times 0.25 \times CLOCK \times I_{OH} \times t2 + 0.25 \times CLOCK \times I_{OH} \times (Vsat \times t1 + Vdf \times t3)$ ---------- (4-2)

W1-2 Phase excitation mode
$W1\text{-}2PdAVex = 0.64[(Vsat+Vdf) \times 0.125 \times CLOCK \times I_{OH} \times t2 + 0.125 \times CLOCK \times I_{OH} \times (Vsat \times t1 + Vdf \times t3)]$ ---------- (4-3)

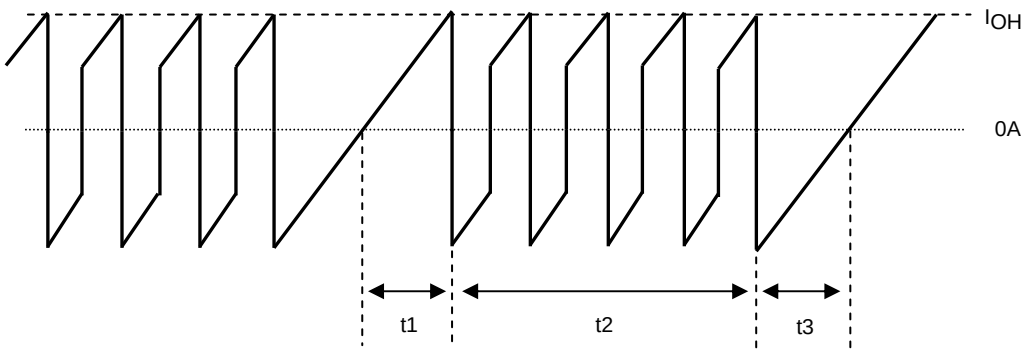
2W1-2 Phase excitation mode
$2W1\text{-}2PdAVex = 0.64[(Vsat+Vdf) \times 0.0625 \times CLOCK \times I_{OH} \times t2 + 0.0625 \times CLOCK \times I_{OH} \times (Vsat \times t1 + Vdf \times t3)]$ ------ (4-4)

4W1-2 Phase excitation mode
$4W1\text{-}2PdAVex = 0.64[(Vsat+Vdf) \times 0.0625 \times CLOCK \times I_{OH} \times t2 + 0.0625 \times CLOCK \times I_{OH} \times (Vsat \times t1 + Vdf \times t3)]$ ------ (4-5)

Motor hold mode
$HoldPdAVex = (Vsat+Vdf) \times I_{OH}$ ---------- (4-6)

Note: 2-phase 100% conductance is assumed in Equation (4-6).
Vsat: Combined voltage of Ron voltage drop + current detection resistance
Vdf: Combined voltage of the FET body diode + current detection resistance *1
CLOCK: Input CLOCK (HIC: input frequency at Pin 12)
*1 Although a synchronous rectification system is used, substitute using the value of Vdf, while taking design margins into account.

t1, t2, and t3 represent the waveforms shown in the figure below.
t1: Time required for the winding current to reach the set current (I_{OH})
t2: Time in the constant current control (PWM) region
t3: Time from end of phase input signal until inverse current regeneration is complete



Motor COM Current Waveform Model

$t1 = (-L/(R+0.35)) \ln (1-(((R+0.35)/V_{CC}) \times I_{OH}))$ ---------- (4-7)
$t3 = (-L/R) \ln ((V_{CC}+1)/(I_{OH} \times R + V_{CC}+1))$ ---------- (4-8)
V_{CC}: Motor supply voltage (V)
L: Motor inductance (H)
R: Motor winding resistance (Ω)
I_{OH}: Motor set output current crest value (A)

Fixed current control time, t2, for each excitation mode

(1) 2-phase excitation	t2 = (2÷CLOCK) - (t1 + t3) ·····(4-9)
(2) 1-2 phase excitation	t2 = (3÷CLOCK) - t1 ·····(4-10)
(3) W1-2 phase excitation	t2 = (7÷CLOCK) - t1 ·····(4-11)
(4) 2W1-2 phase excitation (and 4W1-2 phase excitation)	t2 = (15÷CLOCK) - t1 ·····(4-12)

For the values of Vsat and Vdf, be sure to substitute from Vsat vs I_{OH} and Vdf vs I_{OH} at the setting current value I_{OH}. (See pages to follow)
Then, determine if a heat sink is necessary by comparing with the ΔTc vs Pd graph (see next page) based on the calculated average output loss, HIC.
For heat sink design, be sure to see STK672-430A-E.
The HIC average power, PdAVex described above, represents loss when not in avalanche mode. To add the loss in avalanche mode, be sure to add PAVL (4-13, 14) using the formula (3-2) for average power loss , PAVL, for STK672-4** avalanche mode, described below to PdAVex described above.
When using this IC without a fin, always check for temperature increases in the set, because the HIC substrate temperature, Tc, varies due to effects of convection around the HIC.

[Calculating the average power loss, PAVL, during avalanche mode]
The allowable avalanche energy, EAVL, during fixed current chopping operation is represented by Equation (3-2) used to find the average power loss, PAVL, during avalanche mode that is calculated by multiplying Equation (3-1) by the chopping frequency.

$$PAVL=V_{DSS}\times IAVL\times 0.5\times tAVL\times fc \cdots\cdots (3\text{-}2)$$

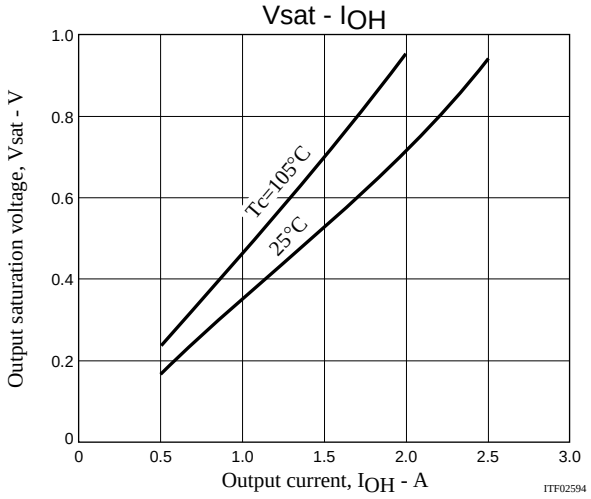
fc: Hz units (input MAX PWM frequency when using the STK672-4** series.)

Be sure to actually operate an STK672-4** series and substitute values found when observing operations on an oscilloscope for V_{DSS}, IAVL, and tAVL.

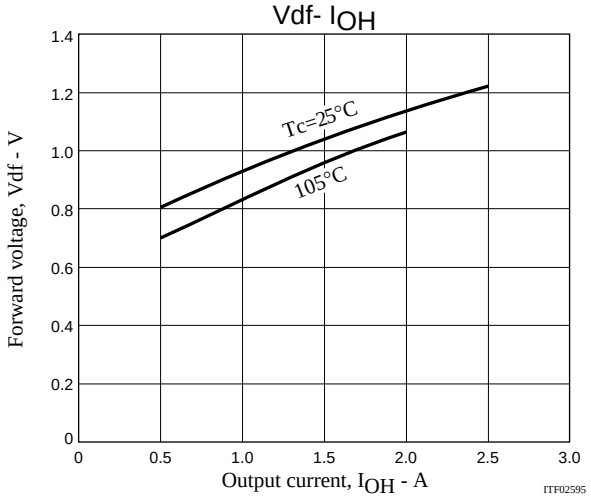
The sum of PAVL values for each excitation mode is multiplied by the constants given below and added to the average internal HIC loss equation, except in the case of 2-phase excitation.

1-2 excitation mode and higher: $PAVL(1)=0.7\times PAVL$ ·····(4-13)
During 2-phase excitation and motor hold: $PAVL(1)=1\times PAVL$ ·····(4-14)

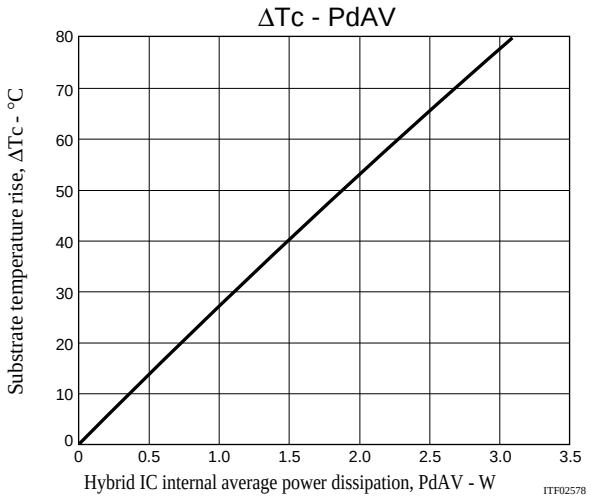
STK672-430A-E Output saturation voltage, Vsat - Output current, I_{OH}



STK672-430A-E Forward voltage, Vdf -Output current, I_{OH}



Substrate temperature rise, ΔTc (no heat sink) - Internal average power dissipation, PdAV



5. Thermal design

[Operating range in which a heat sink is not used]

Use of a heat sink to lower the operating substrate temperature of the HIC (Hybrid IC) is effective in increasing the quality of the HIC.

The size of heat sink for the HIC varies depending on the magnitude of the average power loss, PdAV, within the HIC. The value of PdAV increases as the output current increases. To calculate PdAV, refer to "Calculating Internal HIC Loss for the STK672-430A-E, STK672-440A-E" in the specification document.

Calculate the internal HIC loss, PdAV, assuming repeat operation such as shown in Figure 1 below, since conduction during motor rotation and off time both exist during actual motor operations,

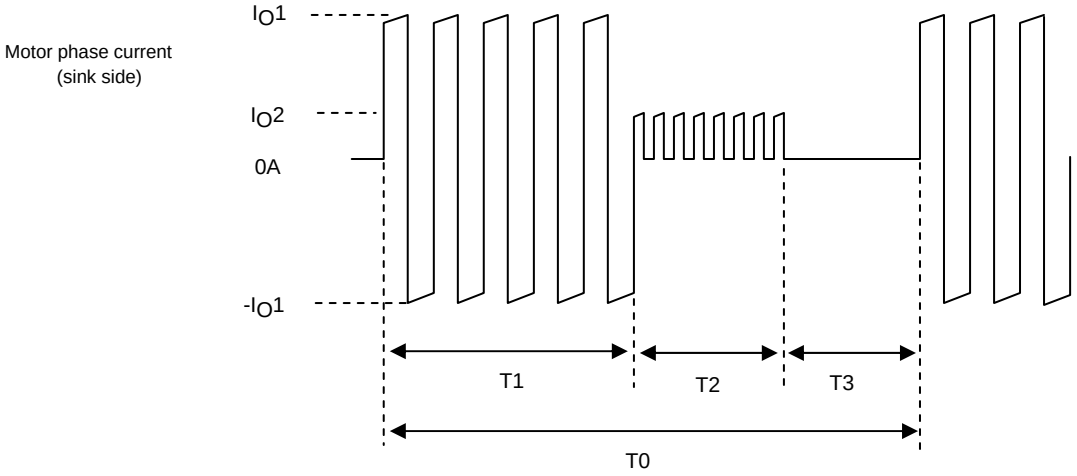


Figure 1 Motor Current Timing

T1: Motor rotation operation time
T2: Motor hold operation time
T3: Motor current off time
T2 may be reduced, depending on the application.
T0: Single repeated motor operating cycle
I_O1 and I_O2: Motor current peak values
Due to the structure of motor windings, the phase current is a positive and negative current with a pulse form.
Note that figure 1 presents the concepts here, and that the on/off duty of the actual signals will differ.
The hybrid IC internal average power dissipation PdAV can be calculated from the following formula.

PdAV= (T1×P1+T2×P2+T3×0) ÷TO ---------- (I)

(Here, P1 is the PdAV for I_O1 and P2 is the PdAV for I_O2)

If the value calculated using Equation (I) is 1.5W or less, and the ambient temperature, Ta, is 60°C or less, there is no need to attach a heat sink. Refer to Figure 2 for operating substrate temperature data when no heat sink is used.

[Operating range in which a heat sink is used]

Although a heat sink is attached to lower Tc if PdAV increases, the resulting size can be found using the value of θc-a in Equation (II) below and the graph depicted in Figure 3.

θc-a= (Tc max-Ta) ÷PdAV ---------- (II)

Tc max: Maximum operating substrate temperature =105°C

Ta: HIC ambient temperature

Although a heat sink can be designed based on equations (I) and (II) above, be sure to mount the HIC in a set and confirm that the substrate temperature, Tc, is 105°C or less.

The average HIC power loss, PdAV, described above represents the power loss when there is no avalanche operation. To add the loss during avalanche operations, be sure to add Equation (3-2), "Allowable STK672-4** Avalanche Energy Value", to PdAV.

Figure 2 Substrate temperature rise, ΔTc - Internal average power dissipation, PdAV

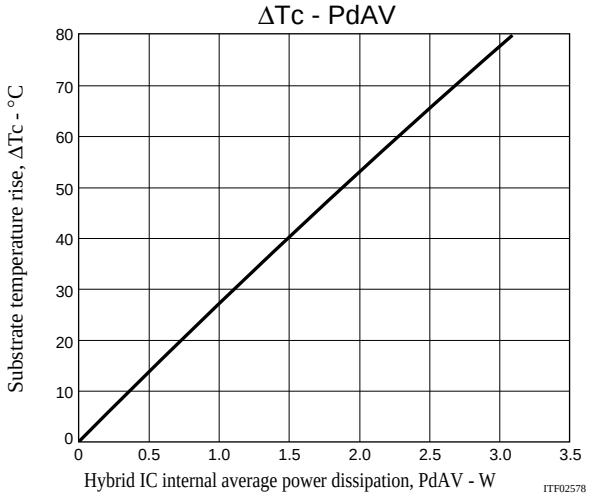
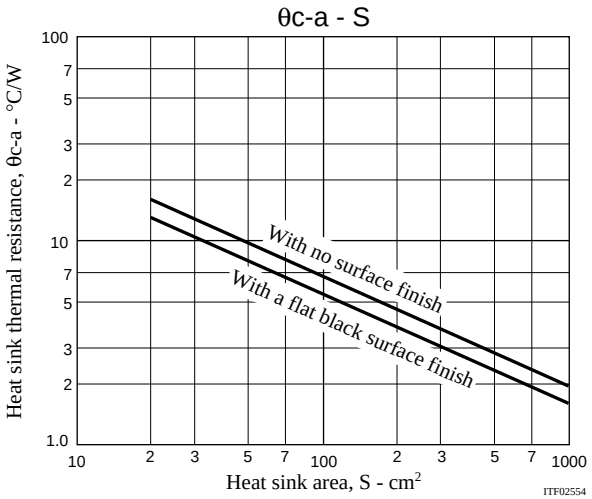


Figure 3 Heat sink area (Board thickness: 2mm) - θc-a



6. Mitigated Curve of Package Power Loss, PdPK, vs. Ambient Temperature, Ta

Package power loss, PdPK, refers to the average internal power loss, PdAV, allowable without a heat sink. The figure below represents the allowable power loss, PdPK, vs. fluctuations in the ambient temperature, Ta. Power loss of up to 3.1W is allowable at Ta=25°C, and of up to 1.75W at Ta=60°C.

Allowable power dissipation, PdPK (no heat sink) - Ambient temperature, Ta