

SANYO Semiconductors DATA SHEET

An ON Semiconductor Company

Thick-Film Hybrid IC **Unipolar Constant-current Chopper (external excitation** STK672-050-E — PWM) Circuit with Built-in Microstepping Controller

Stepping Motor Driver (sine wave drive) Output Current 3.0A (no heat sink*)

Overview

The STK672-050-E is a stepping motor driver hybrid IC that uses power MOSFETs in the output stage. It includes a builtin microstepping controller and is based on a unipolar constant-current PWM system. The STK672-050-E supports application simplification and standardization by providing a built-in 4 phase distribution stepping motor controller. It supports five excitation methods: 2 phase, 1-2 phase, W1-2 phase, 2W1-2 phase, and 4W1-2 phase excitations, and can provide control of the basic stepping angle of the stepping motor divided into 1/16 step units. It also allows the motor speed to be controlled with only a clock signal.

The use of this hybrid IC allows designers to implement systems that provide high motor torques, low vibration levels, low noise, fast response, and high-efficiency drive.

Applications

- Facsimile stepping motor drive (send and receive)
- Paper feed and optical system stepping motor drive in copiers
- Laser printer drum drive
- Printer carriage stepping motor drive
- X-Y plotter pen drive
- Other stepping motor applications

Note*: Conditions: $V_{CC1} = 24V$, $I_{OH} = 2.0A$, 2W1-2 excitation mode.

- Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.
- Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

Features

• Can implement stepping motor drive systems simply by providing a DC power supply and a clock pulse generator.

<Control Block Features>

- One of five drive types can be selected with the drive mode settings (M1, M2, and M3)
 - 1) 2 phase excitation drive
 - 2) 1-2 phase excitation drive
 - 3) W1-2 phase excitation drive
 - 4) 2W1-2 phase excitation drive
 - 5) 4W1-2 phase excitation drive
- Provides four freely selectable modes for the vector locus during microstepping drive: circular mode, one inside mode, and two outside modes.
- Phase retention even if excitation is switched.
- The excitation phase state can be verified in real time using the MO1, MO2, and MOI signal output pins.
- The CLK input counter block can be selected to be one of the following by the high/low setting of the M3 input pin.
 - 1) Rising edge only
 - 2) Both rising and falling edges
- The CLK and RETURN input pins include built-in malfunction prevention circuits for external pulse noise.
- ENABLE and $\overline{\text{RESET}}$ pins provided. These are Schmitt trigger inputs with built-in 20k Ω (typical) pull-up resistors.
- No noise generation due to the difference between the A and B phase time constants during motor hold since external excitation is used.
- Microstepping operation supported even for small motor currents, since the reference voltage Vref can be set to any value between 0V and 1/2V_{CC}2.

<Driver Block>

- External excitation PWM drive allows a wide operating supply voltage range (V_{CC}1 = 10 to 45V) to be used.
- Current detection resistor (0.2 Ω) built-in the hybrid IC itself.
- Power MOSFETs adopted for low drive loss.
- Provides a motor output drive current of $I_{OH} = 3.0A$.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V _{CC} 1 max	No signal	52	V
Maximum supply voltage 2	V _{CC} 2 max	No signal	-0.3 to +7.0	V
Input voltage	V _{IN} max	Logic input pins	-0.3 to +7.0	V
Output current	I _{OH} max	0.5s, 1 pulse, when V_{CC} 1 applied. Load: $R = 5\Omega$, $L = 10mH$ for each phase.	4.0	А
Repeated avalanche capacity	Ear max		38	mJ
Allowable power dissipation	Pd max	θc-a = 0	25	W
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V _{CC} 1	With signals applied	10 to 45	V
Supply voltage 2	V _{CC} ²	With signals applied	5 ± 5%	V
Input voltage	VIH		0 to V _{CC} 2	V
Phase driver withstand voltage	V _{DSS}	Tr1, 2, 3, and 4 (the A, \overline{A} , B, and \overline{B} outputs)	100 (min)	V
Output current	loн	Duty 50%	3.0	Α

STK672-050-E

Electrical Characteristics at Tc = 25°C, $V_{CC}1 = 24V$, $V_{CC}2 = 5V$

Doromotoro	Cumbala	Symbols Conditions		Rating			
Parameters	Symbols Conditions		min	nin typ		unit	
Control supply current	l _{CC}	Pin 7, with ENABLE pin held low.		4.5	15	mA	
Output saturation voltage	Vsat	$R_L = 7.5\Omega \ (I \approx 3A)$		1.4	2.6	V	
Average output current	loave	Load: R = 3.5Ω / L = 3.8 mH For each phase, Vref ≈ 0.6 V	0.45	0.50	0.55	Α	
FET diode forward voltage	Vdf	If = 1A		1.2	1.8	V	
[Control Inputs]		·					
	VIH	Except for the Vref pin	4			V	
Input voltage	V _{IL}	Except for the Vref pin			1	V	
	lн	Except for the Vref pin	0	1	10	μΑ	
Input current	I _{IL}	Except for the Vref pin	125	250	510	μΑ	
[Vref Input Pin]				'			
Input voltage	VI	Pin 8	0		2.5	V	
Input current	lı	Pin 8		1		μΑ	
[Control Outputs]				'			
	VOH	I = -3mA, pins MOI, MO1, MO2	2.4			V	
Output voltage	V _{OL}	I = +3mA, pins MOI, MO1, MO2			0.4	V	
[Current Distribution Ratio (A-B)]		•		'			
2W1-2, W1-2, 1-2	Vref	θ = 1/8		100		%	
2W1-2, W1-2	Vref	$\theta = 2/8$		92		%	
2W1-2	Vref	$\theta = 3/8$		83		%	
2W1-2, W1-2, 1-2	Vref	$\theta = 4/8$		71		%	
2W1-2	Vref	$\theta = 5/8$		55		%	
2W1-2, W1-2	Vref	$\theta = 6/8$		40		%	
2W1-2	Vref	θ = 7/8		20		%	
2	Vref			100		%	
PWM frequency	fc		37	47	57	kHz	

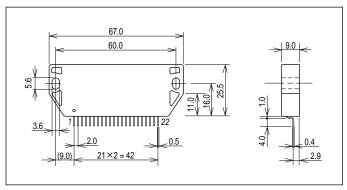
Note: A constant-voltage power supply must be used.

The design target value is shown for the current distribution ratio.

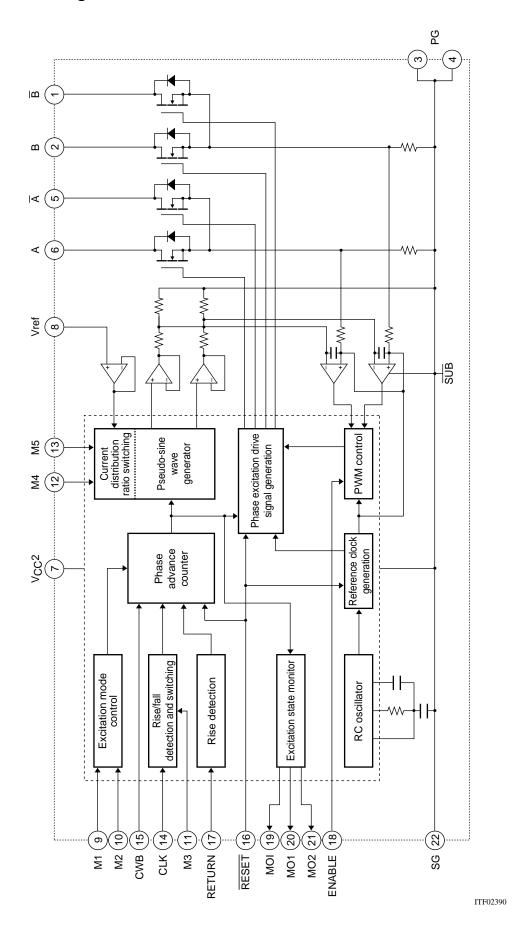
Package Dimensions

unit:mm (typ)

4164



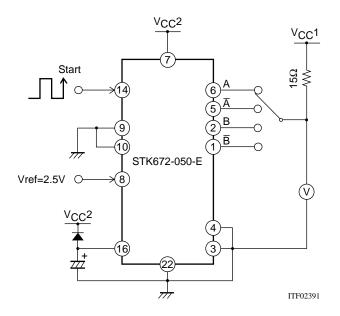
Internal Block Diagram

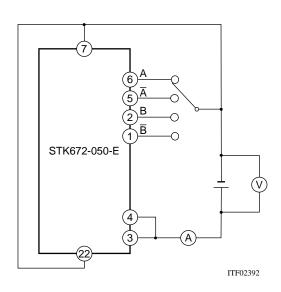


Test Circuit Diagrams

Vsat

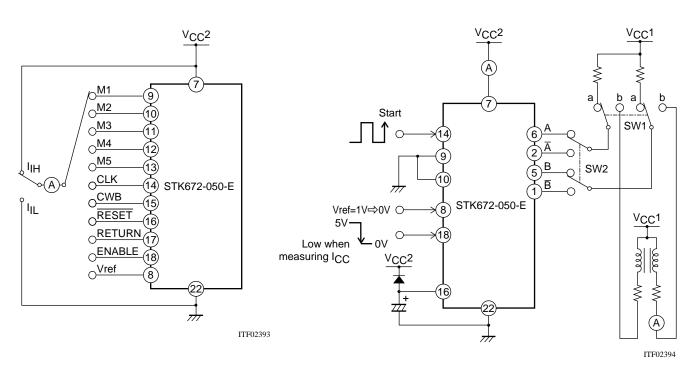
Vdf





I_{IH}, I_{IL}

Ioave, ICC, fc

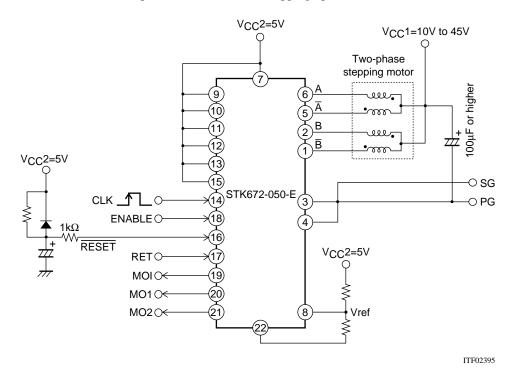


When measuring Ioave: With SW1 set to 'a', Vref = 0.6V When measuring fc: With SW1 set to 'b', Vref = 0V

When measuring ICC: Set ENABLE low

Power-on Reset

The application must perform a power-on reset operation when V_{CC}2 power is first applied to this hybrid IC. Application circuit that used 2W1-2 phase excitation (microstepping operation) mode.

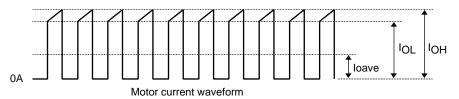


Setting the Motor Current

The motor current I_{OH} is set by the Vref voltage on the hybrid IC pin 8. The following formula gives the relationship between I_{OH} and Vref.

$$I_{OH} = \frac{1}{3} \times Vref/Rs$$
, Rs: The hybrid IC internal current detection resistor (0.2 $\Omega \pm 3\%$)

Applications can use motor currents from the current (0.05 to 0.1A) set by the duty of the frequency set by the oscillator up to the limit of the allowable operating range, $I_{OH} = 3.0A$



A12408

Function Table

M2	0	0 0 1		1		
M1 M3	0	1	0	1	Phase switching clock edge timing	
1	2 phase excitation 1-2 phase excitation		W1-2 phase excitation	2W1-2 phase excitation	Rising edge only	
0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Rising and falling edges	

CWB	0	1	RESET	Active low
	Forward	Reverse	ENABLE	Motor current is cut off when low

	А	Ā	В	B
MO1	1	0	0	1
MO2	0	0	1	1

Printed Circuit Board Design Recommendations

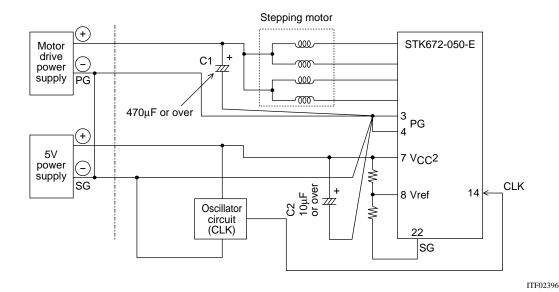
This hybrid IC has two grounds, the PG pins (pins 3 and 4) and the SG pin (pin 22). These are connected internally in the hybrid IC.

Two power supplies are required: a motor drive supply and a 5V supply for the hybrid IC itself. If the ground connections for these supplies are not good, the motor current waveforms may become unstable, motor noise may increase, and vibration levels may increase. Use appropriate wiring for these grounds. Here we present two methods for implementing these ground connections.

If the grounds for the motor drive supply and the hybrid IC 5V supply are connected in the immediate vicinity of the power supplies:

- If PG and SG are shorted at the power supply, connect only the PG line to pins 3 and 4 on the hybrid IC. Also, be sure that no problems occur due to voltage drops due to common impedances. In the specifications, this must be V_{CC}2 +5%
- The current waveforms will be more stable if the Vref ground is connected to pin 22.
- For initial values, use 470μF or over for C1 and 10μF or over for C2.

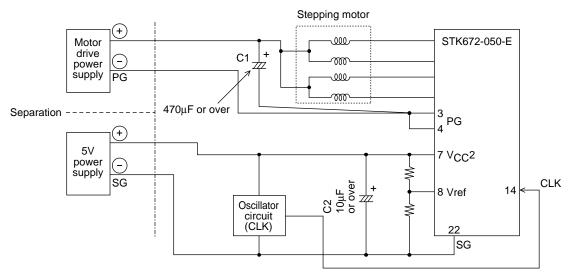
 Locate C1 as close to the hybrid IC as possible, and the capacitor ground line must be as short as possible.



If the grounds for the motor drive supply and the hybrid IC 5V supply are separated:

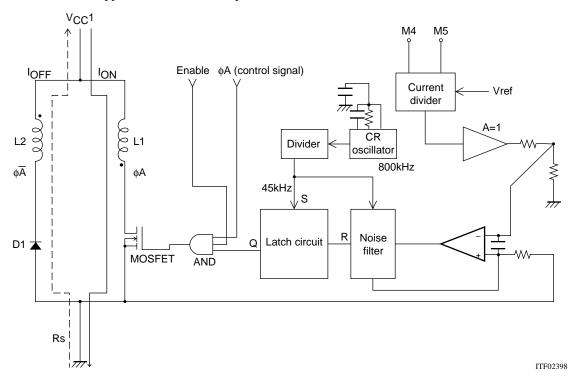
• Insert a capacitor (C1) of $100\mu F$ or over as close as possible to the hybrid IC. The capacitor ground line must be as short as possible.

The capacitor C2 may be included if necessary. Its ground line should also be as short as possible.



Functional Description

External Excitation Chopper Drive Block Description



Driver Block Basic Circuit Structure

Since this hybrid IC adopts an external excitation method, no external oscillator circuit is required.

When a high level is input to ϕA in the basic driver block circuit shown in the figure and the MOSFET is turned on, the comparator + input will go low and the comparator output will go low. Since a set signal with the PWM period will be input, the Q output will go high, and the MOSFET will be turned on as its initial value.

The current I_{ON} flowing in the MOSFET passes through L1 and generates a potential difference in Rs. Then, when the Rs potential and the Vref potential become the same, the comparator output will invert, and the reset signal Q output will invert to the low level. Then, the MOSFET will be turned off and the energy stored in L1 will be induced in L2 and the current I_{OFF} will be regenerated to the power supply. This state will be maintained until the time when an input to the latch circuit set pin occurs.

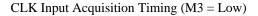
In this manner, the Q output is turned off and on repeatedly by the reset and set signals, thus implementing constant current control. The resistor and capacitor on the comparator input are spike removal circuit elements and synchronize with the PWM frequency. Since this hybrid IC uses a fixed frequency due to the external excitation method and at the same time also adopts a synchronized PWM technique, it can suppress the noise associated with holding a position when the motor is locked.

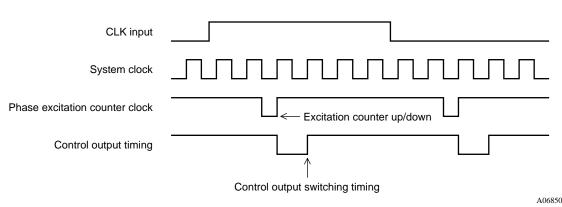
Input Pin Functions

Pin No.	Symbol	Function	Pin circuit type
14	CLK	Phase switching clock	Built-in pull-up resistor CMOS Schmitt trigger input
15	CWB	Rotation direction setting (CW/CCW)	Built-in pull-up resistor CMOS Schmitt trigger input
17	RETURN	Forced phase origin return	Built-in pull-up resistor CMOS Schmitt trigger input
18	ENABLE	Output cutoff	Built-in pull-up resistor CMOS Schmitt trigger input
9, 10, 11	M1, M2, M3	Excitation mode setting	Built-in pull-up resistor CMOS Schmitt trigger input
12, 13	M4, M5	Vector locus setting	Built-in pull-up resistor CMOS Schmitt trigger input
16	RESET	System reset	Built-in pull-up resistor CMOS Schmitt trigger input
8	Vref	Current setting	Operational amplifier input

Input Signal Functions and Timing

- CLK (phase switching clock)
 - 1) Input frequency range: DC to 50kHz
 - 2) Minimum pulse width: 10µs
 - 3) Duty: 40 to 60% (However, the minimum pulse width takes precedence when M3 is high.)
 - 4) Pin circuit type: Built-in pull-up resistor ($20k\Omega$, typical) CMOS Schmitt trigger structure
 - 5) Built-in multi-stage noise rejection circuit
 - 6) Function:
 - When M3 is high or open: The phase excited (driven) is advanced one step on each CLK rising edge.
 - When M3 is low: The phase is advanced one step by both rising and falling edges, for a total of two steps per cycle.



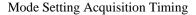


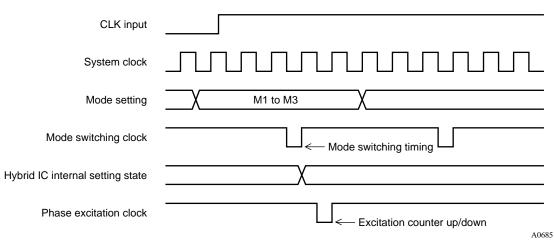
- CWB (Method for setting the rotation direction)
 - 1) Pin circuit type: Built-in pull-up resistor ($20k\Omega$, typical) CMOS Schmitt trigger structure
 - 2) Function:
 - When CWB is low: The motor turns in the clockwise direction.
 - When CWB is high: The motor turns in the counterclockwise direction.
 - 3) Notes: When M3 is low, the CWB input must not be changed for about 6.25µs before or after a rising or falling edge on the CLK input.
- RETURN (Forcible return to the origin for the currently excited phase)
 - 1) Pin circuit type: Built-in pull-up resistor ($20k\Omega$, typical) CMOS Schmitt trigger structure
 - 2) Built-in noise rejection circuit
 - 3) Notes: The currently excited (driven) phase can be forcibly moved to the origin by switching this input from low to high. Normally, if this input is unused, it must be left open or connected to V_{CC}2.
- ENABLE (Controls the on/off state of the A, \overline{A} , B, and \overline{B} excitation drive outputs and selects either operating or hold as the internal state of this hybrid IC.)
 - 1) Pin circuit type: Built-in pull-up resistor ($20k\Omega$, typical) CMOS Schmitt trigger structure
 - 2) Function:
 - When ENABLE is high or open: Normal operating state
 - When ENABLE is low: This hybrid IC goes to the hold state and excitation drive output (motor current) is forcibly turned off. In this mode, the hybrid IC system clock is stopped and no inputs other than the reset input have any effect on the hybrid IC state.

- M1, M2, and M3 (Excitation mode and CLK input edge timing selection)
 - 1) Pin circuit type: Built-in pull-up resistor ($20k\Omega$, typical) CMOS Schmitt trigger structure
 - 2) Function:

M2	0	0	1	1		
M1 M3	0	1	0	1	Phase switching clock edge timing	
1	2 phase excitation	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	Rising edge only	
0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Rising and falling edges	

3) Valid mode setting timing: Applications must not change the mode in the period 5µs before or after a CLK signal rising or falling edge.

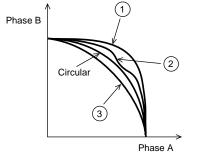




• M4 and M5 (Microstepping mode rotation vector locus setting)

111 1 001105 111	e (miles obtep	pring model r	otteron reeto	1 10000 50000
M4	1	0	1	0
M5	1	0	0	1
Mode	Circular	①	2	3

See page 10 for details on the current division ratio.



- RESET (Resets all parts of the system.)
 - 1) Pin circuit type: Built-in pull-up resistor ($20k\Omega$, typical) CMOS Schmitt trigger structure
 - 2) Function:
 - All circuit states are set to their initial values by setting the \overline{RESET} pin low. (Note that the pulse width must be at least $10\mu s$.)
 - At this time, the A and \overline{B} phases are set to their origin, regardless of the excitation mode. The output current goes to about 71% after the reset is released.
 - 3) Notes: When power is first applied to this hybrid IC, Vref must be established by applying a reset. Applications must apply a power on reset when the V_{CC}2 power supply is first applied.
- Vref (Sets the current level used as the reference for constant-current detection.)
 - 1) Pin circuit type: Analog input structure
 - 2) Function:
 - Constant-current control can be applied to the motor excitation current at 100% of the rated current by applying a voltage less than the control system power supply voltage V_{CC}2 minus 2.5V.
 - Applications can apply constant-current control proportional to the Vref voltage, with this value of 2.5V as the upper limit.

STK672-050-E

Output Pin Functions

Pin No.	Symbol	Function	Pin circuit type	
19 MOI		Phase excitation origin monitor	Standard CMOS structure	
20, 21	MO1, MO2	Phase excitation state monitor	Standard CMOS structure	

Output Signal Functions and Timing

- A, \overline{A} , B, and \overline{B} (Motor phase excitation outputs)
 - 1) Function:
 - In the 4 phase and 2 phase excitation modes, a 3.75 μs (typical) interval is set up between the A and \overline{A} and B and \overline{B} output signal transition times.
- MO1, MO2, and MOI (Phase excitation state monitors)
 - 1) Pin circuit type: Standard CMOS structure
 - 1) Function:
 - Output of the current phase excitation output state.

Phase coordinate	Phase A	Phase B	Phase A	Phase B
MO1	1	0	0	1
MO2	0	1	0	1

MOI outputs a 0 when each phase is at the origin, and outputs a 1 otherwise.

• Current division ratios set by M3, M4, and M5 Values provided for reference purposes.

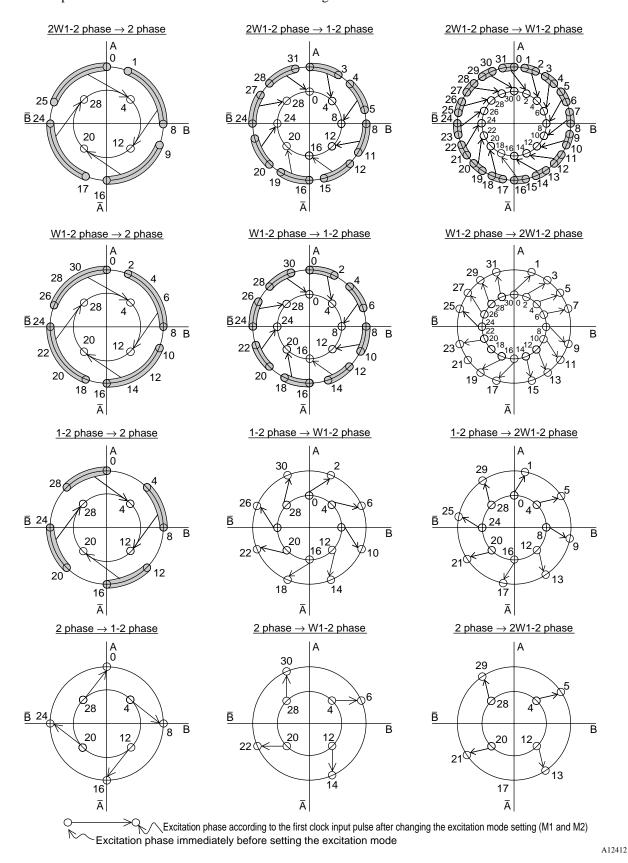
	Mode		Circular	1	2	3			
0-44	0		M4 = 1	M4 = 0	M4 = 1	M4 = 1	Units	Number of steps	
Setting	M3 = 0	M3 = 1	M5 = 1	M5 = 0	M5 = 0	M5 = 1			
			14	15	15	13			1/16
		2W1-2	20	25	23	19		1/8	2/16
			31	34	33	28			3/16
		2W1-2	40	44	42	39	%	2/8	4/16
			48	51	49	45			5/16
		2W1-2	55	62	57	54		3/8	6/16
Current division	4)//4 0		65	69	65	62			7/16
ratio	4W1-2	2W1-2	71	77	71	69		4/8	8/16
14.15			77	82	77	74			9/16
		2W1-2	83	88	85	82		5/8	10/16
			88	92	89	85			11/16
		2W1-2	92	95	95	92		6/8	12/16
			97	98	98	94			13/16
		2W1-2	100	100	100	100		7/8	14/16

[Load conditions]

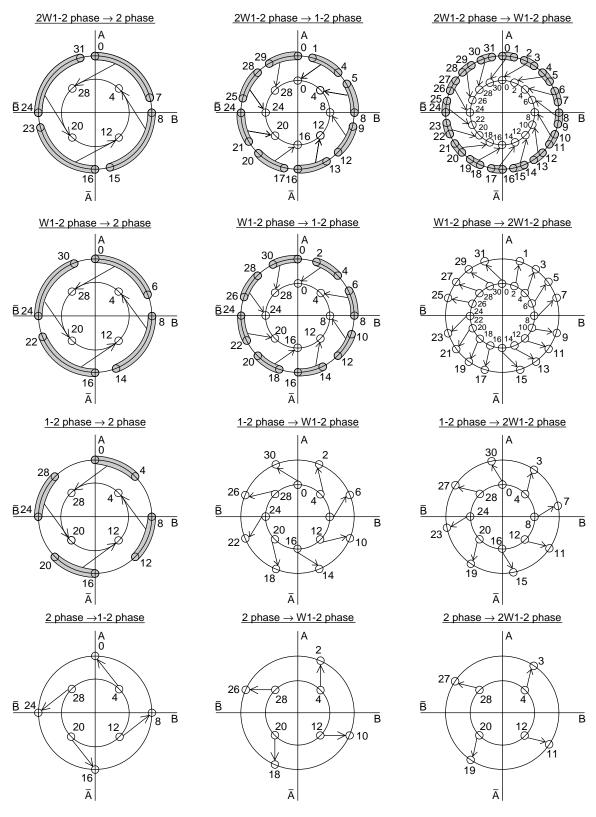
 $V_{CC}1 = 24V, V_{CC}2 = 5V, R/L = 3.5/3.8mH$

Phase States During Excitation Switching

• Excitation phases before and after excitation mode switching <clockwise direction>



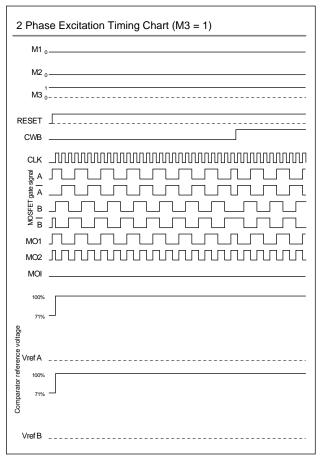
• Excitation phases before and after excitation mode switching <counterclockwise direction>

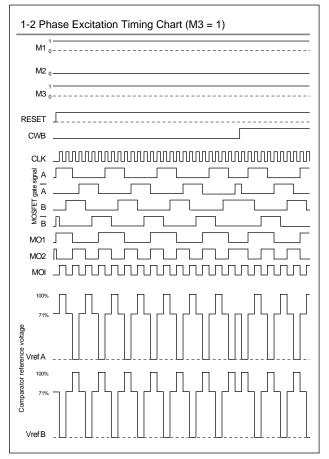


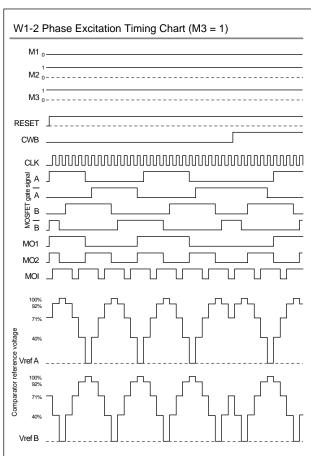
A12413

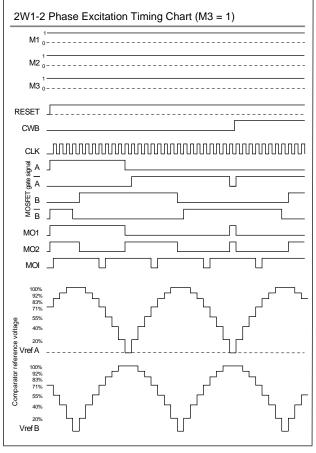
Excitation Time and Timing Charts

• CLK rising edge operation

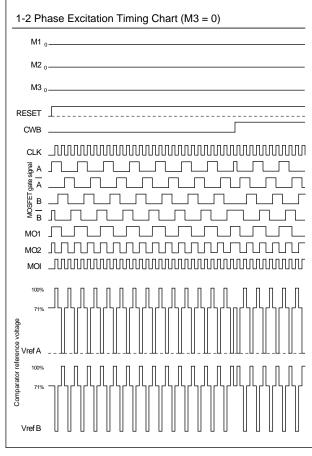


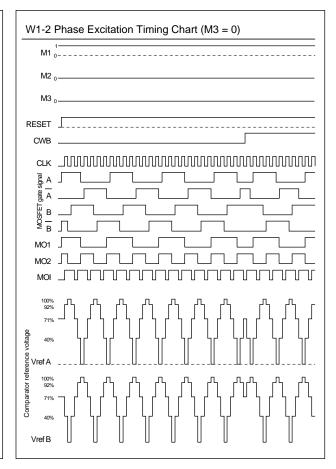


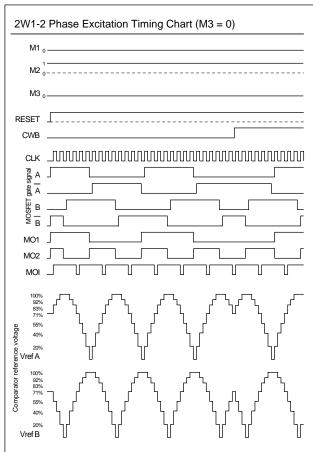


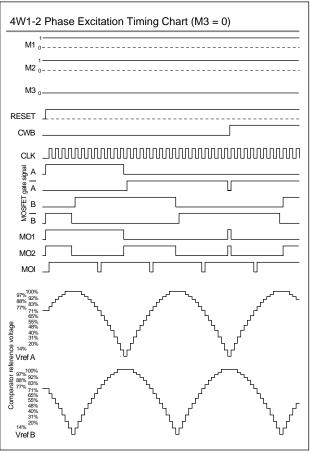


• CLK rising and falling edge operation









Thermal Design

< Hybrid IC Average Internal Power Loss Pd>

The main elements internal to this hybrid IC with large average power losses are the current control devices, the regenerative current diodes, and the current detection resistor. Since sine wave drive is used, the average power loss during microstepping drive can be approximated by applying a waveform factor of 0.64 to the square wave loss during 2 phase excitation.

The losses in the various excitation modes are as follows.

2 phase excitation
$$Pd_{2EX} = (Vsat + Vdf) \cdot \frac{fclock}{2} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{2} \cdot (Vsat \cdot t1 + Vdf \cdot t3)$$

1-2 phase excitation
$$Pd_{1-2EX} = 0.64 \cdot \{(Vsat + Vdf) \cdot \frac{fclock}{4} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{4} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

$$W1\text{-}2 \text{ phase excitation} \quad PdW_{1\text{-}2EX} = 0.64 \cdot \{(Vsat + Vdf) \cdot \frac{-fclock}{8} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{8} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

$$2W1-2 \text{ phase excitation } Pd_{2W1-2EX} = 0.64 \cdot \{(Vsat+Vdf) \cdot \frac{fclock}{16} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{16} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

$$4W1-2 \ phase \ excitation \ Pd_{4W1-2EX} = 0.64 \cdot \{(Vsat+Vdf) \cdot \frac{fclock}{16} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{16} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

Here, t1 and t3 can be determined from the same formulas for all excitation methods.

$$t1 = \frac{-L}{R + 0.48} \cdot \ell \, n \, \left(1 - \frac{R + 0.48}{V_{CC} 1} \cdot I_{OH}\right)$$

$$t3 = \frac{-L}{R} \cdot \ell \, n \, \left(\frac{V_{CC}^{1+0.48}}{I_{OH} \cdot R + V_{CC}^{1+0.48}} \right)$$

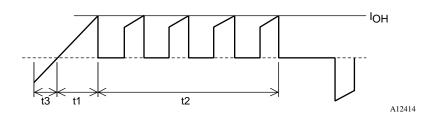
However, the formula for t2 differs with the excitation method.

2 phase excitation
$$t2 = \frac{2}{\text{fclock}} - (t1+t3)$$

$$t2 = \frac{2}{\text{fclock}} - (t1+t3)$$
 1-2 phase excitation $t2 = \frac{3}{\text{fclock}} - t1$

W1-2 phase excitation
$$t2 = \frac{7}{\text{fclock}} - t1$$

2W1-2 phase excitation
$$t2 = \frac{15}{\text{fclock}} - t1$$



Motor Phase Current Model Figure (2 Phase Excitation)

fclock: CLK input frequency (Hz)

Vsat : The voltage drop of the power MOSFET and the current detection resistor (V)

: The voltage drop of the body diode and the current detection resistor (V) Vdf

IOH : Phase current peak value (A)

: Phase current rise time (s) V_{CC}1 : Supply voltage applied to the motor (V) t1

t2 : Constant-current operating time (s) : Motor inductance (H) L

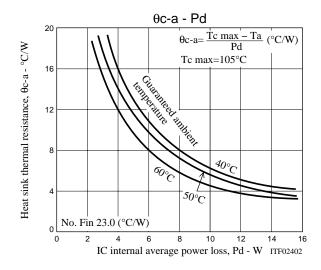
: Phase switching current regeneration time (s) R : Motor winding resistance (Ω) t3

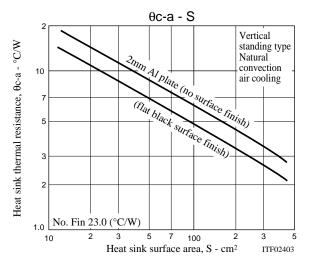
<Determining the Size of the Hybrid IC Heat Sink>

Determine θ c-a for the heat sink from the average power loss determined in the previous item.

$$\theta \text{c-a} = \frac{\text{Tc max - Ta}}{\text{Pd}_{EX}} \ [^{\circ}\text{C/W}]$$
 Ta: Application internal temperature ($^{\circ}\text{C}$) PdEX: Hybrid IC internal average loss (W)

Determine θ c-a from the above formula and then size S (in cm²) of the heat sink from the graphs shown below. The ambient temperature of the device will vary greatly according to the air flow conditions within the application. Therefore, always verify that the size of the heat sink is adequate to assure that the Hybrid IC back surface (the aluminum plate side) will never exceed a Tc max of 105° C, whatever the operating conditions are.





Next we determine the usage conditions with no heat sink by determining the allowable hybrid IC internal average loss from the thermal resistance of the hybrid IC substrate, namely 18.5°C/W.

For a Tc max of
$$105^{\circ}$$
C at an ambient temperature of 50° C
$$Pd_{EX} = \frac{105 - 50}{18.5} = 2.9W$$

For a Tc max of
$$105^{\circ}$$
C at an ambient temperature of 40° C
$$Pd_{EX} = \frac{105 - 40}{18.5} = 3.5W$$

This hybrid IC can be used with no heat sink as long as it is used at operating conditions below the losses listed above. (See $\Delta Tc - Pd$ curve in the graph on page 19.)

<Hybrid IC internal power element (MOSFET) junction temperature calculation>

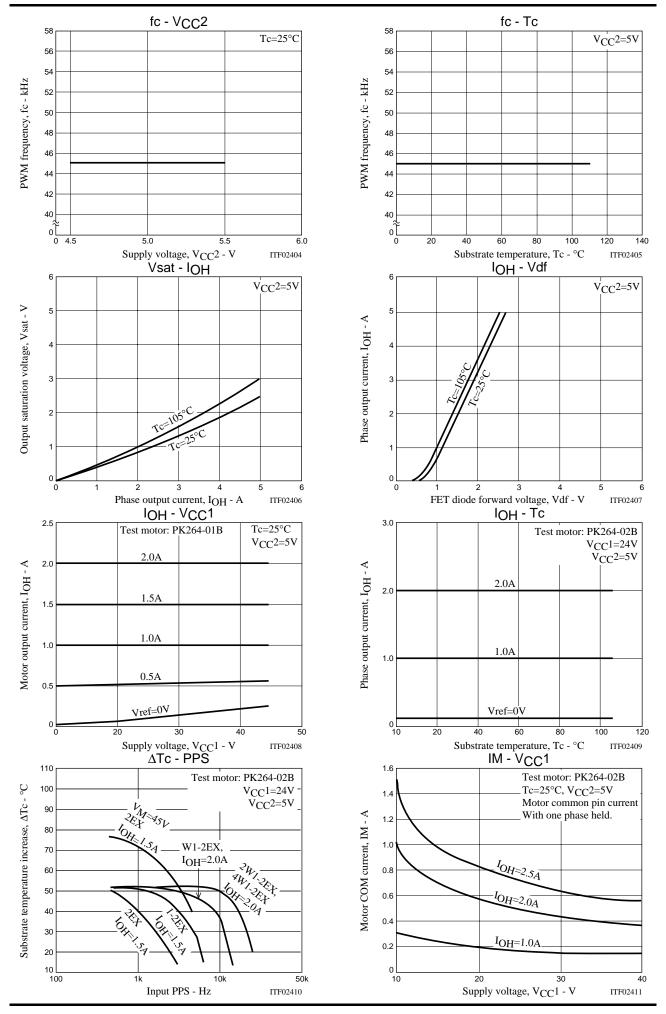
The junction temperature, Tj, of each device can be determined from the loss Pds in each transistor and the thermal resistance θ j-c.

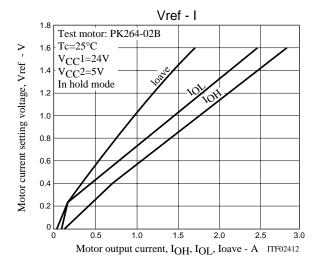
$$T_i = T_c + \theta_{i-c} \times Pds$$
 (°C)

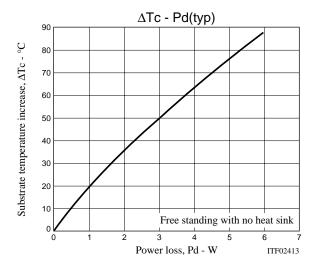
Here, we determine Pds, the loss for each transistor, by determining Pdfx in each excitation mode.

$$Pds = Pd_{EX}/4$$

The steady-state thermal resistance θ j-c of a power MOSFET is 5°C/W.







- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of June, 2008. Specifications and information herein are subject to change without notice.