

### SP8660 A, B & M

#### 180 MHz ÷ 10 (LOW POWER)

The SP8660 is a fixed ratio (divide by 10) low power counter for operation at frequencies in excess of 100MHz over the temperature ranges  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ('A' grade)  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  ('B' grade) and  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  ('M' grade)

The input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used, the unused input must be capacitively decoupled to the ground plane. There are two bias points, which should also be capacitively decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

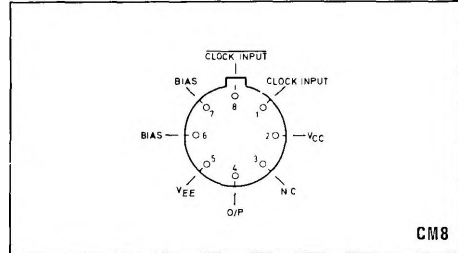


Fig. 1 Pin connections (viewed from beneath)

#### FEATURES

- ☐ VHF Operation
- ☐ Low Power Dissipation
- ☐ Output TTL and CMOS Compatible
- ☐ Military and Commercial Temperature Ranges

#### APPLICATIONS

- ☐ Low Power VHF Communications
- ☐ Portable Counters

#### ABSOLUTE MAXIMUM RATINGS

Power supply voltage, $ V_{CC} - V_{EE} $	8V	Not greater than supply voltage in use
Input voltage $V_{in}$		10mA
Output sink current, $I_o$		$+150^{\circ}\text{C}$
Operating junction temperature		$-55^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Storage temperature		

#### OPERATING NOTES

Fig. 3 gives capacitor values for AC and DC coupling of the input and bias points on the test circuit; these values are not critical and will depend on the operating frequency.

The device will normally self-oscillate in the absence of an input signal. This can be easily prevented by connecting a  $39\text{k}\Omega$  pulldown resistor from either input (double drive) to  $V_{EE}$ ; if the device is single driven then it is recommended that the pulldown resistor be connected to the decoupled unused input. The slight loss of input sensitivity resulting from this technique does not seriously affect the operation of the device.

The input waveform will normally be sinusoidal but below 40MHz correct operation depends on the slew rate of the input signal. A slew rate of  $100\text{V}/\mu\text{s}$  will enable the device to operate down to DC.

The output stage will drive three TTL gates without the addition of a pull-up resistor. Using a pull-up resistor of  $3.3\text{k}\Omega$  (or less) to  $+10\text{V}$  will allow the output to drive a CMOS binary counter at a frequency of up to 5MHz.

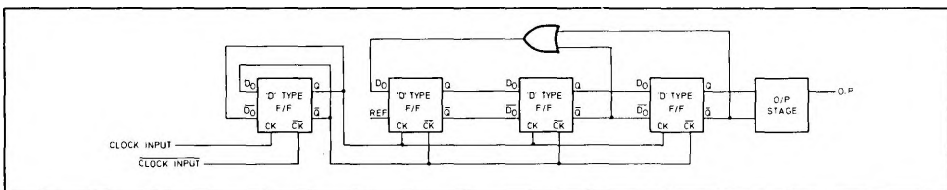


Fig. 2 Logic diagram

**SP8660**

**ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated)

Operating ambient temperature  $T_A$

'A' grade:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; 'B' grade:  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ; 'M' grade:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;

Operating supply voltages

$V_{CC} : +5.0\text{V} \pm 0.25\text{V}$ ;  $V_{EE} : 0\text{V}$

Input voltage

Single drive:  $400\text{mV}$  to  $800\text{mV}$  p-p; double drive:  $250\text{mV}$  to  $800\text{mV}$  p-p

Output load  $3.3\text{k}\Omega$  to  $+10\text{V}$ , in parallel with  $7\text{pF}$

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Maximum input frequency	100	200		MHz	$V_{CC} = +5.0\text{V}$
Minimum sinusoidal input frequency		20	40	MHz	
Minimum slew rate of square wave input		30	100	$\text{V}/\mu\text{s}$	
Power supply drain current		10	13	mA	
Output level (high)	9.0			V	
Output level (low)			400	mV	

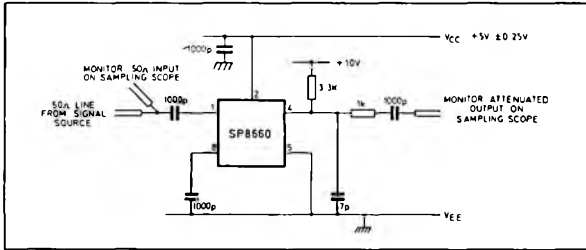


Fig. 3 Test circuit