

SP8000 SERIES HIGH SPEED DIVIDERS

SP8655A, B & M (÷32) SP8657A, B & M (÷20) SP8659A, B & M (÷16)

The SP8655A, B & M, SP8657A, B & M and SP8659A, B & M are fixed ratio (divide by 32, 20 and 16) low power counters for operation at frequencies in excess of 200 MHz over the temperature ranges $-55 \,^{\circ}$ C to $+125 \,^{\circ}$ C ('A' grade), 0°C to $+ 70 \,^{\circ}$ C ('B' grade) and $-40 \,^{\circ}$ C to $+85 \,^{\circ}$ C ('M' grade).

In all cases the input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used the unused input must be capacitively decoupled to the ground plane. There are two bias points, which should be capacitively decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

FEATURES

- VHF Operation
- Low Power Dissipation
- Output TTL and CMOS Compatible

APPLICATIONS

- Low Power VHF Communications
- Portable Counters

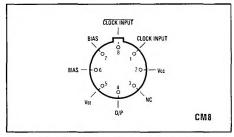


Fig. 1 Pin connections (viewed from beneath)

ABSOLUTE MAXIMUM RATINGS

Power supply voltage, Vcc—VEE Input voltage Vin

Output sink current, lo Operating junction temperature Storage temperature 8V Not greater than supply voltage in use 10mA

+150°C -55°C to +150°C

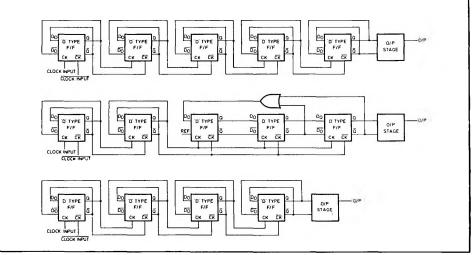


Fig. 2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

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Operating ambient temperature Tamb:	—55°C to +125°C ('A' grade)
	0 °C to +70 °C ('B' grade)
	—40 °C to +85 °C ('M' grade)
Operating supply voltages VCC:	+5.2V+0.25V; VEE: OV
Input voltage single drive:	400mV to 800mV p-p
double drive :	250mV to 800mV p-p
Output load 3.3k Ω to $-10V$, in parallel with 7pF.	

Value Characteristic Units Conditions Min. Max. Typ. Maximum input frequency 200 MHz Minimum sinusoidal input frequency 20 40 MHz Minimum slew rate of square wave input 30 100 V/µs Power supply drain current 10 13 mΑ VCC = +5.2VOutput level (high) 9.0 v Output level (low) m٧ 400

OPERATING NOTES

Fig. 3 gives capacitor values for AC and DC coupling of the input and bias points on the test circuit these values are not critical and will depend on the operating frequency.

The devices will normally self-oscillate in the absence of an input signal. This can be easily torevented by connecting a 39k Ω pulldown resistor from either input (double drive) to VEE; if the device is single driven then it is recommended that the pulldown resistor be connected to the decoupled unused input. The slight loss of input sensitivity resulting from this technique does not seriously affect the operation of the device.

The input waveform will normally be sinusoidal but below 40MHz correct operation depends on the slew rate of the input signal. A slew rate of 100V/µs will enable the device to operate down to DC.

The output stage will drive three TTL gates without the addition of a pull-up resistor. Using a pull-up resistor of 3.3k Ω (or less) to a +10V will allow the output to drive a CMOS binary counter at a frequency of up to 5MHz.

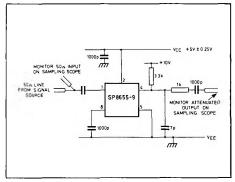


Fig. 3 Test circuit