

SP1668B (HIGH Z)
SP1669B (LOW Z)
DUAL CLOCKED LATCH

This device is a Dual Clocked Latch/R-S Flip-Flop. Whenever the Clock is low, the R-S inputs control the output state. Whenever the Clock is high, the output follows the data (D) input.

TRUTH TABLE

S	R	D	C	Q_{n+1}
0	0	ϕ	0	Q_n
1	0	ϕ	0	1
0	1	ϕ	0	0
1	1	ϕ	0	**
ϕ	ϕ	0	1	0

** Output stage not defined
 ϕ Don't care

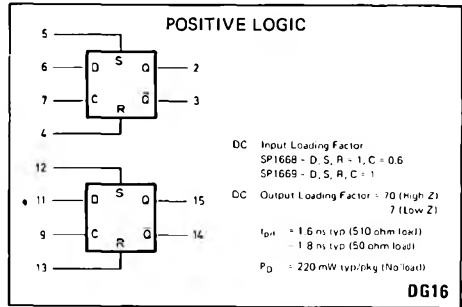


Fig. 1 Logic diagram of SP1668/1669

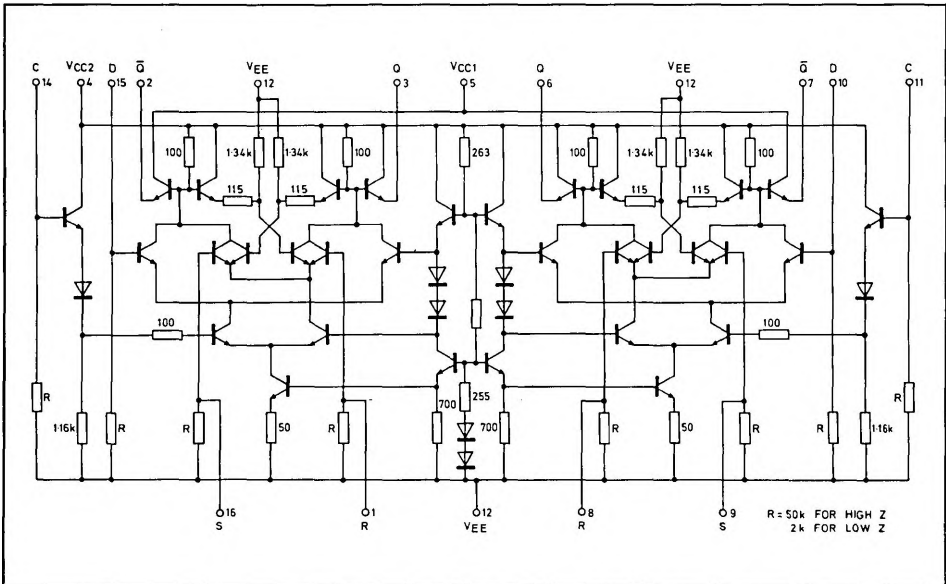


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package

should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board.

③ Test Temperature

0°C

+25°C

+75°C

Characteristic	Symbol	Pin Under Test	SP1668 /SP1669 Test Limits						TEST VOLTAGE APPLIED TO PINS LISTED BELOW:							
			0°C		+25°C		+75°C		Unit	V _{IH} max	V _{IH} min	V _{IHL} max	V _{IHL} min			
			Min	Max	Min	Max	Min	Max								
Power Supply Drain Current	I _E (H-Z)	8	-	-	-	55	-	-	mAde	7.9	-	-	-	8	1.16	
Input Current (H-Z)	I _{in} H	11,12,13	-	-	-	0.370	-	-	mAde	11,12,13	-	-	-	8	1.16	
	I _{in} L	11,12,13	-	-	0.500	0.225	-	-	mAde	9	-	-	-	8	1.16	
Input Current (L-Z)	I _{in} H	11,12,13	-	-	0.500	-	-	-	μAde	-	11,12,13	-	-	8	1.16	
	I _{in} L	11,12,13	-	-	3.2	3.1	-	-	μAde	-	9	-	-	8	1.16	
	I _{in} L	11,12,13	-	-	1.300	1.300	-	-	mAde	-	11,12,13	-	-	8	1.16	
"Q" Logic "1" Output Voltage	V _{OH}	15	1.000	-0.840	-0.860	-0.810	-0.900	-0.720	Vdc	-	13	-	-	8	1.16	
Output Voltage	V _{OL}	14	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	9	-	-	-	8	1.16	
"Q" Logic "0" Output Voltage	V _{OH}	14	-1.000	-0.840	-0.860	-0.810	-0.900	-0.720	Vdc	-	12	-	-	8	1.16	
Output Voltage	V _{OL}	14	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	9	-	-	-	8	1.16	
"Q" Logic "1" Output Threshold Voltage	V _{OHA}	15	-1.020	-	-	-	-0.970	-	Vdc	-	-	12	13	8	1.16	
	V _{OHA}	15	-	-	-	-	-	-	Vdc	11	-	-	9	-	-	
"Q" Logic "0" Output Threshold Voltage	V _{OLA}	15	-	-1.615	-	-	-1.600	-	Vdc	-	-	-	13	12	8	1.16
	V _{OLA}	15	-	-	-	-	-	-	Vdc	-	-	11	9	-	-	
"Q" Logic "0" Output Threshold Voltage	V _{OHA}	14	-1.020	-	-	-	-0.970	-	Vdc	-	-	-	13	12	8	1.16
	V _{OHA}	14	-	-	-	-	-	-	Vdc	-	-	11	9	-	-	
"Q" Logic "0" Output Threshold Voltage	V _{OLA}	14	-	-1.615	-	-	-1.600	-	Vdc	-	-	-	12	13	8	1.16
	V _{OLA}	14	-	-	-	-	-	-	Vdc	-	-	11	9	-	-	
Switching Times (50Ω Load) Clock Input		15	1.0	2.5	1.0	2.5	1.1	2.8	ns	9	15	-	-	8	1.16	
		15	-	-	-	-	-	-	ns	-	15	-	-	-	-	
		14	-	-	-	-	-	-	ns	-	14	-	-	-	-	
		14	-	-	-	-	-	-	ns	-	14	-	-	-	-	
Rise Time	t _r	14,15	0.8	2.6	0.9	2.5	0.9	2.8	ns	9	14,15	-	-	8	1.16	
Fall Time	t _f	14,15	0.5	2.2	0.5	2.2	0.5	2.5	ns	9	14,15	-	-	8	1.16	
Set Input	t ₁₂₊₁₅₊	15	1.0	2.3	1.1	2.3	1.1	2.6	ns	12	15	-	-	8	1.16	
	t ₁₂₊₁₅₋	14	1.0	2.3	1.1	2.3	1.1	2.6	ns	12	14	-	-	8	1.16	
Reset Input	t ₁₃₊₁₄₊	14	1.0	2.3	1.1	2.3	1.1	2.6	ns	13	14	-	-	8	1.16	
	t ₁₃₊₁₅₋	15	1.0	2.3	1.1	2.3	1.1	2.6	ns	13	15	-	-	8	1.16	

TEST VOLTAGE VALUES (Volts)

V_{IH} max

V_{IHL} min

V_{IHL} max

V_{IHL} min

V_{IHL} max

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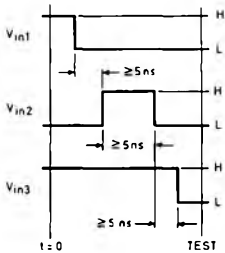
V_{IHL} min

V_{IHL} max

V_{IHL} min

V_{IHL} max

- ① I_E is measured with no output pulldown resistors.
- ② Test voltage applied to pin under test.
- ③ Apply V_{in1} to S (V_{IH} to V_{IL}).
- ④ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL}), V_{in2} to C (V_{IH} to V_{IL}), V_{in3} to D (V_{IH} to V_{IL})



- ⑤ Apply V_{in1} to R (V_{IH} to V_{IL})
- ⑥ Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL}), V_{in2} to C (V_{IH} to V_{IL})
- ⑦ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL}), V_{in2} to C (V_{IH} to V_{IL})

Fig. 3 Notes referred to in electrical characteristics

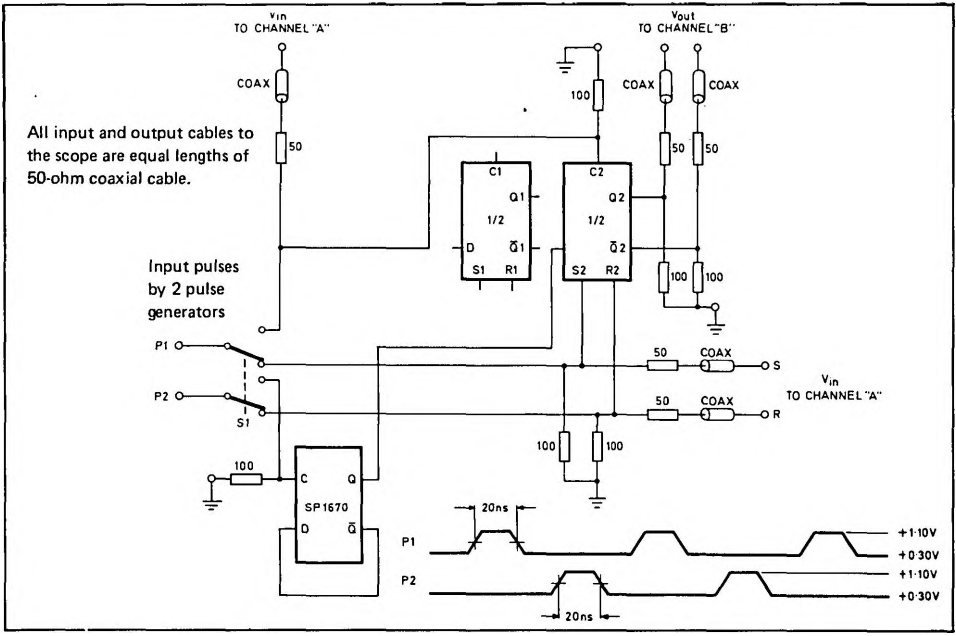


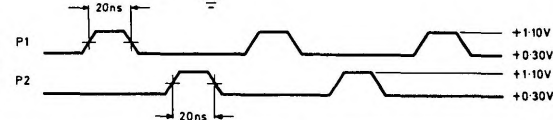
Fig. 4 Switching time test circuit

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Input pulses by 2 pulse generators

TO CHANNEL "A"

TO CHANNEL "A"



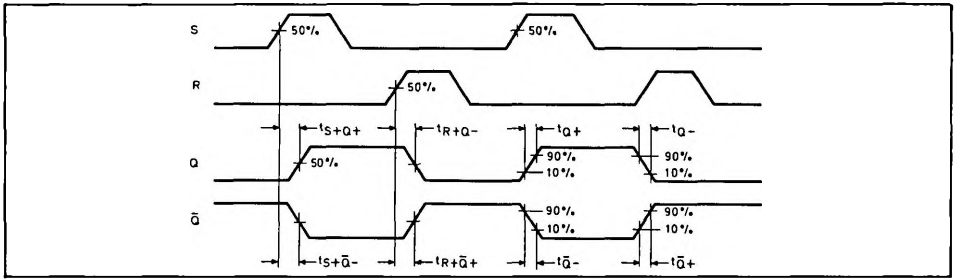


Fig. 5 Switching time waveforms (set/reset to Q/Q-bar, switch S1 in position shown in Fig. 3)

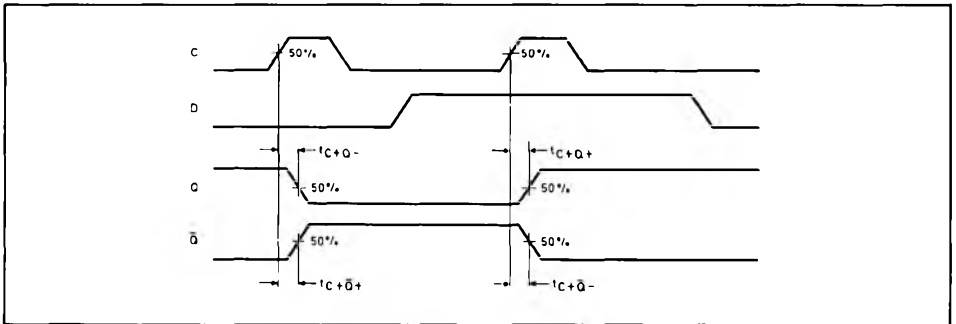


Fig. 6 Switching time waveforms (clock to Q/Q-bar, switch S1 in position opposite to that shown in Fig. 3)