SN75437A
QUADRUPLE PERIPHERAL DRIVER

- **Saturating Outputs With Low On-State Resistance**
- **High-Impedance Inputs Compatible With CMOS and TTL Levels**
- **Very Low Standby Power . . . 21 mW Max**
- **High-Voltage Outputs . . . 70 V Min**
- **No Power-Up or Power-Down Output Glitch**
- **No Latch-Up Within Recommended Operating Conditions**
- **Output-Clamp Diodes for Transient Suppression**
- **Packaged in 2-W Power, Thermally Enhanced Plastic DIP**

NE PACKAGE
(TOP VIEW)

1Y	1		16	1A
1, 2 D	2		15	2A
2Y	3		14	G
HEAT SINK AND GND	4		13	HEAT SINK AND GND
	5		12	
3Y	6		11	V$_{CC}$
3, 4 D	7		10	3A
4Y	8		9	4A
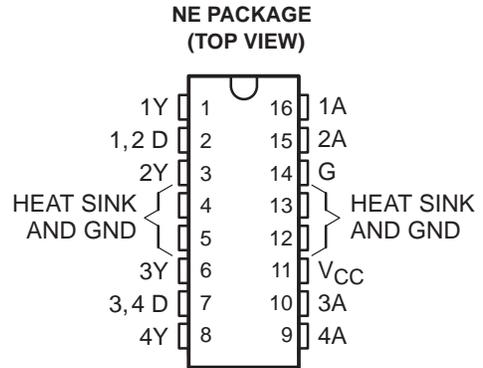
description

The SN75437A quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. This device features four inverting open-collector outputs with a common-enable (G) input that, when taken low, disables all four outputs. The envelope of 1-V characteristics exceeds the specifications sufficiently to avoid high-current latch-up. Applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand devices.

The SN75437A is characterized for operation over the free-air temperature range of 0°C to 70°C.

FUNCTION TABLE
(each NAND driver)

INPUTS		OUTPUT
A	**G**	**Y**
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

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QUADRUPLE PERIPHERAL DRIVER

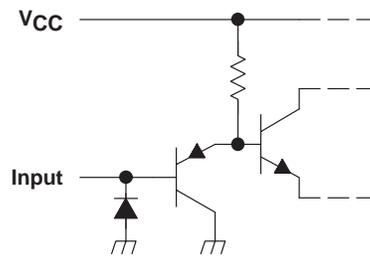## logic diagram (positive logic)†
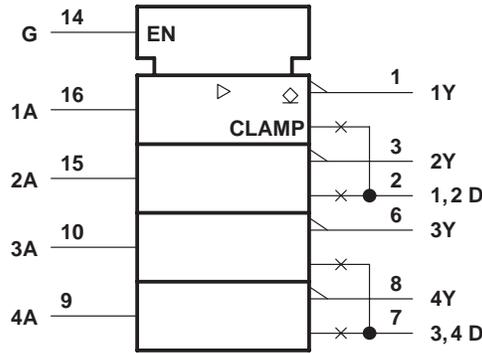
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

logic diagram (positive logic, each driver)
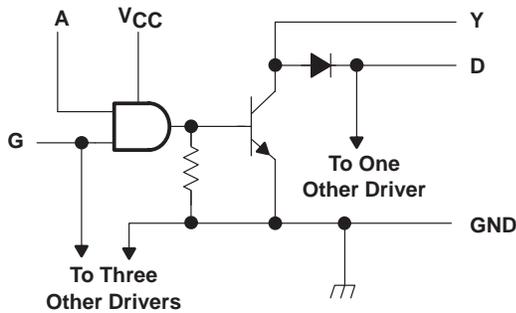
equivalent schematic of each input

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 30 V
Output current (see Note 1) .... 0.75 A
Output clamp-diode current, I_{OK} .... 1.25 A
Output voltage, V_O (off state) .... 70 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) .... 2075 mW
Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds .... 260°C
Storage temperature range, T_{stg} .... −65°C to 150°C

NOTES: 1. All four sections of these circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
2. For operation above 25°C free-air temperature, derate linearly to 1328 mW at 70°C at the rate of 16.6 mW/°C.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Output supply voltage in inductive switching circuit (see Figure 2), V_S			35	V
Output current, I_O			0.5	A
Operating free-air temperature, T_A	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$V_{CC} = 4.75$ V,	$I_I = -12$ mA		-0.9	-1.5	V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V	$I_{OL} = 250$ mA		0.14	0.25	V
			$I_{OL} = 500$ mA		0.28	0.5	
$V_{R(K)}$	Output clamp-diode reverse voltage	$V_{CC} = 4.75$ V,	$I_R = 100$ μA	70	100		V
$V_{F(K)}$	Output clamp-diode forward voltage	$I_F = 500$ mA			1	1.6	V
I_{OH}	High-level output current	$V_{CC} = 4.75$ V, $V_{IL} = 0.8$ V,	$V_{IH} = 2$ V, $V_{OH} = 70$ V		1	100	μA
I_{IH}	High-level input current	$V_{CC} = 5.25$ V,	$V_I = 5.25$ V		0.1	10	μA
I_{IL}	Low-level input current	$V_{CC} = 5.25$ V,	$V_I = 0.8$ V		-0.25	-10	μA
I_{CCH}	Supply current, outputs high	$V_{CC} = 5.25$ V,	$V_I = 0$		1	4	mA
I_{CCL}	Supply current, outputs low	$V_{CC} = 5.25$ V,	$V_I = 5$ V		45	65	mA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 30$ pF, See Figure 1	$R_L = 60$ Ω,		1950	5000	ns
t_{PHL}	Propagation delay time, high-to-low-level output				150	500	ns
t_{TLH}	Transition time, low-to-high-level output				40		ns
t_{THL}	Transition time, high-to-low-level output				36		ns
V_{OH}	High-level output voltage after switching	$V_S = 35$ V, $R_L = 70$ Ω,	$I_O \approx 500$ mA, See Figure 2	V_S-10			mV

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PARAMETER MEASUREMENT INFORMATION
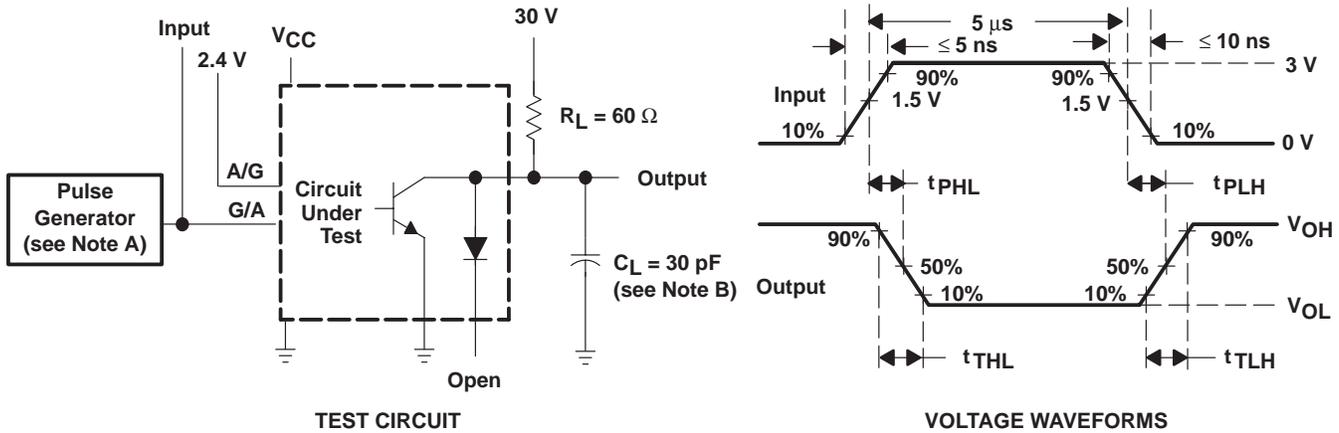
NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms
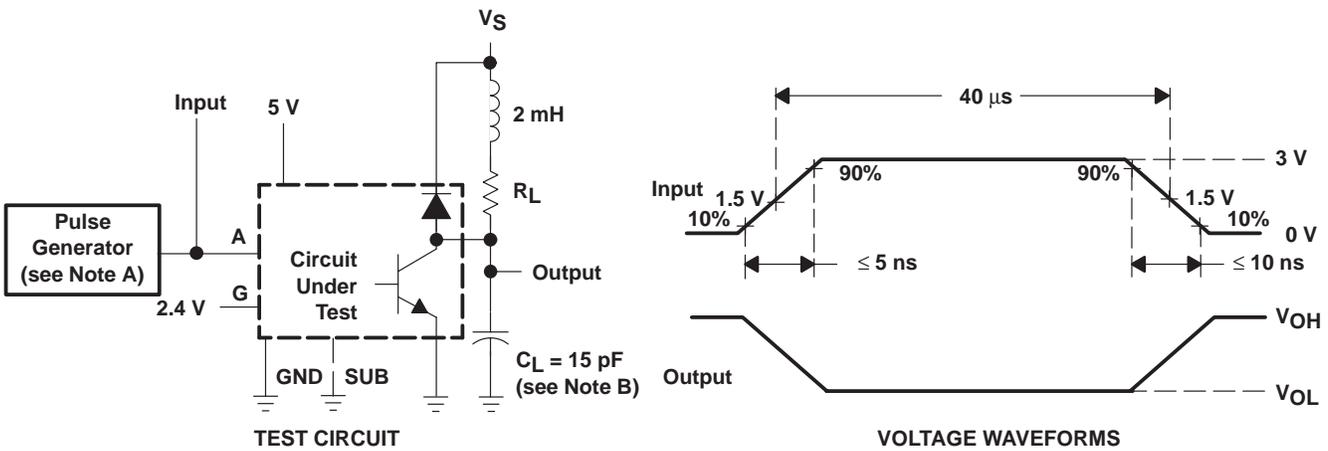
NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Latch-Up Test Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN75437ANE	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75437ANEE4	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
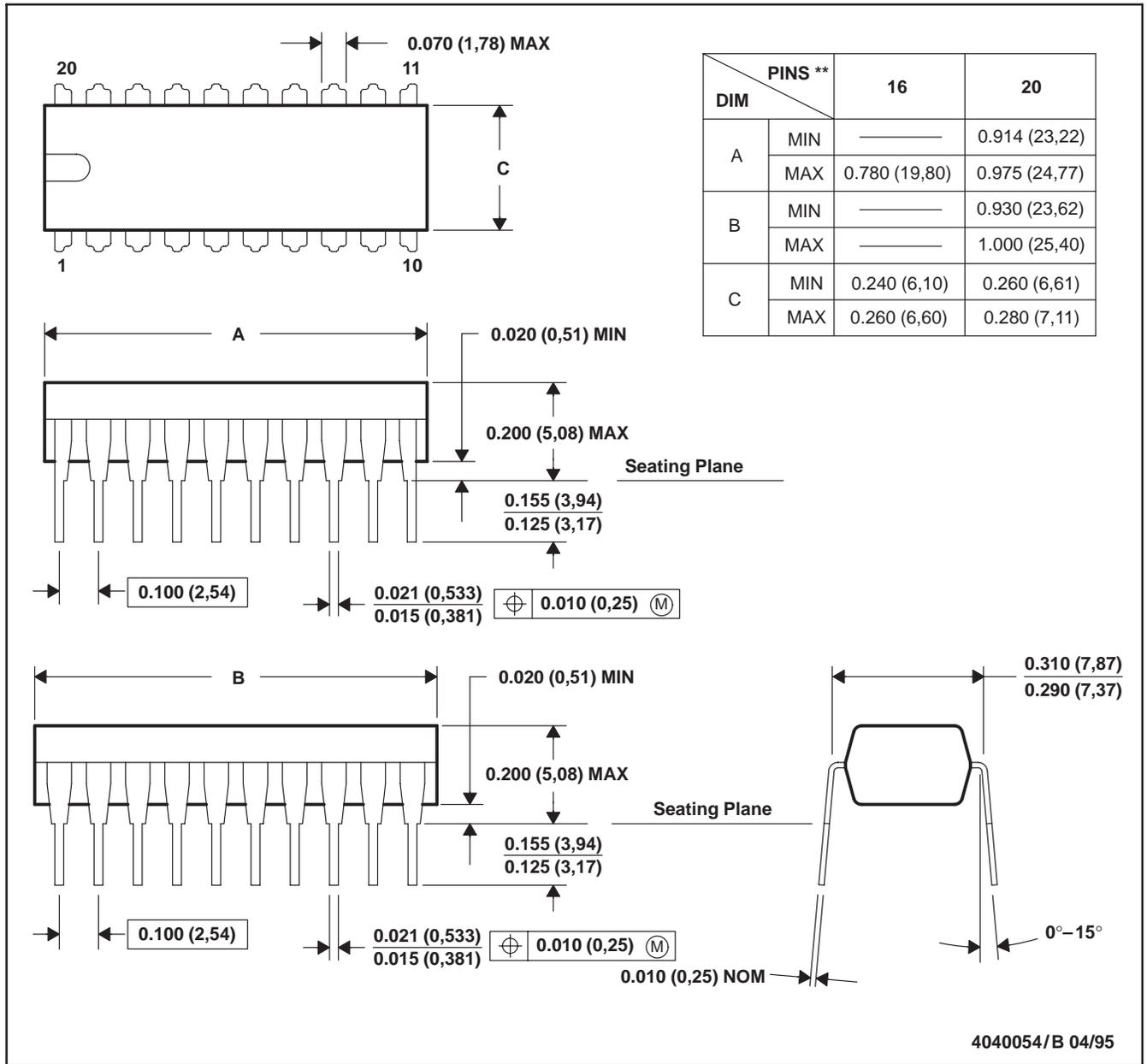
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NE (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

20 PIN SHOWN

DIM	PINS **	16	20
A	MIN	———	0.914 (23,22)
	MAX	0.780 (19,80)	0.975 (24,77)
B	MIN	———	0.930 (23,62)
	MAX	———	1.000 (25,40)
C	MIN	0.240 (6,10)	0.260 (6,61)
	MAX	0.260 (6,60)	0.280 (7,11)

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.155 (3,94)
0.125 (3,17)

0.100 (2,54)

0.021 (0,533)
0.015 (0,381)

⊕ 0.010 (0,25) Ⓜ

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.155 (3,94)
0.125 (3,17)

0.100 (2,54)

0.021 (0,533)
0.015 (0,381)

⊕ 0.010 (0,25) Ⓜ

0.310 (7,87)
0.290 (7,37)

0°−15°

0.010 (0,25) NOM

4040054 / B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (16 pin only)

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