

# SN54LVT646, SN74LVT646

## 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS140D – MAY 1992 – REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (JT) DIPs

### description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

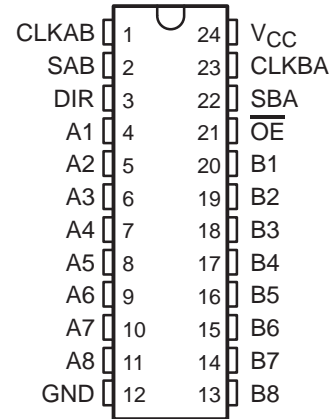
The 'LVT646 consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT646.

Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

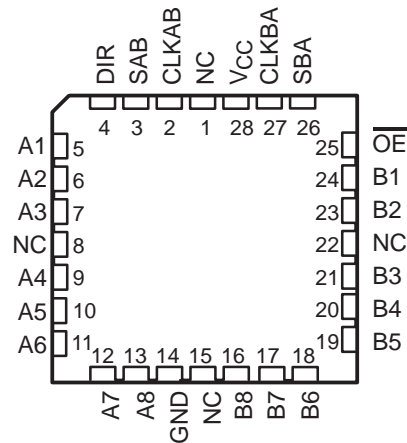
The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

SN54LVT646 . . . JT OR W PACKAGE  
SN74LVT646 . . . DB, DW, OR PW PACKAGE  
(TOP VIEW)



SN54LVT646 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

# SN54LVT646, SN74LVT646

## 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

### WITH 3-STATE OUTPUTS

SCBS140D – MAY 1992 – REVISED JULY 1995

#### description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT646 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT646 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LVT646 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

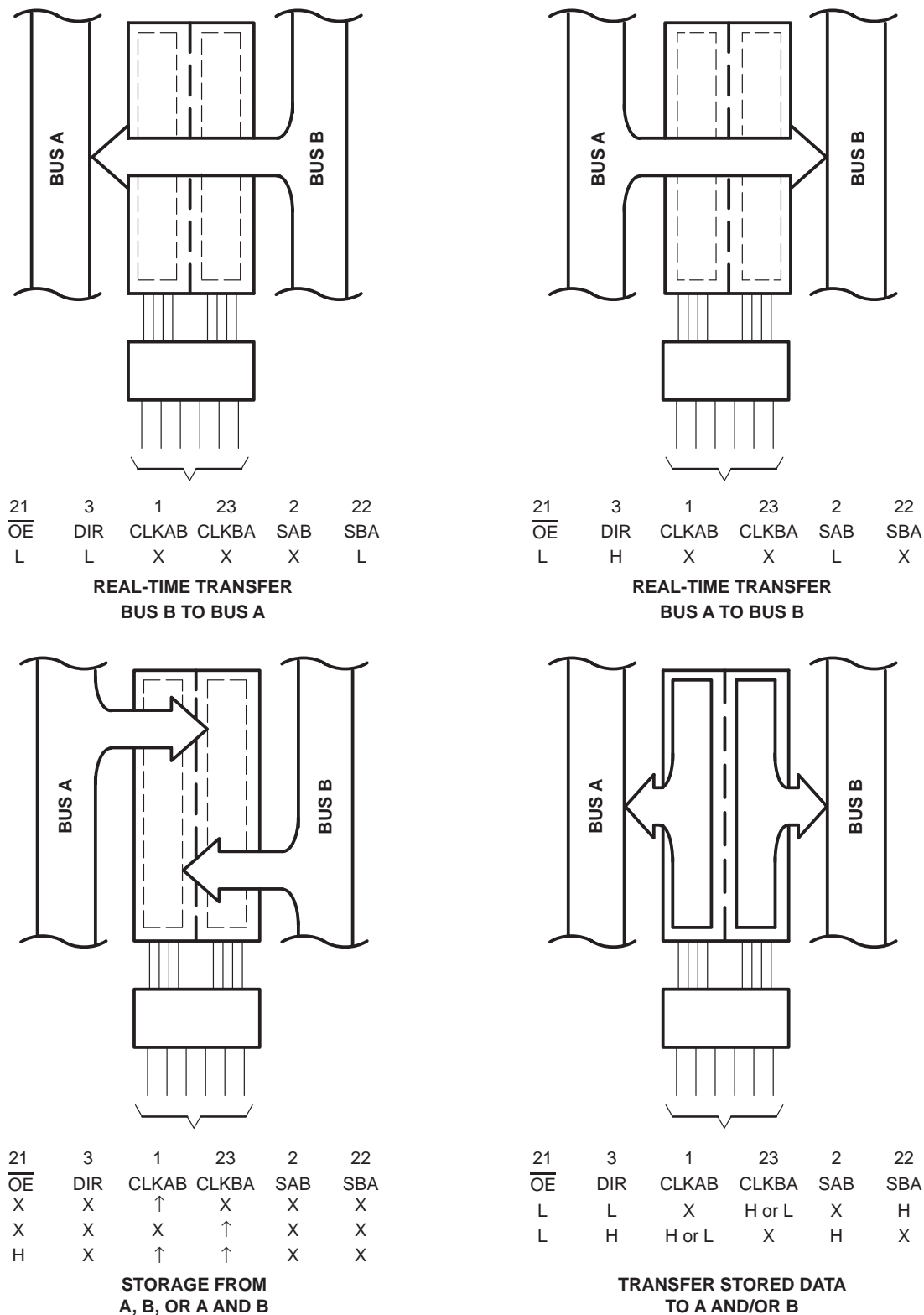
FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

**SN54LVT646, SN74LVT646**  
**3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS**  
**WITH 3-STATE OUTPUTS**

SCBS140D – MAY 1992 – REVISED JULY 1995



**Figure 1. Bus-Management Functions**

Pin numbers shown are for the DB, DW, JT, PW, and W packages.

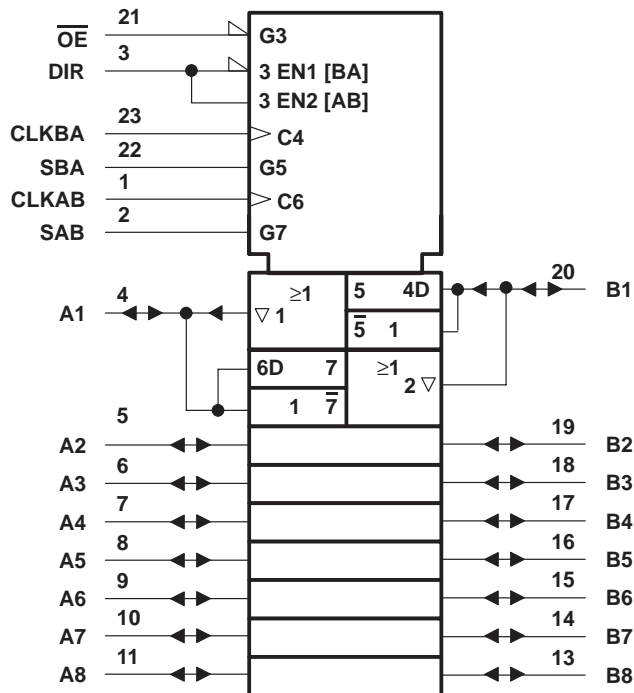
# SN54LVT646, SN74LVT646

## 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

### WITH 3-STATE OUTPUTS

SCBS140D – MAY 1992 – REVISED JULY 1995

#### logic symbol†

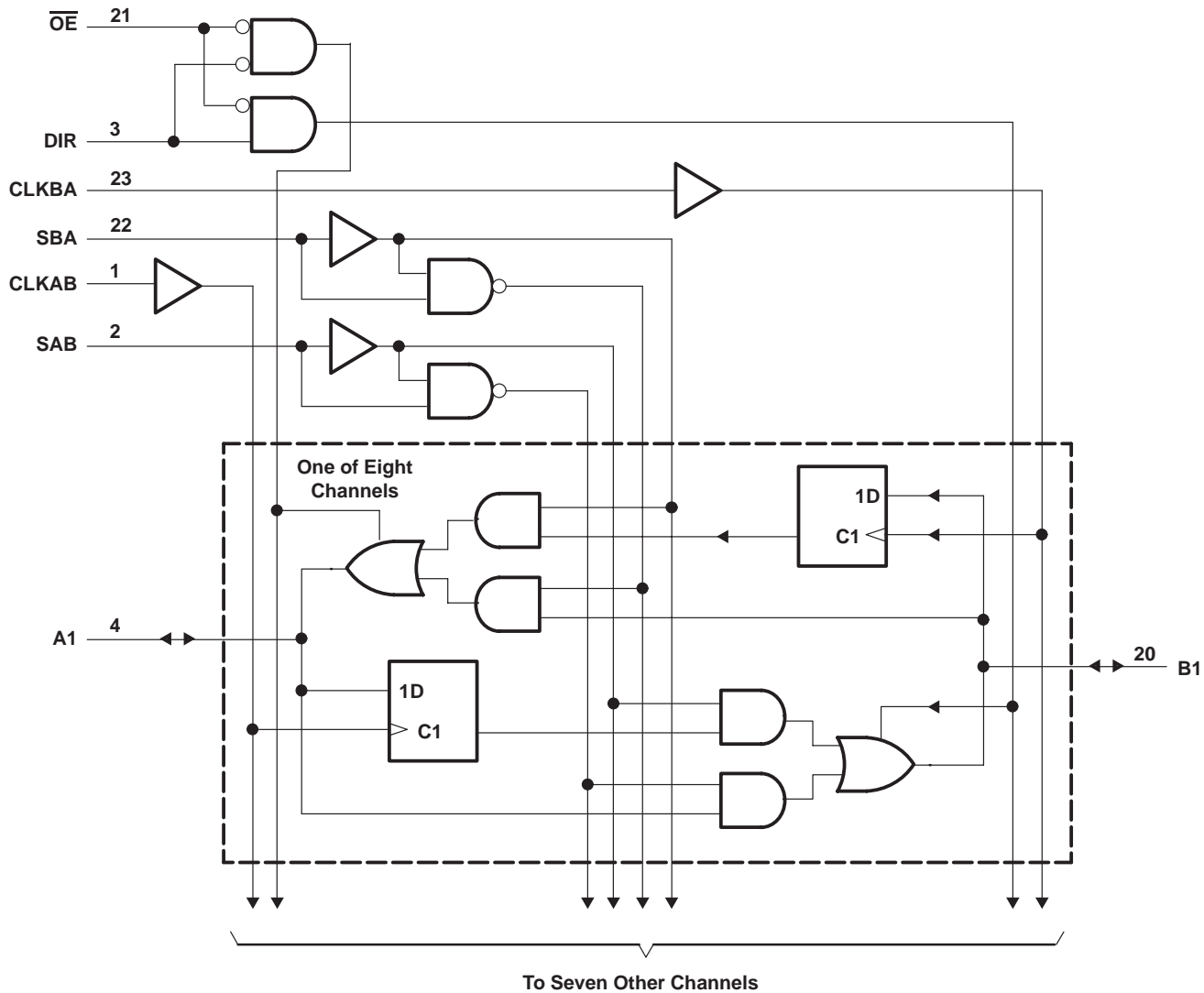


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, PW, and W packages.

SN54LVT646, SN74LVT646  
 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS  
 WITH 3-STATE OUTPUTS

SCBS140D – MAY 1992 – REVISED JULY 1995

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, PW, and W packages.

# SN54LVT646, SN74LVT646

## 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS140D – MAY 1992 – REVISED JULY 1995

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) ....	-0.5 V to 7 V
Current into any output in the low state, $I_O$ : SN54LVT646 .....	96 mA
SN74LVT646 .....	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVT646 .....	48 mA
SN74LVT646 .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DB package .....	0.65 W
DW package .....	1.7 W
PW package .....	0.7 W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

### recommended operating conditions (see Note 4)

		SN54LVT646		SN74LVT646		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



**SN54LVT646, SN74LVT646**  
**3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS**  
**WITH 3-STATE OUTPUTS**

SCBS140D – MAY 1992 – REVISED JULY 1995

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54LVT646		SN74LVT646		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$		-1.2		-1.2		V	
$V_{OH}$	$V_{CC} = \text{MIN to MAX}^\ddagger$ , $I_{OH} = -100\ \mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V	
	$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4		2.4			
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2		2			
$I_{OH} = -32\text{ mA}$								
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\ \mu\text{A}$	0.2		0.2		V	
		$I_{OL} = 24\text{ mA}$	0.5		0.5			
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$	0.4		0.4			
		$I_{OL} = 32\text{ mA}$	0.5		0.5			
		$I_{OL} = 48\text{ mA}$	0.55		0.55			
		$I_{OL} = 64\text{ mA}$						
$I_I$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND		$\pm 1$		$\pm 1$		$\mu\text{A}$	
	$V_{CC} = 0$ or $\text{MAX}^\ddagger$ , $V_I = 5.5\text{ V}$		10		10			
	$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V}$	100		20			
		$V_I = V_{CC}$	1		1			
		$V_I = 0$	-5		-5			
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5\text{ V}$				$\pm 100$		$\mu\text{A}$	
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	75		75		$\mu\text{A}$	
		$V_I = 2\text{ V}$	-75		-75			
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$		1		1		$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$		-1		-1		$\mu\text{A}$	
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND	$I_O = 0$ ,	Outputs high	0.13	0.39	0.13	0.19	$\text{mA}$
			Outputs low	8.8	14	8.8	12	
			Outputs disabled	0.13	0.39	0.13	0.19	
$\Delta I_{CC}^\parallel$	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND		0.3		0.2		$\text{mA}$	
$C_i$	$V_I = 3\text{ V or }0$		4.5		4.5		pF	
$C_{io}$	$V_O = 3\text{ V or }0$		11		11		pF	

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused terminals at  $V_{CC}$  or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

# SN54LVT646, SN74LVT646

## 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS140D – MAY 1992 – REVISED JULY 1995

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		SN54LVT646				SN74LVT646				UNIT
		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	150	0	150	0	150	0	150	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high	1.5	1.5	1.3	1.3				ns
		Data low	2.5	3.0	2	2.4				
t <sub>h</sub>	Hold time, A or B after CLKAB↑ or CLKBA↑	0.9		0.9		0.4		0.4		ns

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT646				SN74LVT646				UNIT
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	
f <sub>max</sub>			150				150				MHz
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	1.2	5.9	6.9		1.8	3.8	5.7	6.7	ns
t <sub>PHL</sub>			1.2	5.9	6.6		2.1	3.8	5.7	6.4	
t <sub>PLH</sub>	A or B	B or A	0.8	4.9	5.6		1.3	2.8	4.7	5.4	ns
t <sub>PHL</sub>			0.6	4.8	5.5		1	2.7	4.6	5.3	
t <sub>PLH</sub>	SBA or SAB‡	A or B	1	6.4	7.4		1.4	3.7	6.2	7.2	ns
t <sub>PHL</sub>			1	6.4	7		1.4	3.8	6.2	6.8	
t <sub>PZH</sub>	OE	A or B	0.6	6	7.4		1	3	5.8	7.2	ns
t <sub>PZL</sub>			0.6	6.2	7.5		1	3.2	6	7.3	
t <sub>PHZ</sub>	OE	A or B	1.4	6.7	7.1		2.3	4.3	6.5	6.9	ns
t <sub>PLZ</sub>			1.4	6.4	6.5		2.2	3.8	5.8	5.9	
t <sub>PZH</sub>	DIR	A or B	0.6	6.7	7.7		1	3.4	6.5	7.5	ns
t <sub>PZL</sub>			0.8	6.5	7.3		1.2	3.4	6.3	7.1	
t <sub>PHZ</sub>	DIR	A or B	0.8	7.4	8.3		1.7	4.1	7.2	8.1	ns
t <sub>PLZ</sub>			1	6.7	7		1.5	3.5	5.8	6.3	

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.



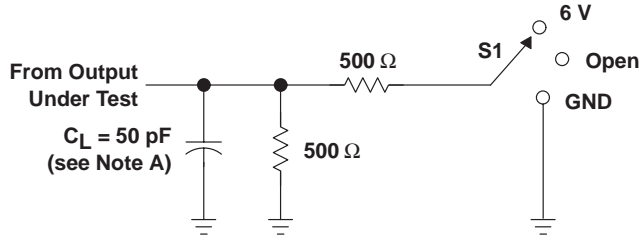


# SN54LVT646, SN74LVT646

## 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

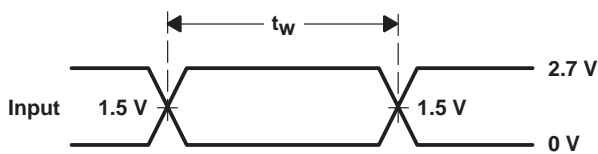
SCBS140D – MAY 1992 – REVISED JULY 1995

### PARAMETER MEASUREMENT INFORMATION

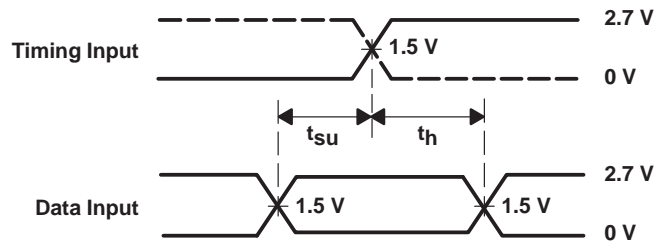


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

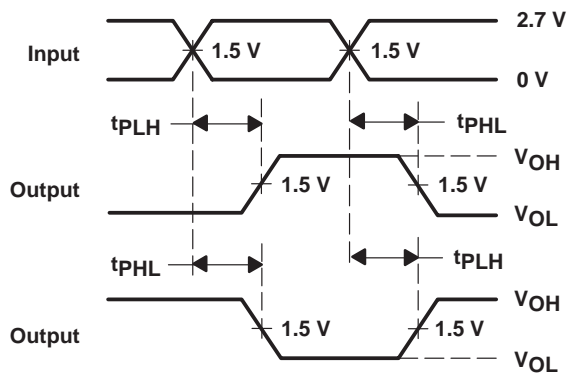
LOAD CIRCUIT FOR OUTPUTS



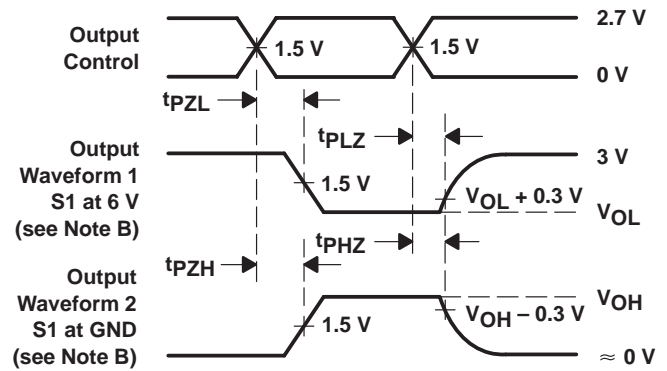
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVT646DBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
SN74LVT646DBR	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
SN74LVT646DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74LVT646DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74LVT646PWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI
SN74LVT646PWR	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI
SNJ54LVT646FK	OBSOLETE	LCCC	FK	28		TBD	Call TI	Call TI
SNJ54LVT646JT	OBSOLETE	CDIP	JT	24		TBD	Call TI	Call TI
SNJ54LVT646W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

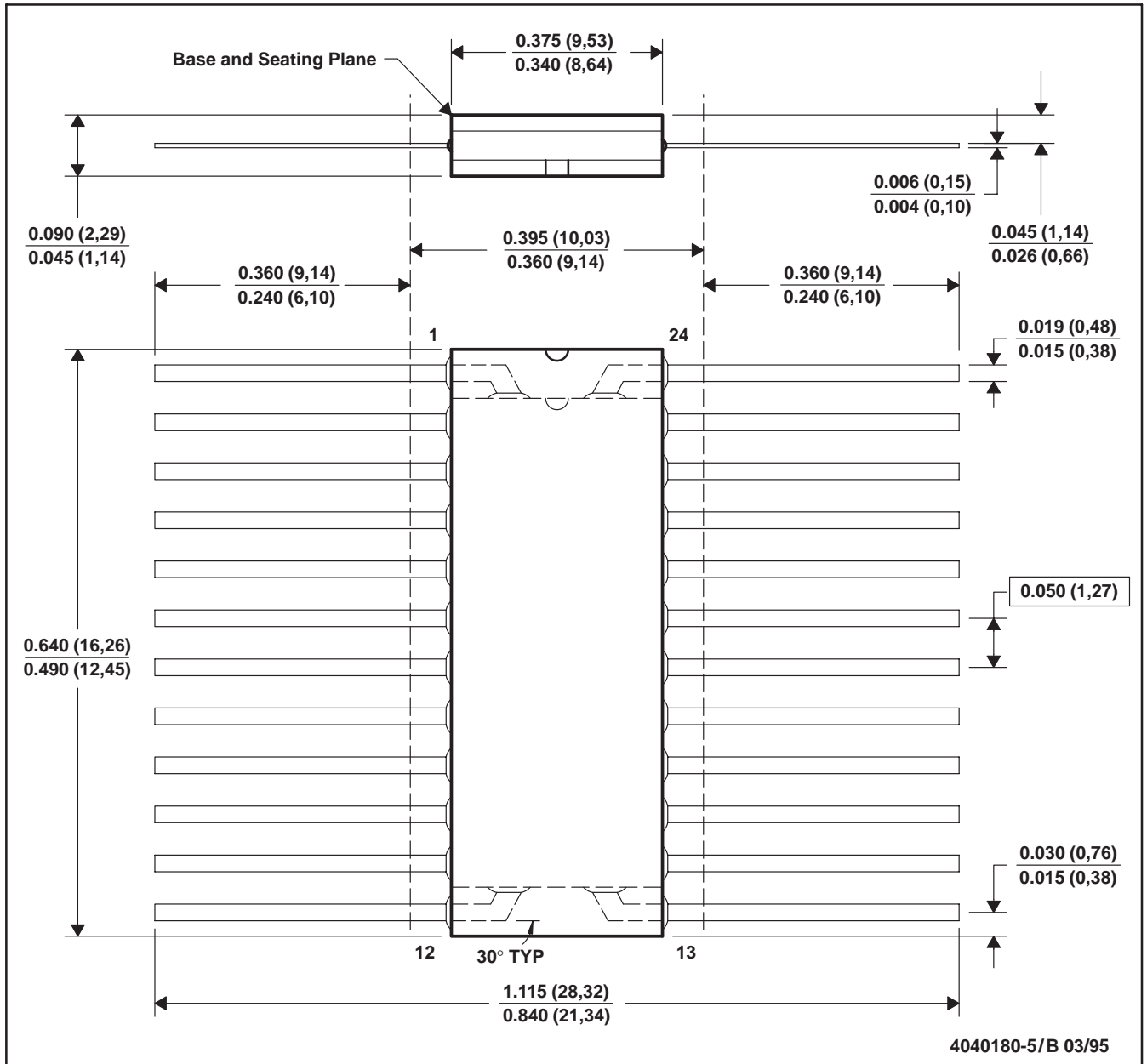
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
  - E. Index point is provided on cap for terminal identification only.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

DW (R-PDSO-G24)

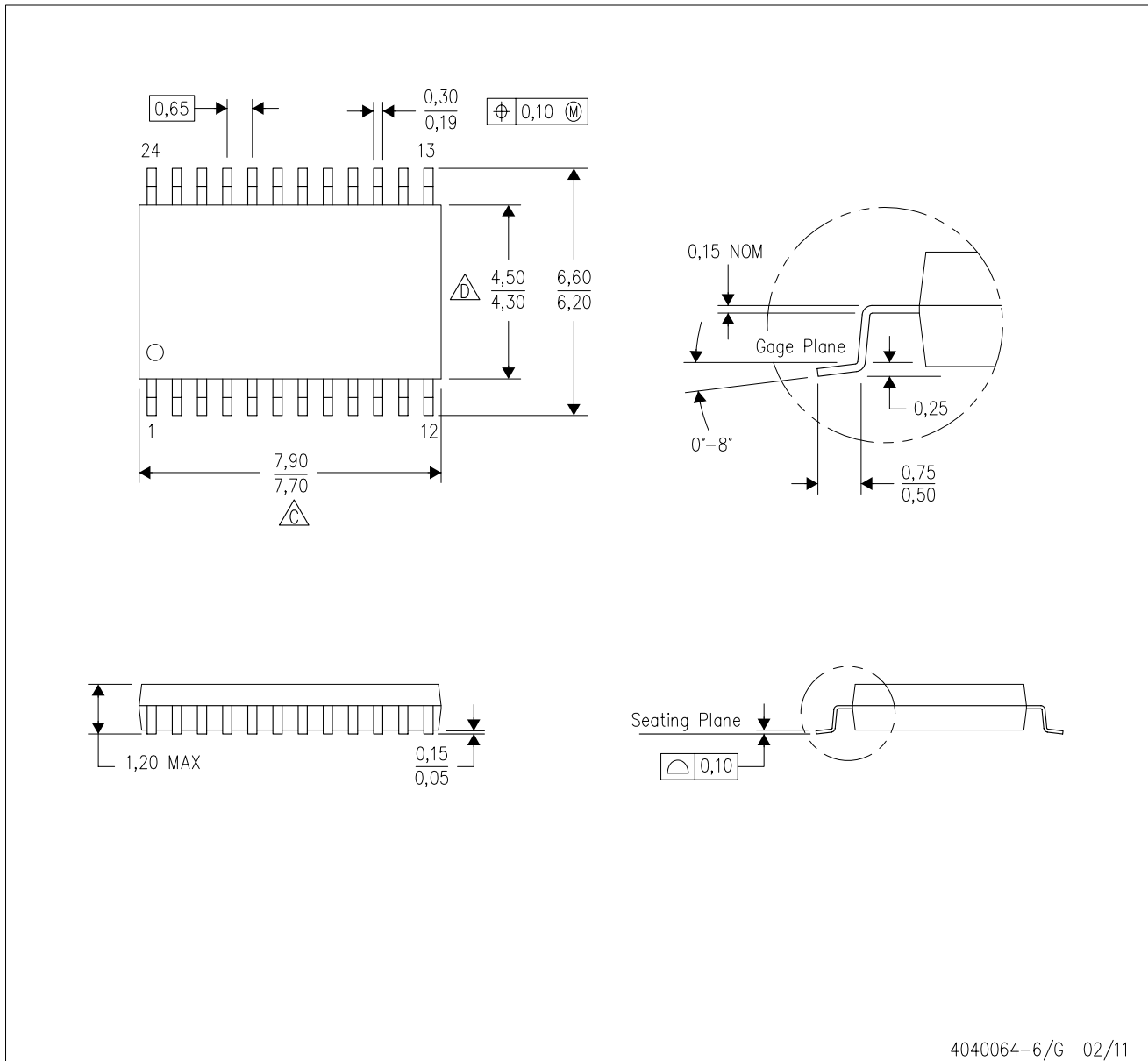
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Transportation and Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>

TI E2E Community Home Page

[e2e.ti.com](http://e2e.ti.com)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2011, Texas Instruments Incorporated