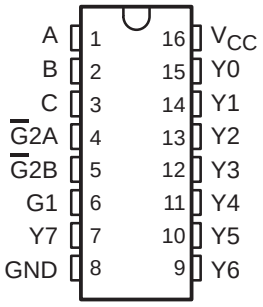
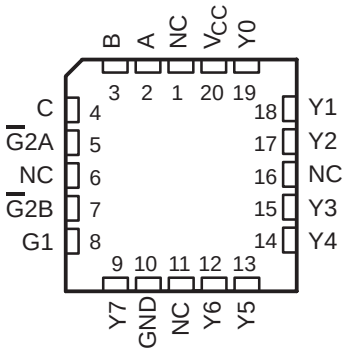
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$, $T_A$ = 25°C**
- **Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) > 2 V at $V_{CC}$, $T_A$ = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

**SN54LV138 . . . J OR W PACKAGE**
**SN74LV138 . . . D, DB, OR PW PACKAGE**
**(TOP VIEW)**




**SN54LV138 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These 3-line to 8-line decoders/demultiplexers are designed for 2.7-V to 5.5-V $V_{CC}$ operation.

The ’LV138 are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

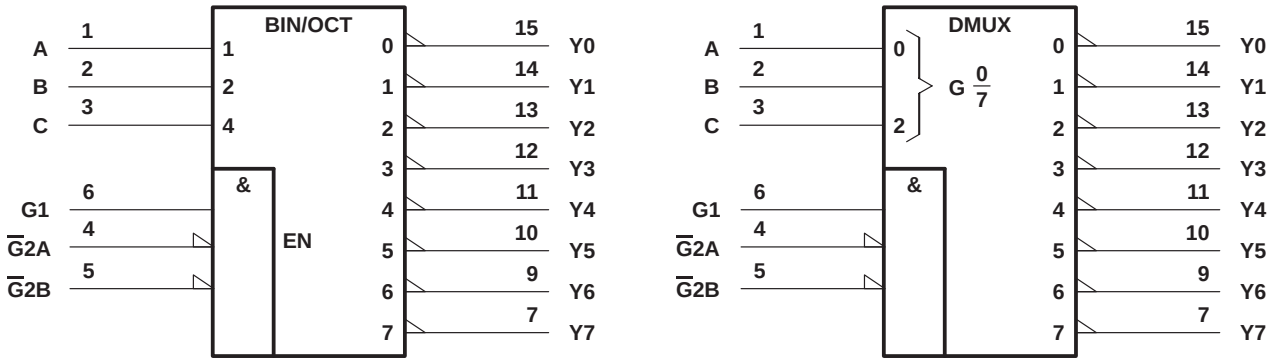
The SN74LV138 is available in TI’s shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV138 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

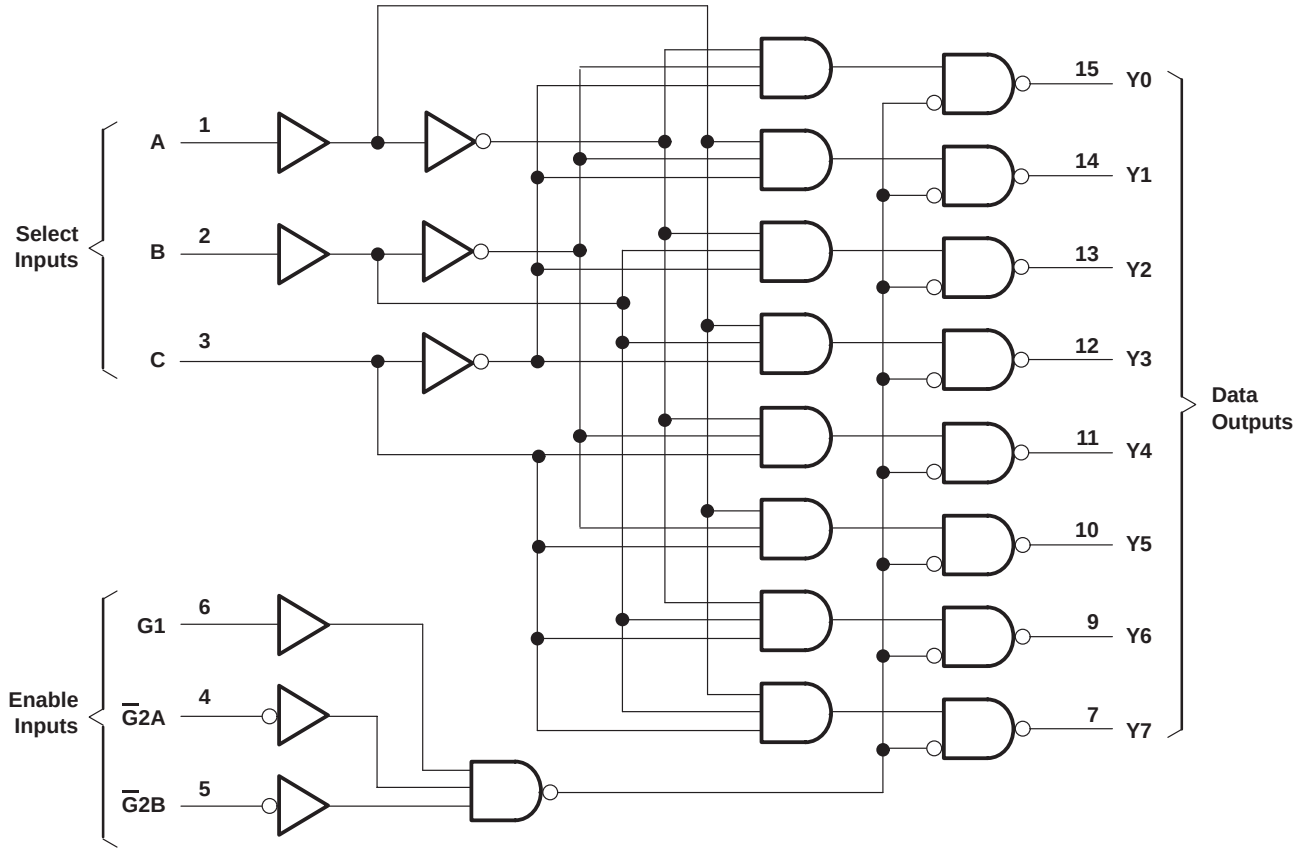
| ENABLE INPUTS | | | SELECT INPUTS | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | $\overline{G}$2A | $\overline{G}$2B | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

## logic symbols (alternatives)†




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): D package . . . . . 1.3 W
DB package . . . . . 0.55 W
PW package . . . . . 0.5 W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

### recommended operating conditions (see Note 4)

| | | | SN54LV138 | | SN74LV138 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 5.5 | 2.7 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | 2 | | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 3.15 | | 3.15 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | | 0.8 | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.7 V to 3.6 V | | –6 | | –6 | mA |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.7 V to 3.6 V | | 6 | | 6 | mA |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | 100 | 0 | 100 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$† | SN54LV138 | | | SN74LV138 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$ = –100 μA | | MIN to MAX | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | $I_{OH}$ = –6 mA | | 3 V | 2.4 | | | 2.4 | | | |
| | $I_{OH}$ = –12 mA | | 4.5 V | 3.6 | | | 3.6 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 μA | | MIN to MAX | | | 0.2 | | | 0.2 | V |
| | $I_{OL}$ = 6 mA | | 3 V | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 12 mA | | 4.5 V | | | 0.55 | | | 0.55 | |
| $I_I$ | $V_I = V_{CC}$ or GND | | 3.6 V | | | ±1 | | | ±1 | μA |
| | | | 5.5 V | | | ±1 | | | ±1 | |
| $I_{CC}$ | $V_I = V_{CC}$ or GND | $I_O$ = 0 | 3.6 V | | | 20 | | | 20 | μA |
| | | | 5.5 V | | | 20 | | | 20 | |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V | Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 500 | | | 500 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | | 3.3 V | | 2.5 | | | 2.5 | | pF |
| | | | 5 V | | 2.1 | | | 2.1 | | |

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LV138 | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V ± 0.5 V | | | $V_{CC}$ = 3.3 V ± 0.3 V | | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A, B, or C | Y | | 8 | 16 | | 10 | 21 | | 26 | ns |
| | Enable | | | 8 | 19 | | 10 | 23 | | 29 | |



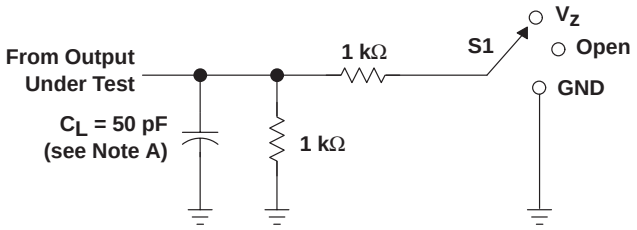
## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LV138 | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V ± 0.5 V | | | $V_{CC}$ = 3.3 V ± 0.3 V | | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A, B, or C | Y | | 8 | 16 | | 10 | 21 | | 26 | ns |
| | Enable | | | 8 | 19 | | 10 | 23 | | 29 | |

## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per channel | $C_L$ = 50 pF, f = 10 MHz | 3.3 V | 47 | pF |
| | | | 5 V | 49 | |

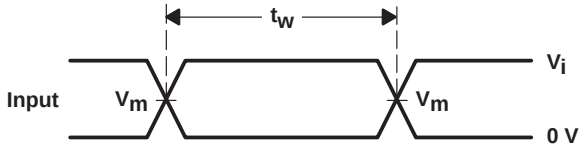
## PARAMETER MEASUREMENT INFORMATION



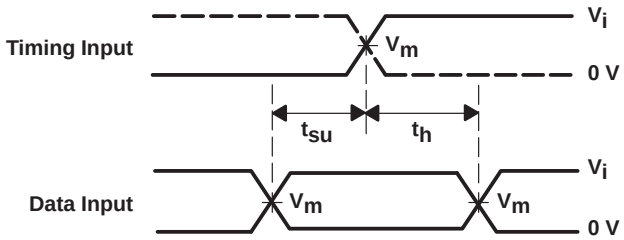

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_z$ |
| $t_{PHZ}/t_{PZH}$ | GND |

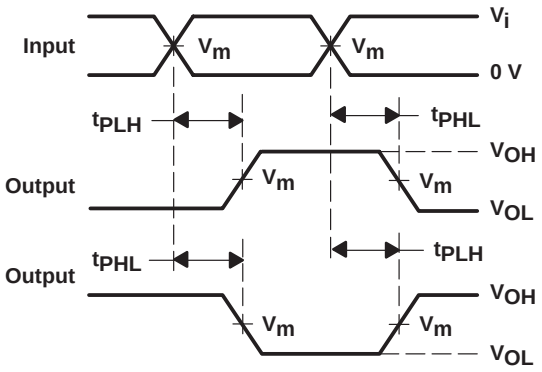
| WAVEFORM CONDITION | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ = 2.7 V to 3.6 V |
|---|---|---|
| $V_m$ | $0.5 \times V_{CC}$ | 1.5 V |
| $V_i$ | $V_{CC}$ | 2.7 V |
| $V_z$ | $2 \times V_{CC}$ | 6 V |



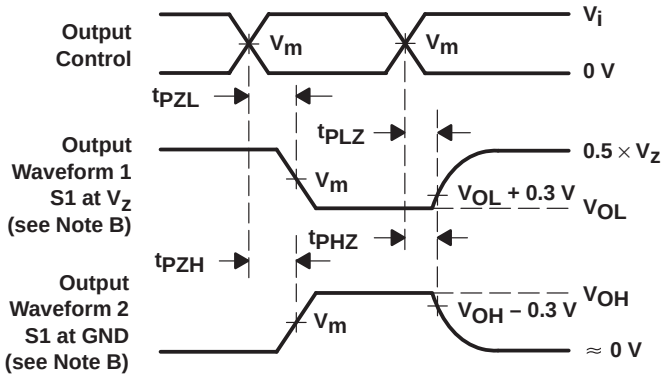

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| SN74LV138D | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI |
| SN74LV138DBLE | OBSOLETE | SSOP | DB | 16 | | TBD | Call TI | Call TI |
| SN74LV138DR | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI |
| SN74LV138PWLE | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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