# OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCLS168

D2804, MARCH 1984–REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **High-Current 3-State Output Drive Bus-Lines Directly or Up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

## description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

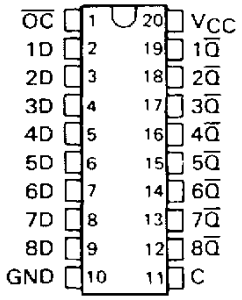
The eight latches are transparent D-type latches. While the enable (C) is high the $\overline{Q}$ outputs will follow the complement of data (D) inputs. When the enable is taken low the outputs will be latched at the inverses of the levels that were set up at the D inputs.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

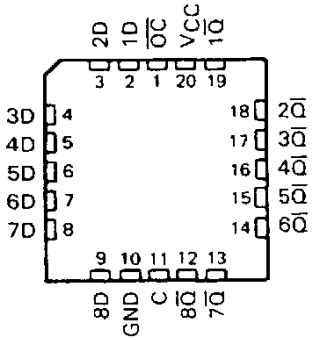
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HCT563 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT563 is characterized for operation from −40°C to 85°C.

**SN54HCT563 . . . J PACKAGE**
**SN74HCT563 . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54HCT563 . . . FK PACKAGE**
**(TOP VIEW)**




**FUNCTION TABLE**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| ENABLE | | | |
| $\overline{OC}$ | C | D | $\overline{Q}$ |
| L | H | H | L |
| L | H | L | H |
| L | L | X | $\overline{Q}_0$ |
| H | X | X | Z |

**PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.**

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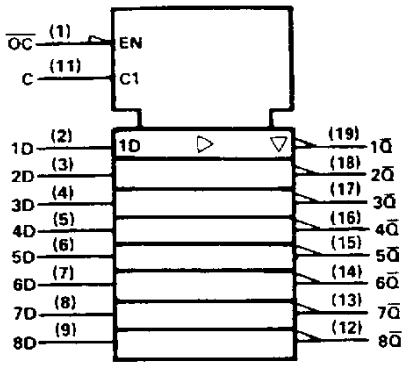
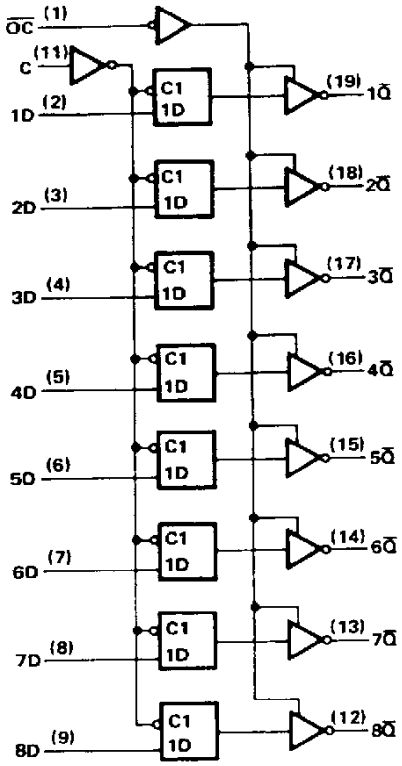
## logic symbol†




†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±35 mA
Continuous current through $V_{CC}$ or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | SN54HCT563 | | | SN74HCT563 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 0 | | 0.8 | 0 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $t_t$ | Input transition (rise and fall) times | | 0 | | 500 | 0 | | 500 | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | −40 | | 85 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT563 | | SN74HCT563 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I = V_{IH}$ or $V_{IL}$, $I_{OH}$ = −20 μA | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | V |
| | $V_I = V_{IH}$ or $V_{IL}$, $I_{OH}$ = −6 mA | 4.5 V | 3.98 | 4.30 | | 3.7 | | 3.84 | | |
| $V_{OL}$ | $V_I = V_{IH}$ or $V_{IL}$, $I_{OL}$ = 20 μA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | $V_I = V_{IH}$ or $V_{IL}$, $I_{OL}$ = 6 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I = V_{CC}$ or 0 | 5.5 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{OZ}$ | $V_O = V_{CC}$ or 0 | 5.5 V | | ±0.01 | ±0.5 | | ±10 | | ±5 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or 0, $I_O$ = 0 | 5.5 V | | | 8 | | 160 | | 80 | μA |
| $\Delta I_{CC}$‡ | One input at 0.5 V or 2.4 V<br>Other inputs at 0 V or $V_{CC}$ | 5.5 V | | 1.4 | 2.4 | | 3 | | 2.9 | mA |
| $C_I$ | | 4.5 to 5.5 V | | 3 | 10 | | 10 | | 10 | pF |

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to $V_{CC}$.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

| | | $V_{CC}$ | $T_A$ = 25°C | | SN54HCT563 | | SN74HCT563 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, enable C high | 4.5 V | 20 | | 30 | | 25 | | ns |
| | | 5.5 V | 17 | | 27 | | 23 | | |
| $t_{su}$ | Setup time, data before enable C↓ | 4.5 V | 10 | | 15 | | 13 | | ns |
| | | 5.5 V | 9 | | 14 | | 12 | | |
| $t_h$ | Hold time, data afer enable C↓ | 4.5 V | 5 | | 5 | | 5 | | ns |
| | | 5.5 V | 5 | | 5 | | 5 | | |

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L$ = 50 pF (see Note 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT563 | | SN74HCT563 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | $\overline{Q}$ | 4.5 V | | 28 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 24 | 32 | | 48 | | 40 | |
| $t_{pd}$ | C | Any $\overline{Q}$ | 4.5 V | | 30 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 28 | 32 | | 48 | | 40 | |
| $t_{en}$ | $\overline{OC}$ | Any $\overline{Q}$ | 4.5 V | | 28 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 25 | 32 | | 48 | | 40 | |
| $t_{dis}$ | $\overline{OC}$ | Any $\overline{Q}$ | 4.5 V | | 25 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 24 | 32 | | 48 | | 40 | |
| $t_t$ | | Any $\overline{Q}$ | 4.5 V | | 10 | 12 | | 18 | | 15 | ns |
| | | | 5.5 V | | 9 | 11 | | 16 | | 14 | |

| | | | |
|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per latch | No load, $T_A$ = 25°C | 50 pF typ |

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L$ = 150 pF (see Note 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT563 | | SN74HCT563 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | $\overline{Q}$ | 4.5 V | | 36 | 52 | | 79 | | 65 | ns |
| | | | 5.5 V | | 32 | 47 | | 71 | | 59 | |
| $t_{pd}$ | C | Any $\overline{Q}$ | 4.5 V | | 40 | 52 | | 79 | | 65 | ns |
| | | | 5.5 V | | 38 | 47 | | 71 | | 59 | |
| $t_{en}$ | $\overline{OC}$ | Any $\overline{Q}$ | 4.5 V | | 35 | 52 | | 79 | | 65 | ns |
| | | | 5.5 V | | 29 | 47 | | 71 | | 59 | |
| $t_t$ | | Any $\overline{Q}$ | 4.5 V | | 18 | 42 | | 63 | | 53 | ns |
| | | | 5.5 V | | 16 | 38 | | 57 | | 48 | |

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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