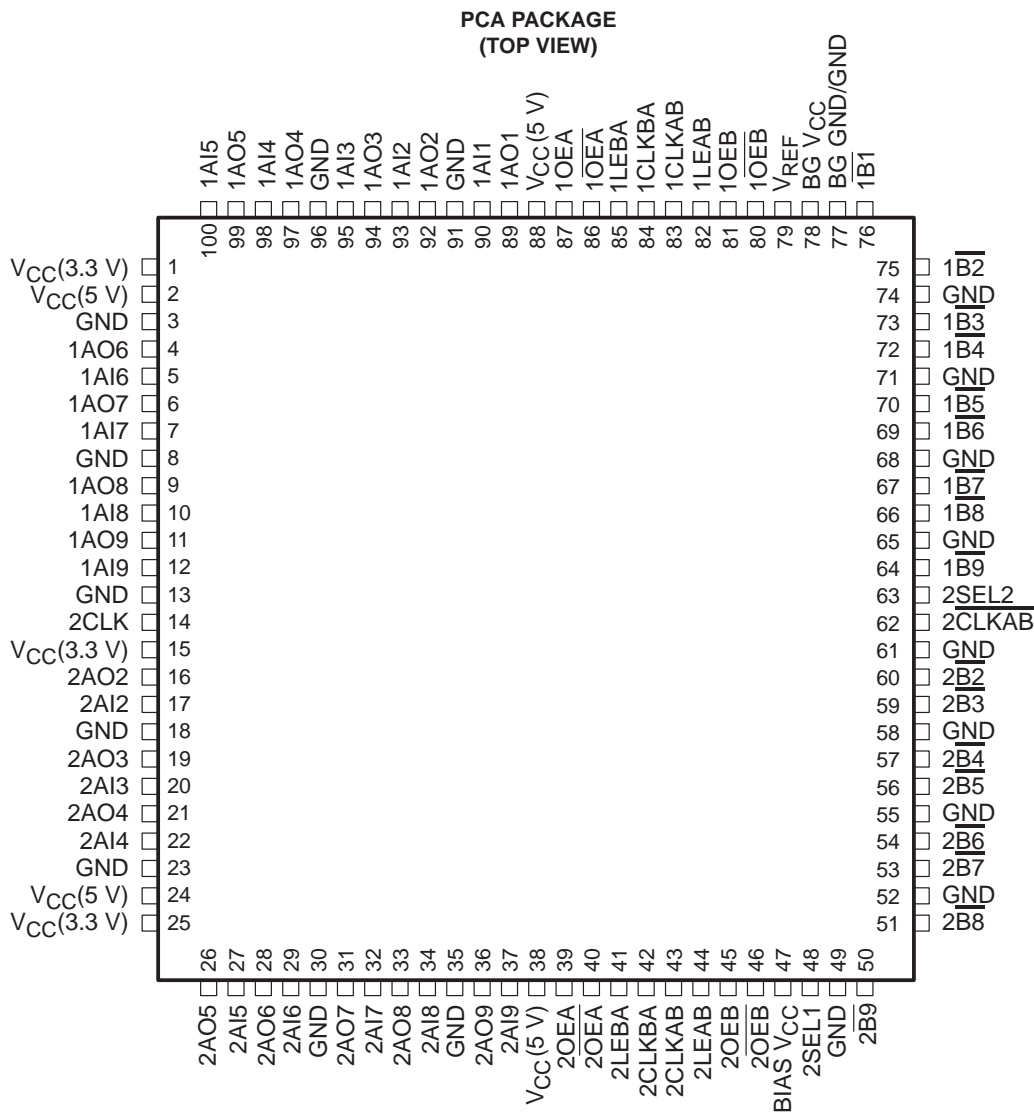


SN74FB1653

17-BIT LVTTTL/BTL UNIVERSAL STORAGE TRANSCEIVER WITH BUFFERED CLOCK LINE

SCBS702H – AUGUST 1997 – REVISED MARCH 2004

- Compatible With IEEE Std 1194.1-1991 (BTL)
- LVTTTL A Port, Backplane Transceiver Logic (BTL) \bar{B} Port
- Open-Collector \bar{B} -Port Outputs Sink 100 mA
- \bar{B} -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage
- High-Impedance State During Power Up and Power Down
- Selectable Clock Delay
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination
- BIAS V_{CC} Minimizes Signal Distortion During Live Insertion/Withdrawal



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

SN74FB1653

17-BIT LVTTTL/BTL UNIVERSAL STORAGE TRANSCEIVER WITH BUFFERED CLOCK LINE

SCBS702H – AUGUST 1997 – REVISED MARCH 2004

description/ordering information

The SN74FB1653 contains an 8-bit and a 9-bit transceiver with a buffered clock. The clock and transceivers are designed to translate signals between LVTTTL and BTL environments. The device is designed specifically to be compatible with IEEE Std 1194.1-1991 (BTL).

The A port operates at LVTTTL signal levels. The A outputs reflect the inverse of the data at the \bar{B} port when the A-port output enable (OEA) is high. When OEA is low or when $V_{CC}(5\text{ V})$ typically is less than 2.5 V, the A outputs are in the high-impedance state.

The \bar{B} port operates at BTL signal levels. The open-collector \bar{B} ports are specified to sink 100 mA. Two output enables (OEB and \overline{OEB}) are provided for the \bar{B} outputs. When OEB is low, \overline{OEB} is high, or $V_{CC}(5\text{ V})$ typically is less than 2.5 V, the \bar{B} port is turned off.

The clock-select (2SEL1 and 2SEL2) inputs are used to configure the TTL-to-BTL clock paths and delays (refer to the *MUX-MODE DELAY* table).

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when $V_{CC}(5\text{ V})$ is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

V_{REF} is an internally generated voltage source. It is recommended that V_{REF} be decoupled with an external 0.1- μF capacitor.

Enhanced heat-dissipation techniques should be used when operating this device from A1 to A0 at frequencies greater than 50 MHz, or from A1 to \bar{B} or \bar{B} to A0 at frequencies greater than 100 MHz.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TQFP – PCA	Tube	SN74FB1653PCA	FB1653

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

TRANSCEIVER

INPUTS				FUNCTION
\overline{OEA}	OEA	OEB	\overline{OEB}	
X	X	H	L	\bar{A} data to B bus
L	H	X	X	\bar{B} data to A bus
L	H	H	L	\bar{A} data to B bus, \bar{B} data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

STORAGE MODE

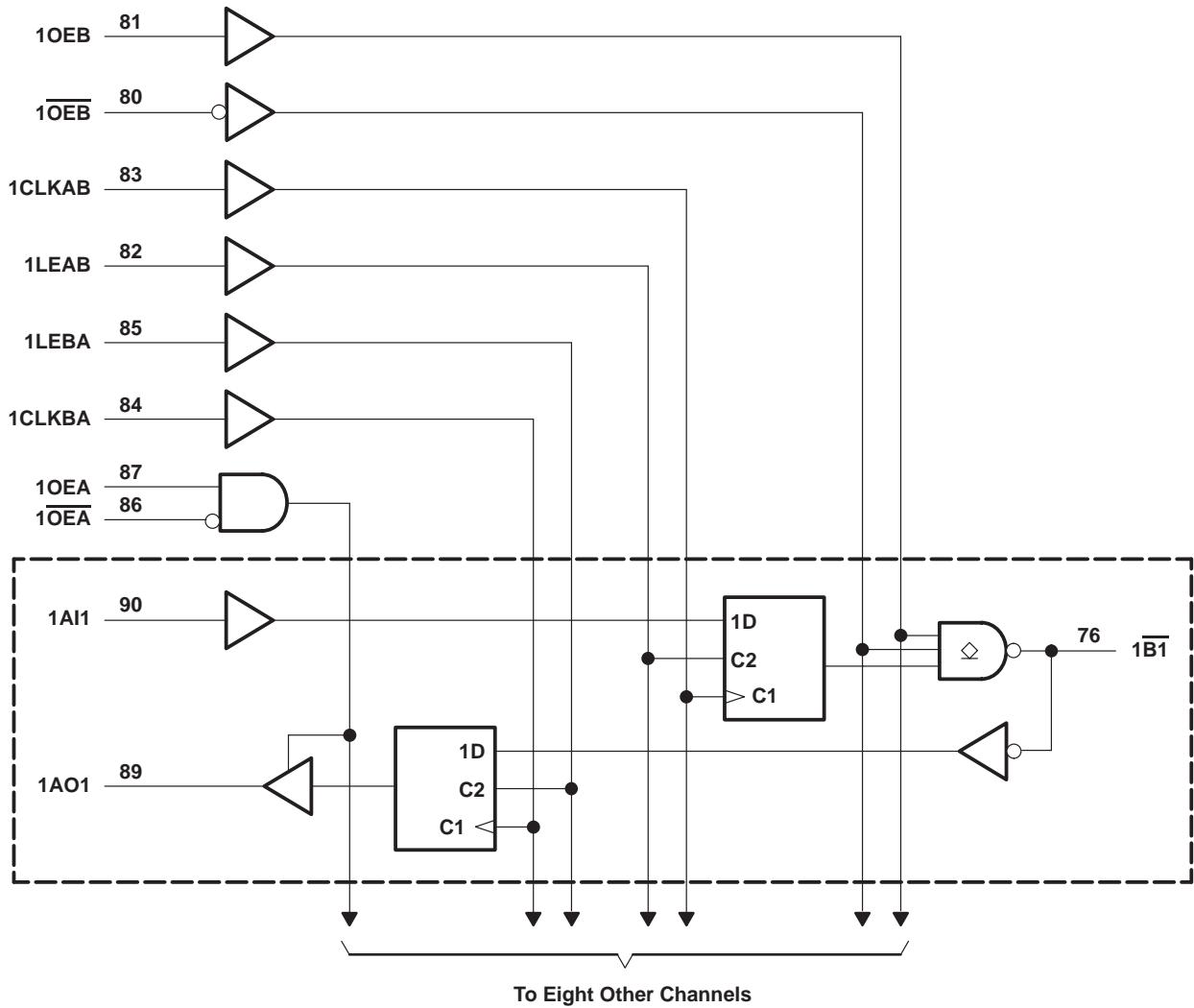
INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage



SN74FB1653
17-BIT LVTTTL/BTL UNIVERSAL STORAGE TRANSCIEVER
WITH BUFFERED CLOCK LINE

SCBS702H - AUGUST 1997 - REVISED MARCH 2004

functional block diagram



SN74FB1653

17-BIT LVTTTL/BTL UNIVERSAL STORAGE TRANSCIEVER WITH BUFFERED CLOCK LINE

SCBS702H – AUGUST 1997 – REVISED MARCH 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range: $V_{CC}(5\text{ V})$, BIAS V_{CC} , BG V_{CC}	–0.5 V to 7 V
$V_{CC}(3.3\text{ V})$	–0.5 V to 4.6 V
Input voltage range, V_I : Except \overline{B} port	–1.2 V to 7 V
\overline{B} port	–1.2 V to 3.5 V
Input clamp current, I_{IK} : Except \overline{B} port	–40 mA
\overline{B} port	–18 mA
Voltage range applied to any \overline{B} output in the disabled or power-off state	–0.5 V to 3.5 V
Voltage range applied to any output in the high state	–0.5 V to V_{CC}
Current applied to any single output in the low state: A port	48 mA
\overline{B} port	200 mA
Package thermal impedance, θ_{JA} (see Note 1)	22°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC} , BG V_{CC} , BIAS V_{CC}	Supply voltage	4.5	5	5.5	V
$V_{CC}(3.3\text{ V})$	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	\overline{B} port	1.62	2.3	V
		Except \overline{B} port	2		
V_{IL}	Low-level input voltage	\overline{B} port	0.75	1.47	V
		Except \overline{B} port		0.8	
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current	AO port		24	mA
		\overline{B} port		100	
T_A	Operating free-air temperature	0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to $V_{CC}(5\text{ V})$ or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74FB1653

17-BIT LVTTTL/BTL UNIVERSAL STORAGE TRANSCEIVER WITH BUFFERED CLOCK LINE

SCBS702H – AUGUST 1997 – REVISED MARCH 2004

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	\overline{B} port	V _{CC} (5 V) = 4.5 V, V _{CC} (3.3 V) = 3.3 V	I _I = -18 mA			-1.2	V
	Except \overline{B} port		I _I = -40 mA			-0.5	
V _{OH}	AO port	V _{CC} (5 V) = 4.5 V, V _{CC} (3.3 V) = 3 V	I _{OH} = -3 mA	2.5			V
V _{OL}	AO port	V _{CC} (5 V) = 4.5 V, V _{CC} (3.3 V) = 3 V	I _{OL} = 24 mA	0.35		0.5	V
	\overline{B} port	V _{CC} (5 V) = 4.5 V, V _{CC} (3.3 V) = 3 V	I _{OL} = 80 mA I _{OL} = 100 mA	0.75		1.1 1.15	
I _I	Except \overline{B} port	V _{CC} (5 V) = 5.5 V, V _{CC} (3.3 V) = 3.6 V	V _I = 5.5 V			50	μA
I _{IH} ‡	Except \overline{B} port	V _{CC} (5 V) = 5.5 V, V _{CC} (3.3 V) = 3.6 V	V _I = 2.7 V			50	μA
I _{IL} ‡	Except \overline{B} port	V _{CC} (5 V) = 5.5 V, V _{CC} (3.3 V) = 3.6 V	V _I = 0.5 V			-50	μA
	\overline{B} port	V _{CC} (5 V) = 5.5 V, V _{CC} (3.3 V) = 3.6 V	V _I = 0.75 V			-100	
I _{OH}	\overline{B} port	V _{CC} (5 V) = 0 to 5.5 V, V _{CC} (3.3 V) = 3.6 V	V _O = 2.1 V			100	μA
I _{OZH}	AO port	V _{CC} (5 V) = 5.5 V, V _{CC} (3.3 V) = 3.6 V	V _O = 2.7 V			50	μA
I _{OZL}	AO port	V _{CC} (5 V) = 5.5 V, V _{CC} (3.3 V) = 3.6 V	V _O = 0.5 V			-50	μA
I _{OZPU}	AO port	V _{CC} = 0 to 2.1 V,	V _O = 0.5 V to 2.7 V			-50	μA
I _{OZPD}	AO port	V _{CC} = 2.1 V to 0,	V _O = 0.5 V to 2.7 V			-50	μA
I _{CC} (5 V)	AI port to \overline{B} port	V _{CC} (5 V) = 5.5 V, V _{CC} (3.3 V) = 3.3 V	I _O = 0			145	mA
	\overline{B} port to AO port					130	
	Outputs disabled					120	
I _{CC} (3.3 V)	\overline{B} port to AO port	V _{CC} (5 V) = 5.5 V, V _{CC} (3.3 V) = 3.3 V	I _O = 0			1	mA
C _i	Control and AI inputs	V _I = 0.5 V or 2.5 V			6.5		pF
C _o	AO port	V _O = 0.5 V or 2.5 V			3.5		pF
C _{io}	\overline{B} port per IEEE Std 1194.1-1991	V _{CC} (5 V) = 0 to 5.5 V, V _{CC} (3.3 V) = 3.3 V	V _{CC} (3.3 V) = 3.3 V			6.5	pF

† All typical values are at V_{CC}(5 V) = 5 V and V_{CC}(3.3 V) = 3.3 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.



SN74FB1653
17-BIT LVTTTL/BTL UNIVERSAL STORAGE TRANSCEIVER
WITH BUFFERED CLOCK LINE

SCBS702H – AUGUST 1997 – REVISED MARCH 2004

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		$V_{CC}(5\text{ V}) = 0$ to 4.5 V, $V_{CC}(3.3\text{ V}) = 3.3\text{ V}$	$V_B = 0$ to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	450		μA
		$V_{CC}(5\text{ V}) = 4.5\text{ V}$ to 5.5 V, $V_{CC}(3.3\text{ V}) = 3.3\text{ V}$		10		
V_O	\overline{B} port	$V_{CC}(5\text{ V}) = 0$, $V_{CC}(3.3\text{ V}) = 0\text{ V}$	V_I (BIAS V_{CC}) = 5 V	1.62	2.1	V
I_O	\overline{B} port	$V_{CC}(5\text{ V}) = 0$, $V_{CC}(3.3\text{ V}) = 0\text{ V}$	$V_B = 1\text{ V}$, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		μA
		$V_{CC}(5\text{ V}) = 0$ to 2.2 V, $V_{CC}(3.3\text{ V}) = 3.3\text{ V}$	OEB = 0 to 5 V	100		
		$V_{CC}(5\text{ V}) = 0$ to 5.5 V, $V_{CC}(3.3\text{ V}) = 3.3\text{ V}$	OEB = 0 to 0.8 V	1		mA

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		MIN	MAX	UNIT	
f_{clock}	Clock frequency	90		MHz	
t_w	Pulse duration	LE high	3		ns
		CLK high or low	3		
t_{su}	Setup time	AI or \overline{B} before LE \downarrow	3.5		ns
		AI or \overline{B} before CLK \uparrow	3.5		
t_h	Hold time	AI or \overline{B} after LE \downarrow	1		ns
		AI or \overline{B} after CLK \uparrow	0.7		



**17-BIT LVTTL/BTL UNIVERSAL STORAGE TRANSCEIVER
WITH BUFFERED CLOCK LINE**

SCBS702H – AUGUST 1997 – REVISED MARCH 2004

switching characteristics over recommended operating free-air temperature range,
 $V_{CC}(5\text{ V}) = 5\text{ V} \pm 0.5\text{ V}$ and $V_{CC}(3.3\text{ V}) = 3.3\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{\max}			90		MHz
t_{PLH}	AI	\overline{B}	1.8	6.2	ns
t_{PHL}			2.9	6.6	
t_{PLH}	LEAB	\overline{B}	2.7	6.9	ns
t_{PHL}			3.5	7.3	
t_{PLH}	CLKAB	\overline{B}	2.3	6.4	ns
t_{PHL}			2.9	6.7	
t_{PLH}	2CLKAB (no delay)	$\overline{2CLKAB}$	2.3	6	ns
t_{PHL}			2.9	6.7	
t_{PLH}	2CLKAB (delay2)	$\overline{2CLKAB}$	4.5	9.5	ns
t_{PHL}			4.5	9.5	
t_{PLH}	2CLKAB (delay3)	$\overline{2CLKAB}$	9.3	15.4	ns
t_{PHL}			9.3	15.4	
t_{PLH}	\overline{B}	AO	2	6.5	ns
t_{PHL}			2	6.5	
t_{PLH}	LEBA	AO	1.8	6.3	ns
t_{PHL}			1.8	6.3	
t_{PLH}	CLKBA	AO	1.8	6.3	ns
t_{PHL}			1.8	6.3	
t_{PLH}	$\overline{2CLKAB}$ (delay1)	2CLK	5.7	12.3	ns
t_{PHL}			5.7	12.3	
t_{PLH}	$\overline{2CLKAB}$ (no delay)	2CLK	2	6.5	ns
t_{PHL}			2	6.5	
t_{PLH}	OEB or \overline{OEB}	\overline{B}	2.6	7	ns
t_{PHL}			2.6	7	
t_{PZH}	OEA or \overline{OEA}	AO	1.4	5.5	ns
t_{PZL}			1.4	5.5	
t_{PHZ}	OEA or \overline{OEA}	AO	1.4	6.5	ns
t_{PLZ}			1.4	5.8	
$t_{sk(p)}^{\dagger}$	Pulse skew, AI to \overline{B} or \overline{B} to AO		1.6		ns
	Pulse skew, $\overline{2CLKAB}$ to 2CLK		1.8		
$t_{sk(p)}$	Pulse skew, CLKAB to \overline{B} or CLKBA to AO		1.5		ns
	Pulse skew, CLKAB to $\overline{2CLKAB}$		1.4		
$t_{sk(HL)}, t_{sk(LH)}^{\dagger}$	Output skew, AI to \overline{B} or \overline{B} to AO		1		ns
$t_{sk(o)}^{\ddagger}$	Output skew, nondelayed mode for $\overline{2CLKAB}$, CLKAB to AO		1		ns
	Output skew, nondelayed mode for $\overline{2CLKAB}$, CLKAB to \overline{B} and $\overline{2CLKAB}$		1		
$t_{sk(o)}^{\ddagger}$	Output skew, nondelayed mode for $\overline{2CLKAB}$, CLKAB to \overline{B} and $\overline{2CLKAB}$		1.5		ns
t_t	Transition time, \overline{B} outputs (1.3 V to 1.8 V)		0.5	4.6	ns
	Transition time, AO outputs (10% to 90%)		0.4	4.2	
t_{PR}	\overline{B} -port input pulse rejection		1		ns

\dagger Skew values are applicable for through mode only, with single-output switching.

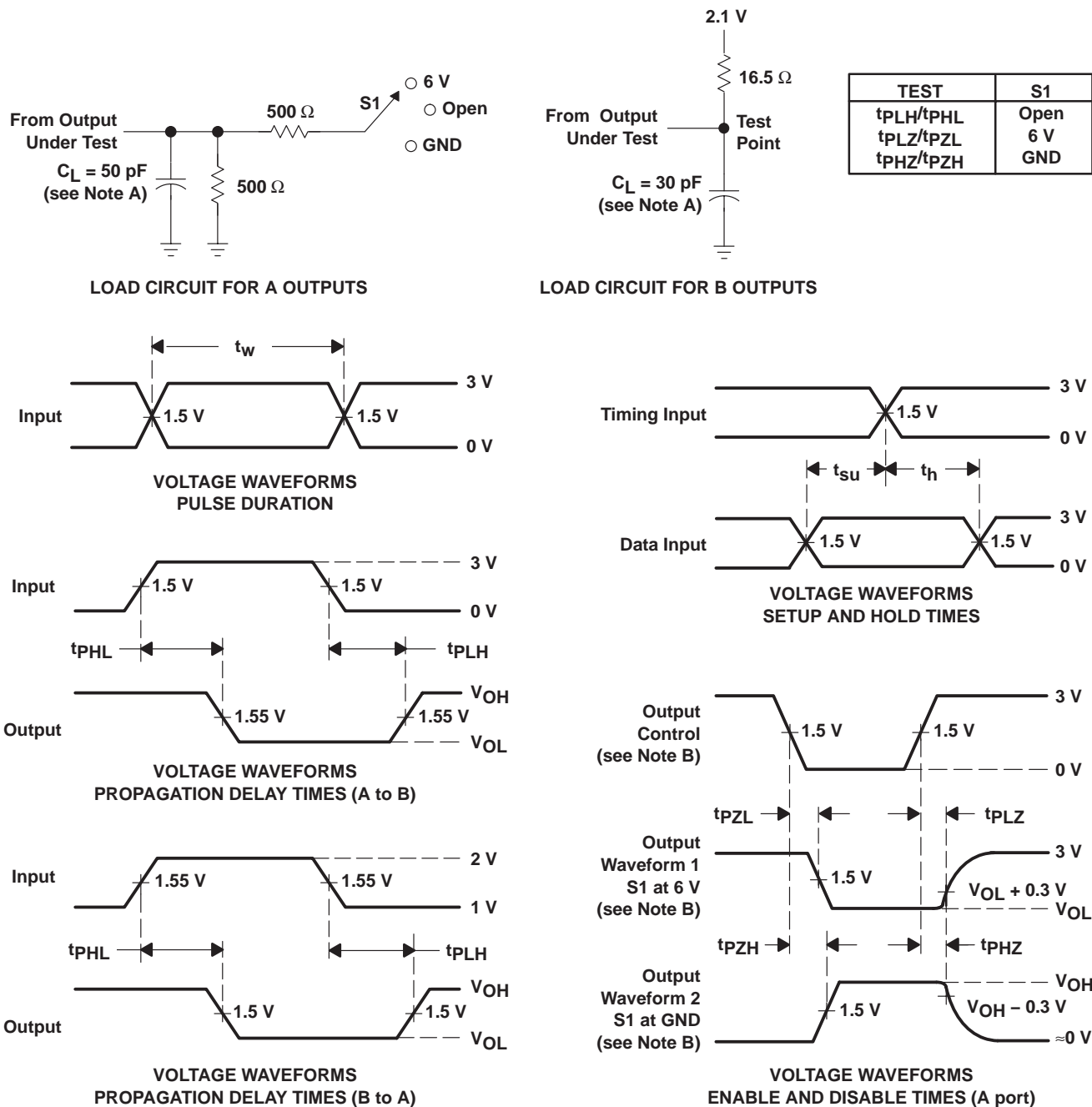
\ddagger Skew values are applicable for CLK mode only, with all outputs simultaneously switching high-to-low or low-to-high.

SN74FB1653

17-BIT LVTTTL/BTL UNIVERSAL STORAGE TRANSCIEVER WITH BUFFERED CLOCK LINE

SCBS702H – AUGUST 1997 – REVISED MARCH 2004



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: TTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns; BTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 1$ ns, $t_f \leq 1$ ns.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74FB1653PCA	ACTIVE	HLQFP	PCA	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	FB1653	
SN74FB1653PCAG4	ACTIVE	HLQFP	PCA	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	FB1653	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

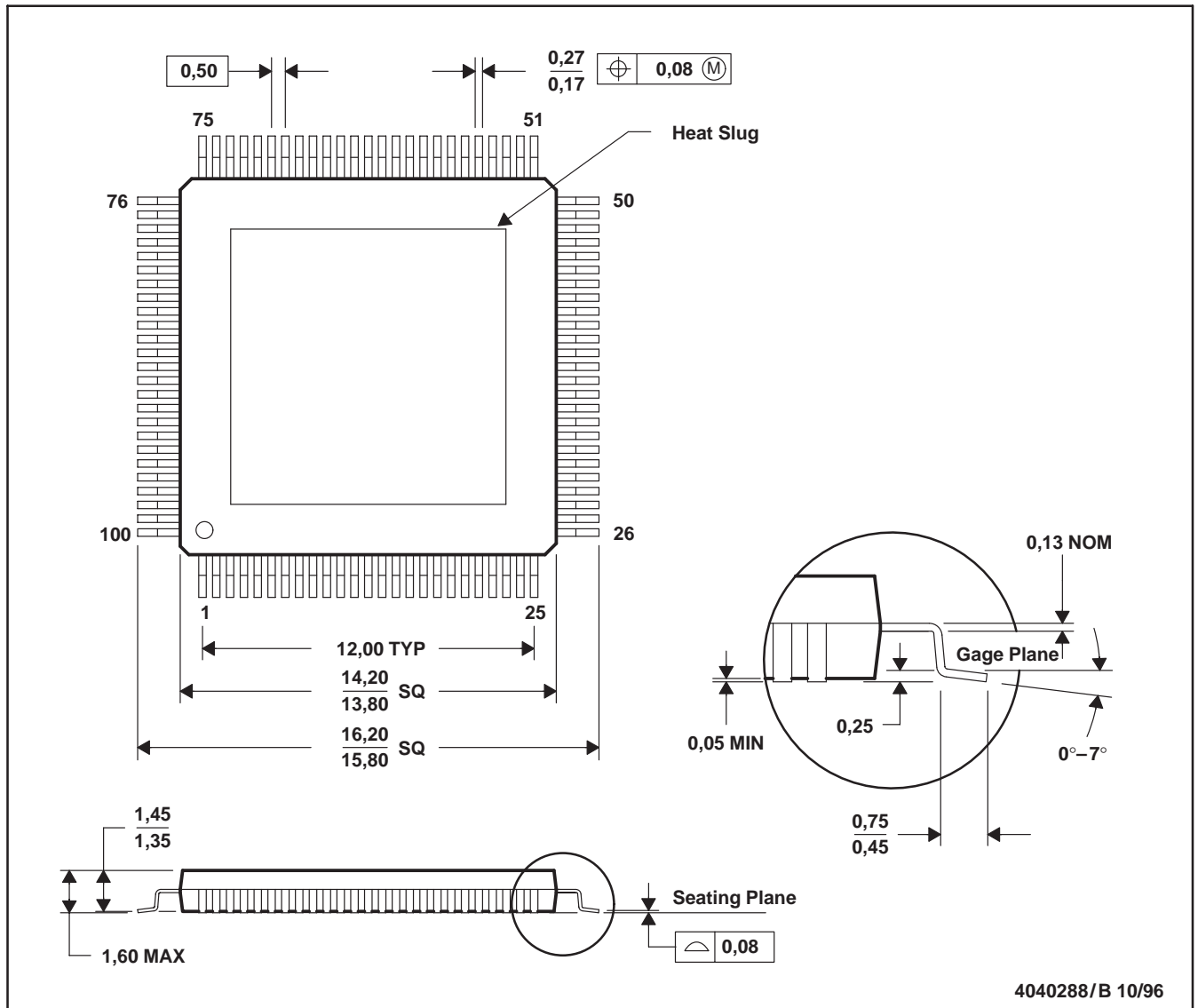
(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PCA (S-PQFP-G100)

PLASTIC QUAD FLATPACK (DIE DOWN)



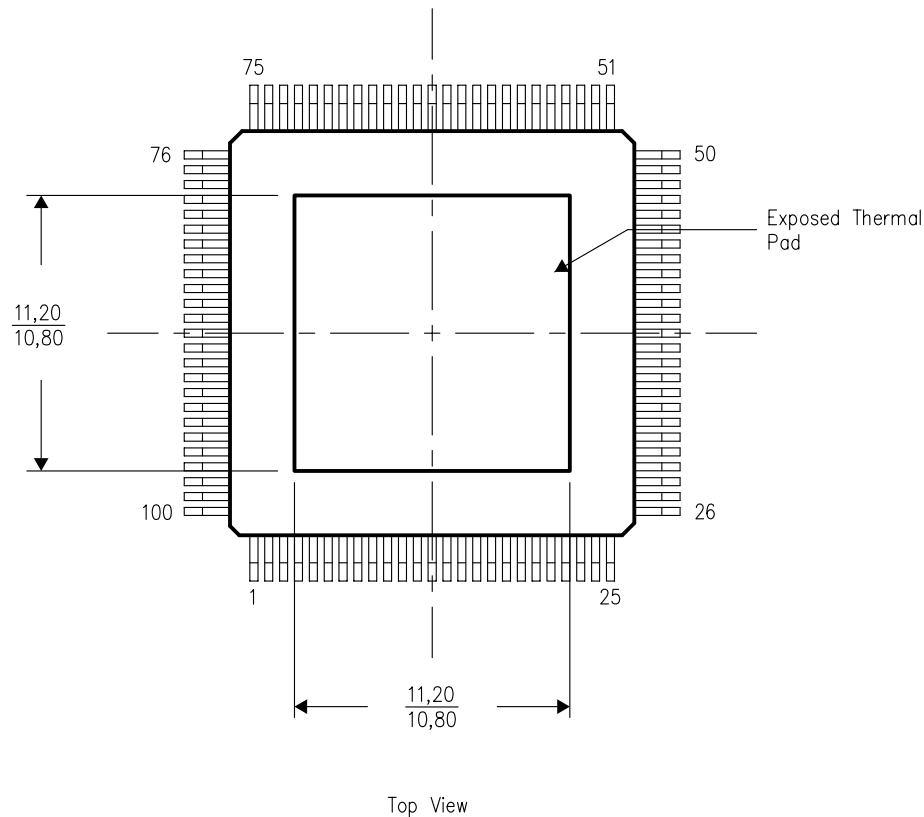
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Thermally enhanced molded plastic package with a heat slug (HSL)
 D. Falls within JEDEC MS-026

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com