#### SN74F323 8-BIT UNIVERSAL SHIFT-STORAGE REGISTER WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

SDFS072A - D2932, MARCH 1987 - REVISED OCTOBER 1993

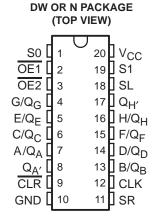
• Four Modes of Operation:

Hold (Store)
Shift Right
Shift Left
Load Data

- Operates With Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Synchronous Clear
- Applications:

Stacked or Push-Down Registers Buffer Storage Accumulator Registers

 Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs



#### description

This 8-bit universal register features multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S0, S1) and two output-enable (OE1, OE2) inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both S0 and S1 high. This places the 3-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs synchronously when the clear (CLR) input is low. Taking either OE1 or OE2 high disables the outputs but this has no effect on clearing, shifting, or storage of data.

The SN74F323 is characterized for operation from 0°C to 70°C.

#### **FUNCTION TABLE**

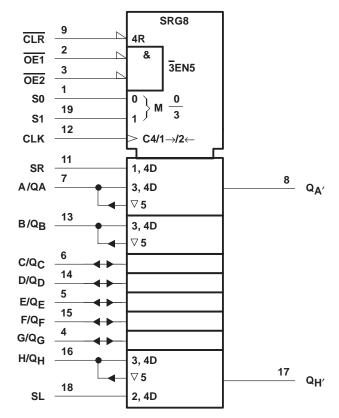
MODE		INPUTS						I/O PORTS						OUTI	PUTS			
MODE	CLR	S1	S0	OE1 <sup>†</sup>	OE2†	CLK	SL	SR	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/QC	D/QD	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	$Q_{\mathbf{A}'}$	$Q_{H'}$
	L	Х	L	L	L	1	Х	Χ	L	L	L	L	L	L	L	L	L	L
Clear	L	L	Χ	L	L	<b>↑</b>	Х	Χ	L	L	L	L	L	L	L	L	L	L
	L	Н	Н	Х	Χ	<b>↑</b>	Χ	X	Х	Χ	Χ	Χ	Χ	Χ	Χ	Χ	L	L
11-1-1	Н	L	L	L	L	Х	Χ	Х	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
Hold	Н	Х	Χ	L	L	L	Χ	Χ	Q <sub>A0</sub>	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$	$Q_{E0}$	Q <sub>F0</sub>	$Q_{G0}$	$Q_{H0}$	Q <sub>A0</sub>	$Q_{H0}$
Shift	Н	L	Н	L	L	1	Χ	Н	Н	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Н	Q <sub>Gn</sub>
Right	Н	L	Н	L	L	<b>↑</b>	Χ	L	L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$Q_{Dn}$	$Q_{En}$	$Q_{Fn}$	$Q_{Gn}$	L	$Q_{Gn}$
Shift	Н	Н	L	L	L	1	Н	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	QGn	Q <sub>Hn</sub>	Н	Q <sub>Bn</sub>	Н
Left	Н	Н	L	L	L	<b>↑</b>	L	Χ	Q <sub>Bn</sub>	$Q_{Cn}$	$Q_{Dn}$	$Q_{En}$	$Q_{Fn}$	$Q_{Gn}$	$Q_{Hn}$	L	Q <sub>Bn</sub>	L
Load	Н	Н	Н	Х	Χ	1	Х	Χ	а	b	С	d	е	f	g	h	а	h

NOTE: a...h = the level of the steady-state input at inputs A through H, respectively. These data inputs are loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.



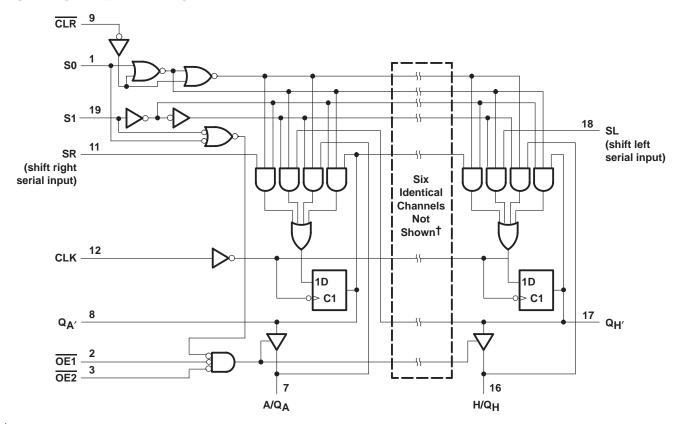
#### logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SDFS072A - D2932, MARCH 1987 - REVISED OCTOBER 1993

#### logic diagram (positive logic)



† I/O ports not shown: B/QB (13), C/QC (6), D/QD (14), E/QE (5), F/QF (15), and G/QG (4).

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Input current range	-30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state	-0.5  V to $5.5  V$
Voltage range applied to any output in the high state	$-0.5$ V to $V_{CC}$
Current into any output in the low state: Q <sub>A'</sub> or Q <sub>H'</sub>	40 mA
QA thru QH	48 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## SN74F323 8-BIT UNIVERSAL SHIFT-STORAGE REGISTER WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

SDFS072A - D2932, MARCH 1987 - REVISED OCTOBER 1993

#### recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	V
$V_{IH}$	High-level input voltage		2			V
$V_{IL}$	Low-level input voltage				0.8	V
ΙΙΚ	Input clamp current			-18	mA	
	Q <sub>A</sub> ' or Q <sub>H</sub> '				- 1	A
ІОН	High-level output current Q <sub>A</sub> thru Q <sub>H</sub>				-3	mA
loL	Law law law taut award	$Q_{A'}$ or $Q_{H'}$			20	4
	Low-level output current Q <sub>A</sub> thru Q <sub>H</sub>				24	mA
TA	Operating free-air temperature		0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		1	TEST CONDITIONS				
٧ıK		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = –18 mA			-1.2	V
	Q <sub>A</sub> ' or Q <sub>H</sub> '		I <sub>OH</sub> = – 1 mA	2.5	3.4		
l.,	O them O	V <sub>CC</sub> = 4.5 V	$I_{OH} = -1 \text{ mA}$	2.5	3.4		.,
VOH	Q <sub>A</sub> thru Q <sub>H</sub>		$I_{OH} = -3 \text{ mA}$	2.4	3.3		V
	Any output	$V_{CC} = 4.75 V$ ,	$I_{OH} = -1 \text{ mA to } -3 \text{ mA}$	2.7			
.,	Q <sub>A</sub> ' or Q <sub>H</sub> '	V 45V	I <sub>OL</sub> = 20 mA		0.3	0.5	V
VOL	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = 4.5 V	$I_{OL} = 24 \text{ mA}$		0.35	0.5	V
	A thru H	V 55V	V <sub>I</sub> = 5.5 V			1	4
I <sub>I</sub>	Any other	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 7 V			0.1	mA
. +	A thru H	V 55V	V 07V			70	٨
I <sub>IH</sub> ‡	Any other	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20	μΑ
	A thru H					-0.65	
IIL‡	S0 or S1	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V			-1.2	mA
	Any other					-0.6	
los§		V <sub>CC</sub> = 5.5 V,	VO = 0	-60		-150	mA
Icc		$V_{CC} = 5.5 \text{ V},$	See Note 2		68	95	mA

NOTE 2: I<sub>CC</sub> is measured with OE1, OE2, and CLK at 4.5 V.

<sup>†</sup> All typical values are at  $V_{CC}$  = 5 V,  $T_A$  = 25°C. ‡ For I/O ports ( $Q_A$  thru  $Q_H$ ), the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

<sup>§</sup> Not more than one output shou<u>ld be shorted at a time, and the duration of the short circuit should not exceed one second.</u>

# 8-BIT UNIVERSAL SHIFT-STORAGE REGISTER WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

SDFS072A - D2932, MARCH 1987 - REVISED OCTOBER 1993

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V <sub>CC</sub> =		MIN	MAX	UNIT	
				MIN	MAX				
fclock	Clock frequency			0	70	0	70	MHz	
t <sub>W</sub>	Pulse duration	CLK high or low		7		7		ns	
		S0 or S1	High or low	8.5		8.5			
t <sub>su</sub> Set	Setup time before CLK↑	A/Q <sub>A</sub> thru H/Q <sub>H</sub> , SR, or SL	High or low	5		5		ns	
		CLR	High or low	10		10			
		S0 or S1	High or low	0		0			
th	Hold time after CLK↑	A/Q <sub>A</sub> thru H/Q <sub>H</sub> , SR, or SL	High or low	2		2	·	ns	
		CLR	High or low	0		0			

#### switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$ = 5 V, $C_{L}$ = 50 pF, $R_{L}$ = 500 Ω, $T_{A}$ = 25°C			$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ $T_A = \text{MIN t}$	UNIT		
			MIN	TYP	MAX	MIN	MAX		
f <sub>max</sub>			70	100		70		MHz	
t <sub>PLH</sub>	OLIV	0	3.2	6.6	9	3.2	10	ns	
<sup>t</sup> PHL	CLK	$Q_{A'}$ or $Q_{H'}$	2.7	6.1	8.5	2.7	9.5		
t <sub>PLH</sub>	OL IX	O . them. O .	3.2	6.6	9	3.2	10		
t <sub>PHL</sub>	CLK	Q <sub>A</sub> thru Q <sub>H</sub>	4.2	8.1	11	4.2	12	ns	
<sup>t</sup> PZH	OE1 or OE2	O . Abania O .	2.7	5.6	8	2.7	9	ns	
t <sub>PZL</sub>	OET OF OEZ	Q <sub>A</sub> thru Q <sub>H</sub>	3.2	6.6	10	3.2	11		
<sup>t</sup> PHZ	OE1 or OE2	O thru O	1.7	4.1	6	1.7	7		
<sup>t</sup> PLZ	OET OF OE2	Q <sub>A</sub> thru Q <sub>H</sub>	1.2	3.6	5.5	1.2	6.5	ns	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 3: Load circuits and waveforms are shown in Section 1.





#### PACKAGE OPTION ADDENDUM

18-Sep-2008

#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74F323DW	OBSOLETE	SOIC	DW	20	TBD	Call TI	Call TI
SN74F323DWR	OBSOLETE	SOIC	DW	20	TBD	Call TI	Call TI
SN74F323N	OBSOLETE	PDIP	N	20	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <a href="http://www.ti.com/productcontent">http://www.ti.com/productcontent</a> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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