- **Supports SSTL_18 Signaling Levels**
- **Suitable for DDR-II Applications**
- **D−Port Outputs Are Precharged by Bias Voltage (V_{BIAS})**
- **Internal Termination for Control Inputs**
- **High Bandwidth (334 MHz Min)**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics, (r_{on} = 17 Ω Max)**
- **Internal 400-Ω Pulldown Resistors**
- **Low Differential and Rising/Falling Edge Skew**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

description/ordering information

The SN74CBTU4411 is a high-bandwidth, SSTL_18 compatible FET multiplexer/demultiplexer with low ON-state resistance (r_{on}). The device utilizes an internal charge pump to elevate the gate voltage of the pass transistor, providing a low and flat r_{on}. The low and flat r_{on} allows for minimal propagation delay and supports rail-to-rail signaling on data input/output (I/O) ports. The device also features very low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Matched r_{on} and I/O capacitance among channels results in extremely low differential and rising/falling edge skew. This allows the device to show optimal performance in DDR-II applications.

The device is organized as an 11-bit 1-of-4 multiplexer/demultiplexer with a single switch-enable ($\overline{EN}$) input. When $\overline{EN}$ is low, the switch is enabled and the H port is connected to one of the D ports. Ports D0 to D9 for the disabled channels are connected to V_{BIAS} through a 400 Ω resistor. DQS_EN determines the output voltage for the disabled D10 ports. When DQS_EN is low, this voltage is V_{BIAS}. When DQS_EN is high, the disabled D10 ports are connected to an internal voltage (V_{BIAS_DQS}) source, which is approximately equal to 0.7 V_{DD}.

When $\overline{EN}$ is high, all the channels are disabled. Ports D0 to D9 are connected to V_{BIAS}. For the D10 port, the disabled output voltage is determined by the DQS_EN input. When DQS_EN is low, this voltage is V_{BIAS}. When DQS_EN is high, this voltage is V_{DD}.

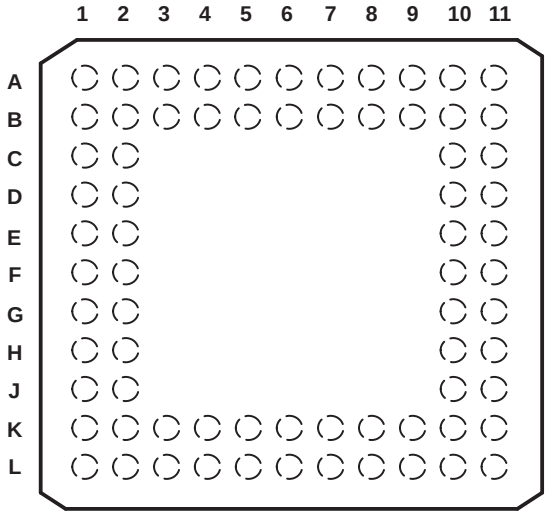
The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. The $\overline{EN}$ and TC inputs determine the internal termination for S0 and S1 inputs. When $\overline{EN}$ is low, the termination is determined by the TC input. When both $\overline{EN}$ and TC are low, termination resistors are disconnected from the S inputs. When $\overline{EN}$ is low and TC is high, both pullup and pulldown resistors are connected to the S inputs. When $\overline{EN}$ is high, only the pulldown termination resistors are connected to the S inputs, regardless of the voltage level at the TC input.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 85°C	LFBGA − GST	Tape and reel	SN74CBTU4411GSTR	CTU4411

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

GST PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6	7	8	9	10	11
A	S1	DQS_EN	V_{DD}	0D0	1D0	2D0	1D1	2D1	3D1	0D2	1D2
B	TC	S0	V_{DD}	GND	H0	3D0	0D1	H1	GND	H2	2D2
C	V_{REF}	$\overline{EN}$								0D3	3D2
D	V_{BIAS}	GND								H3	1D3
E	2D10	3D10								2D3	3D3
F	1D10	H10								GND	0D4
G	0D10	GND								H4	1D4
H	3D9	2D9								2D4	3D4
J	1D9	H9								1D5	0D5
K	0D9	GND	H8	0D8	H7	0D7	GND	H6	0D6	H5	2D5
L	3D8	2D8	1D8	3D7	2D7	1D7	3D6	2D6	1D6	V_{DD}	3D5

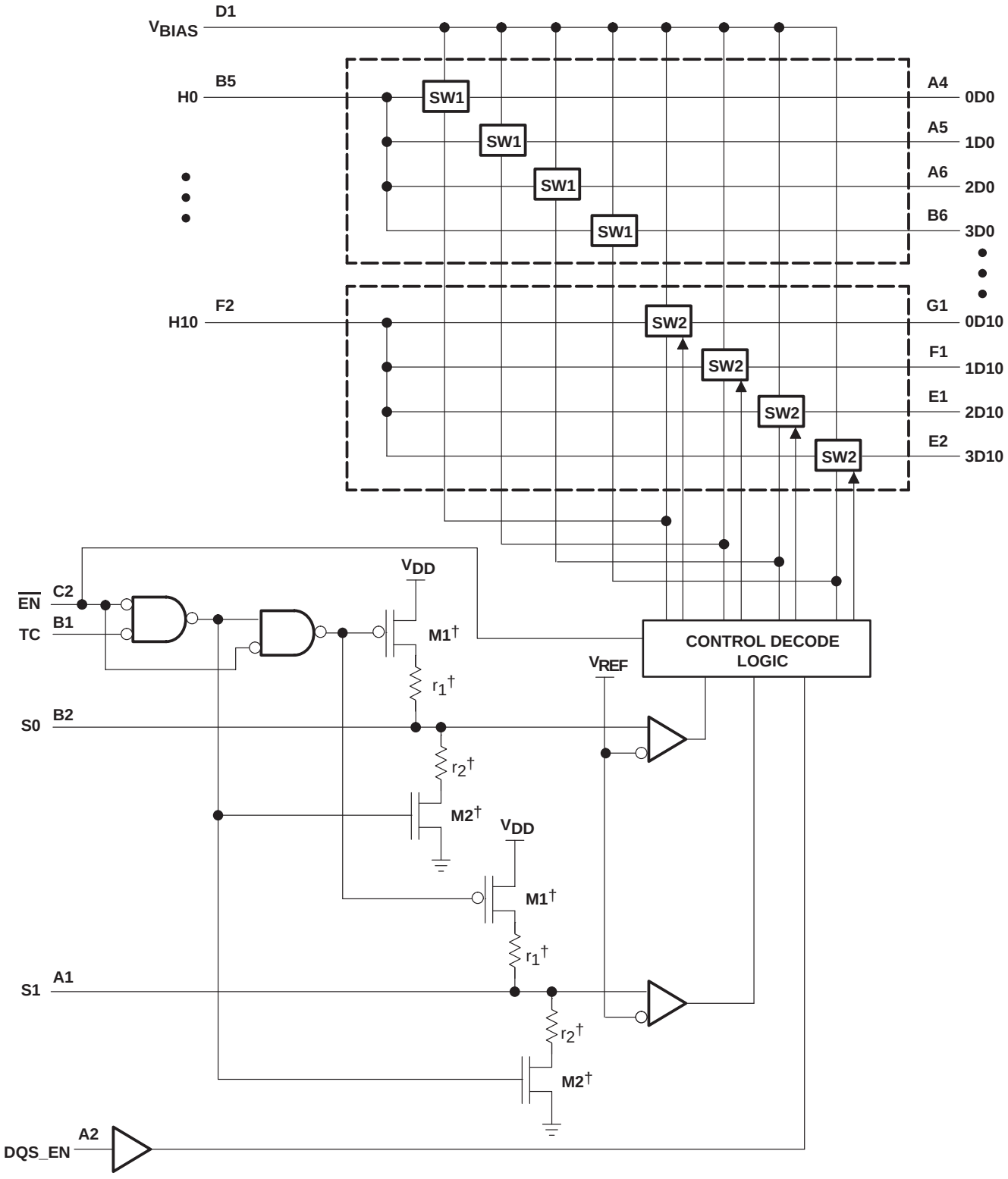
FUNCTION TABLES

INPUTS				INPUT/OUTPUT	FUNCTION
$\overline{EN}$	DQS_EN	S1	S0	Hn	
L	L	L	L	0Dn	Hn = 0Dn 1Dn, 2Dn, 3Dn connected to V_{BIAS}
L	L	L	H	1Dn	Hn = 1Dn 0Dn, 2Dn, 3Dn connected to V_{BIAS}
L	L	H	L	2Dn	Hn = 2Dn 0Dn, 1Dn, 3Dn connected to V_{BIAS}
L	L	H	H	3Dn	Hn = 3Dn 0Dn, 1Dn, 2Dn connected to V_{BIAS}
L	H	L	L	0Dn	H0−H9 = 0D0−0D9 1D0−1D9, 2D0−2D9, 3D0−3D9 connected to V_{BIAS} H10 = 0D10 1D10, 2D10, 3D10 connected to V_{BIAS_DQS}†
L	H	L	H	1Dn	H0−H9 = 1D0−1D9 0D0−0D9, 2D0−2D9, 3D0−3D9 connected to V_{BIAS} H10 = 1D10 0D10, 2D10, 3D10 connected to V_{BIAS_DQS}†
L	H	H	L	2Dn	H0−H9 = 2D0−2D9 0D0−0D9, 1D0−1D9, 3D0−3D9 connected to V_{BIAS} H10 = 2D10 0D10, 1D10, 3D10 connected to V_{BIAS_DQS}†
L	H	H	H	3Dn	H0−H9 = 3D0−3D9 0D0−0D9, 1D0−1D9, 2D0−2D9 connected to V_{BIAS} H10 = 3D10 0D10, 1D10, 2D10 connected to V_{BIAS_DQS}†
H	L	X	X	Z	0Dn, 1Dn, 2Dn, 3Dn connected to V_{BIAS}
H	H	X	X	Z	0D0−0D9, 1D0−1D9, 2D0−2D9, 3D0−3D9 connected to V_{BIAS} 0D10, 1D10, 2D10, 3D10 connected to V_{DD}

† V_{BIAS_DQS} is an internal voltage condition.

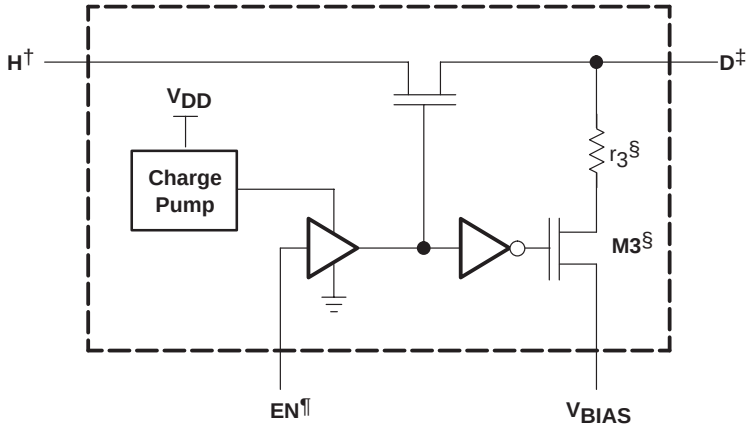
INPUTS		FUNCTION
$\overline{EN}$	TC	
L	L	Termination resistors disconnected from S inputs
L	H	Termination resistors connected with S inputs
H	X	Pulldown termination resistor connected and pullup termination resistor disconnected from the S inputs

logic diagram (positive logic)



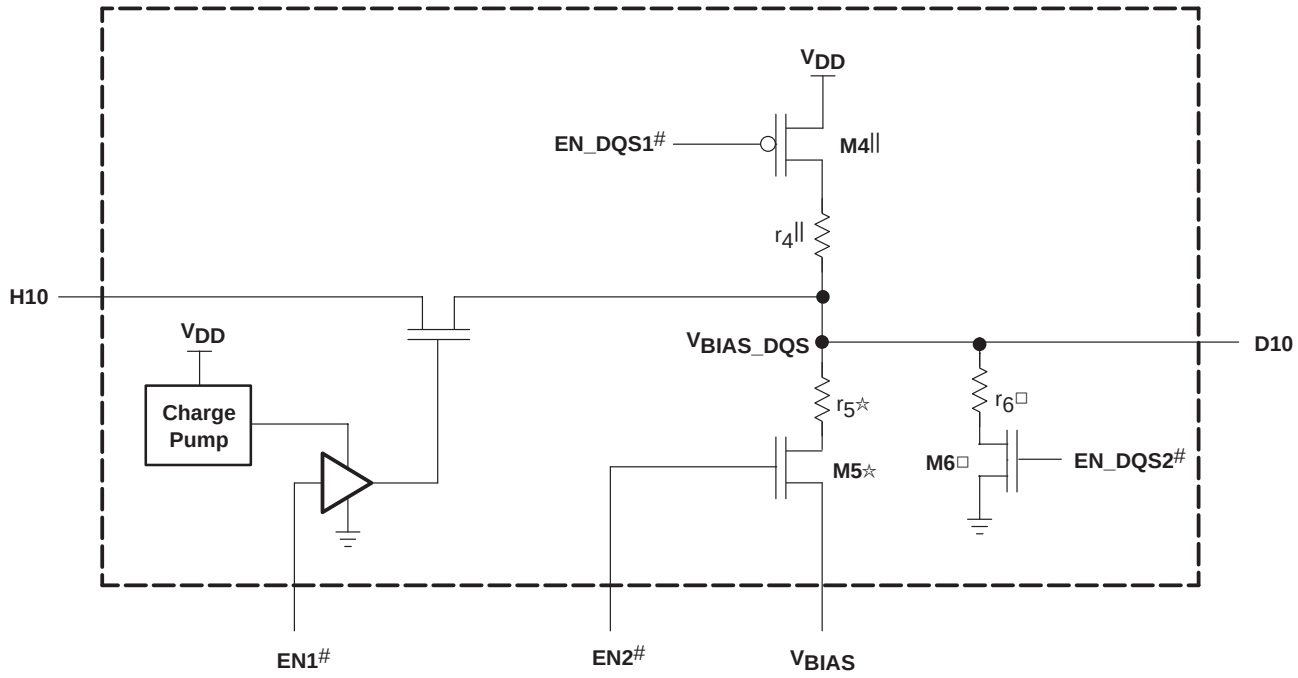
† $r_1 + r_{on}$ (M1), $r_2 + r_{on}$ (M2) = 160 Ω Typical.

simplified schematic, each FET switch (SW1)



† Applicable for ports H0 through H9
‡ Applicable for ports D0 through D9
§ $r_3 + r_{on}$ (M3) = 400 Ω Typical.
¶ EN is the internal enable signal applied to the switch.

simplified schematic, each FET switch (SW2)



EN_DQS1, EN_DQS2, EN1, and EN2 are the internal enable signals applied to the switch.
|| $r_4 + r_{on}$ (M4) = 1 kΩ Typical.
☆ $r_5 + r_{on}$ (M5) = 400 Ω Typical.
□ $r_6 + r_{on}$ (M6) = 2.3 kΩ Typical.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . −0.5 V to 2.5 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . . −0.5 V to 2.5 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . . −0.5 V to 2.5 V
Control input clamp current, I_{IK} ($V_{IN} < 0$ or $V_{IN} > 0$) . . . . . ±50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$ or $V_{I/O} > 0$) . . . . . ±50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . . ±100 mA
Continuous current through V_{DD} or GND terminals . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5) . . . . . TBD°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground, unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	1.7	1.8	1.9	V
V_{REF}	Reference supply voltage	0.49 V_{DD}	0.5 V_{DD}	0.51 V_{DD}	V
V_{BIAS}	BIAS supply voltage	0	0.3 V_{DD}	0.33 V_{DD}	V
V_{IH}	High-level control input voltage (S)	V_{REF} +250 mV			V
	High-level control input voltage ($\overline{EN}$, TC, DQS_EN)	0.65 V_{DD}			
V_{IL}	Low-level control input voltage (S)			V_{REF} −250 mV	V
	Low-level control input voltage ($\overline{EN}$, TC, DQS_EN)			0.35 V_{DD}	
$V_{I/O}$	Data input/output voltage	0		V_{DD}	V
T_A	Operating free-air temperature	0		85	°C

NOTE 6: All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A = 70 °C	T_A = 0 °C TO 85 °C			UNIT
					MIN MAX	MIN	TYP†	MAX	
V_{IK}‡	Control inputs§	V_{DD} = 1.7 V,	I_{IN} = −18 mA					−1.8	V
$V_{BIAS\ DQS}$	D10	V_{DD} = 1.7 V,	DQS_EN = V_{DD}			1.1		1.275	V
V_{OH}	D10	V_{DD} = 1.7 V, DQS_EN = V_{DD},	$\overline{EN}$ = V_{DD},	I_O = 100 µA			1.6	1.8	V
I_{IN}	Control inputs§	V_{DD} = 1.9 V,	V_{IN} = V_{DD} or GND					±1	µA
I_{OZ}¶		V_{DD} = 1.9 V,	V_O = 0 to 1.9 V, V_I = 0,	Switch OFF, V_{BIAS} open				±10	µA
I_{CC}		V_{DD} = 1.9 V, TC = GND, $\overline{EN}$ = GND,	$I_{I/O}$ = 0, S0, S1 = V_{IH} or V_{IL},	Switch ON or OFF			0.7	2.5	mA
		$\overline{EN}$ = V_{DD}						500	µA
I_{CCD}		V_{DD} = 1.9 V, TC = GND, $\overline{EN}$ = GND,	$I_{I/O}$ = 0, S0 or S1 input switching at 50% duty cycle, Data I/O are open					0.5	mA/MHz#
C_{in}	S port	V_{DD} = 1.9 V, TC = GND,	$\overline{EN}$ = GND, V_{IN} = V_{REF} ± 250 mV			2.5		3.5	pF
	$\overline{EN}$, TC, DQS_EN inputs	V_{DD} = 1.9 V,	V_{IN} = 0 or 1.9 V				2.5		pF
$C_{io(OFF)}$	H port	$V_{I/O}$ = 0.5 V_{DD} ± 0.4 V	Switch OFF,	V_{BIAS} open				2.5	pF
$C_{io(ON)}$		$V_{I/O}$ = 0.5 V_{DD} ± 0.4 V,	Switch ON,	V_{BIAS} = GND				4.6	pF
r_{on}‖		V_{DD} = 1.7 V, V_I = 0.5 V_{DD} ± 0.5 V,		I_O = 10 mA		6	10	17	Ω
Δr_{on} (flat)☆		V_{DD} = 1.7 V, DQS_EN = V_{DD}, I_O = 10 mA	V_I = 0.5 V_{DD} ± 0.25 V				1.5	3	Ω
			V_I = 0.5 V_{DD} ± 0.5 V				2.5	5	Ω
r_{term}	S port	V_{DD} = 1.7 V				110	160	210	Ω
$r_{pulldown}$	D0−D10	V_{DD} = 1.7 V	DQS_EN = GND			280	400	520	Ω
	D10		DQS_EN = V_{DD}, $\overline{EN}$ = GND			1600	2300	3000	
r_{pullup}	D10	V_{DD} = 1.7 V,	DQS_EN = V_{DD}, $\overline{EN}$ = GND			700	1000	1300	Ω

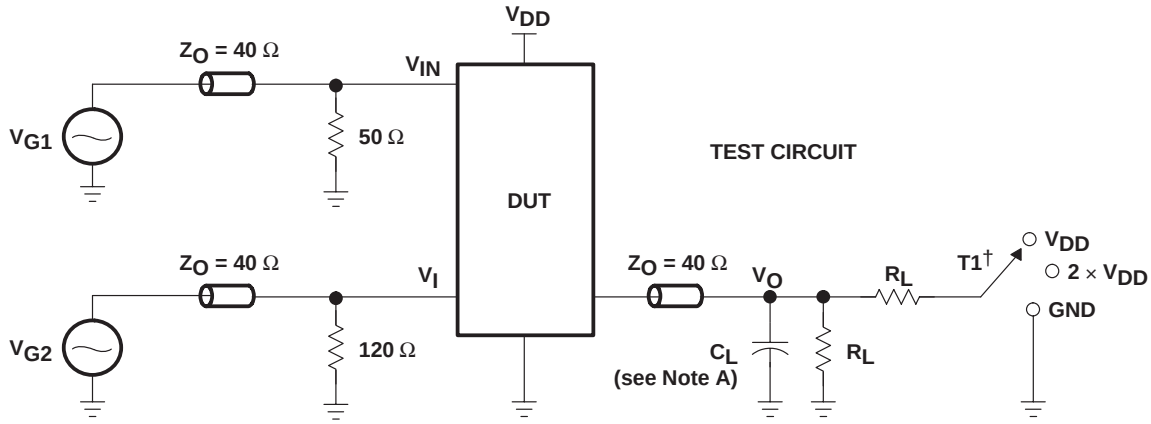
V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
† All typical values are at V_{DD} = 1.8 V (unless otherwise noted), T_A = 25°C.
‡ V_{IK} refers to the clamp voltage due to the internal diode, which is connected from each control input to GND.
§ For the leakage current test on S0 and S1, $\overline{EN}$ and TC inputs are set to low.
¶ For I/O ports, the parameter I_{OZ} includes the input leakage current. I_{OZ} applies only to the H port.
# The frequency of S0 and S1 inputs, for example, for a data I/O rate of 533 Mbit/s, with a burst of 4, the required frequency is for S0 or S1 input is ≅ 66 MHz (533/8). The total I_{CC} due to switching S0, S1 will be approximately 27 mA (66 MHz × 0.4 mA/MHz).
‖ Measured by the voltage drop between the D and H terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (D or H) terminals.
☆ Δr_{on}(flat) is the difference of maximum r_{on} and minimum r_{on} for a specific channel in a specific device.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

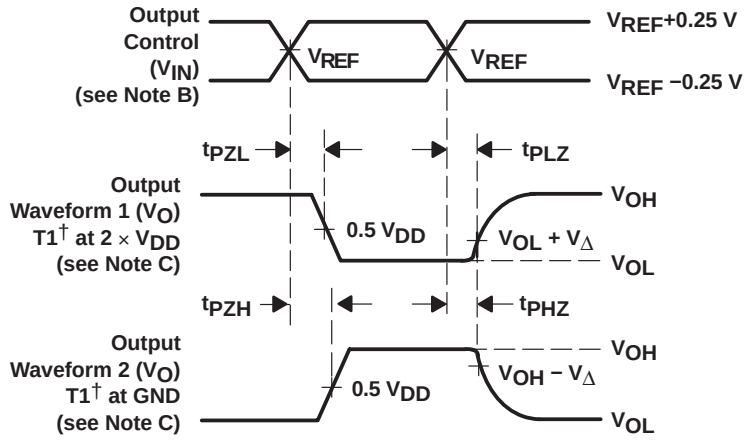
PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 70 °C		T_A = 0 °C TO 85 °C			UNIT
				MIN	MAX	MIN	TYP	MAX	
f_{max}	D or H port					334			MHz
	S port†					84			
t_{pd}		H or D	D or H				297		ps
t_{en} (t_{PZL}, t_{PZH})‡		S	D			750		2100	ps
t_{dis} (t_{PLZ}, t_{PHZ})‡		S	D			750		2100	ps
t_{osk}								85	ps
t_{esk}								40	ps
t_{start}§							20		µs

† $\overline{EN}$ = GND, TC = GND
‡ V_{BIAS} = open
§ t_{start} is the time required for the charge-pump circuit output voltage to reach a steady state value after V_{DD} is applied.

PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	V_{DD}	T1†	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	1.8 V ± 0.1 V	2 × V_{DD}	1 kΩ	GND	6 pF	0.125 V
t_{PHZ}/t_{PZH}	1.8 V ± 0.1 V	GND	1 kΩ	V_{DD}	6 pF	0.125 V



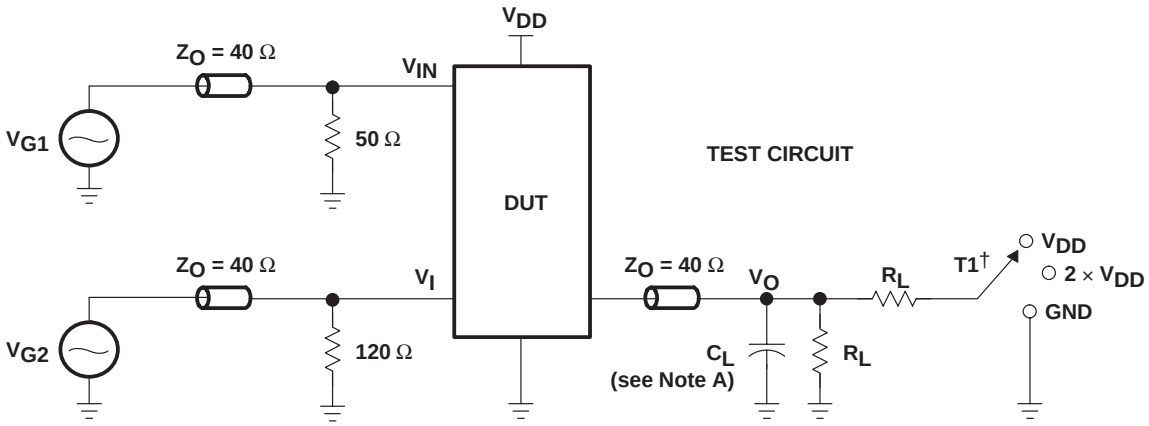
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

† T1 is an external terminal.

NOTES: A. C_L includes probe and jig capacitance.
B. Output control applies to select (S0, S1) inputs.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. All input pulses are supplied by generators having the following characteristics: Z_{OS} = 50 Ω,rising and falling edge rate is 1 V/ns.
E. The outputs are measured one at a time, with one transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.

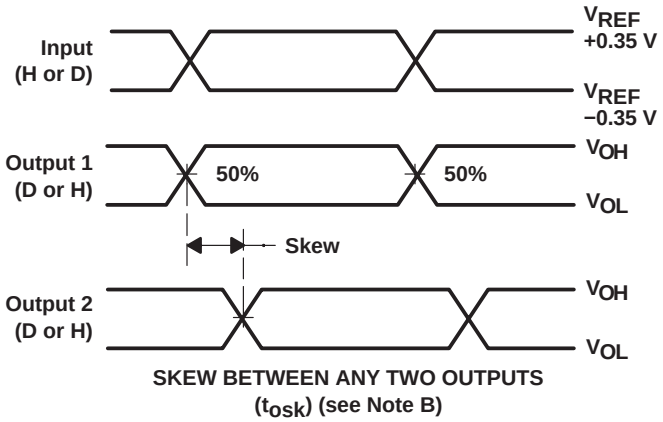
Figure 1. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
(Skew and Propagation Delay Times)

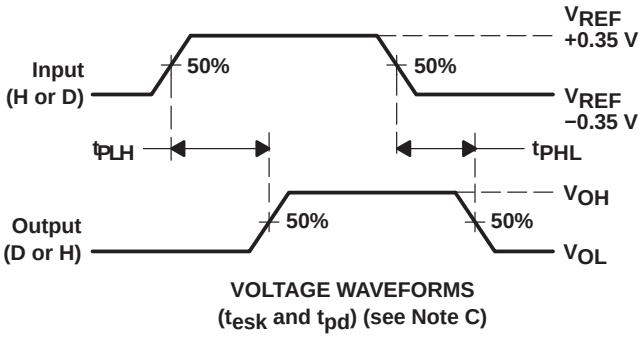


TEST	V_{DD}	T1†	R_L	V_I	C_L
t_{pd}	1.8 V ± 0.1 V	V_{DD}	150 Ω	see Waveform	6 pF
t_{osk}	1.8 V ± 0.1 V	V_{DD}	150 Ω	see Waveform	6 pF
t_{esk}	1.8 V ± 0.1 V	V_{DD}	150 Ω	see Waveform	6 pF

† T1 is an external terminal.



SKEW BETWEEN ANY TWO OUTPUTS
(t_{osk}) (see Note B)

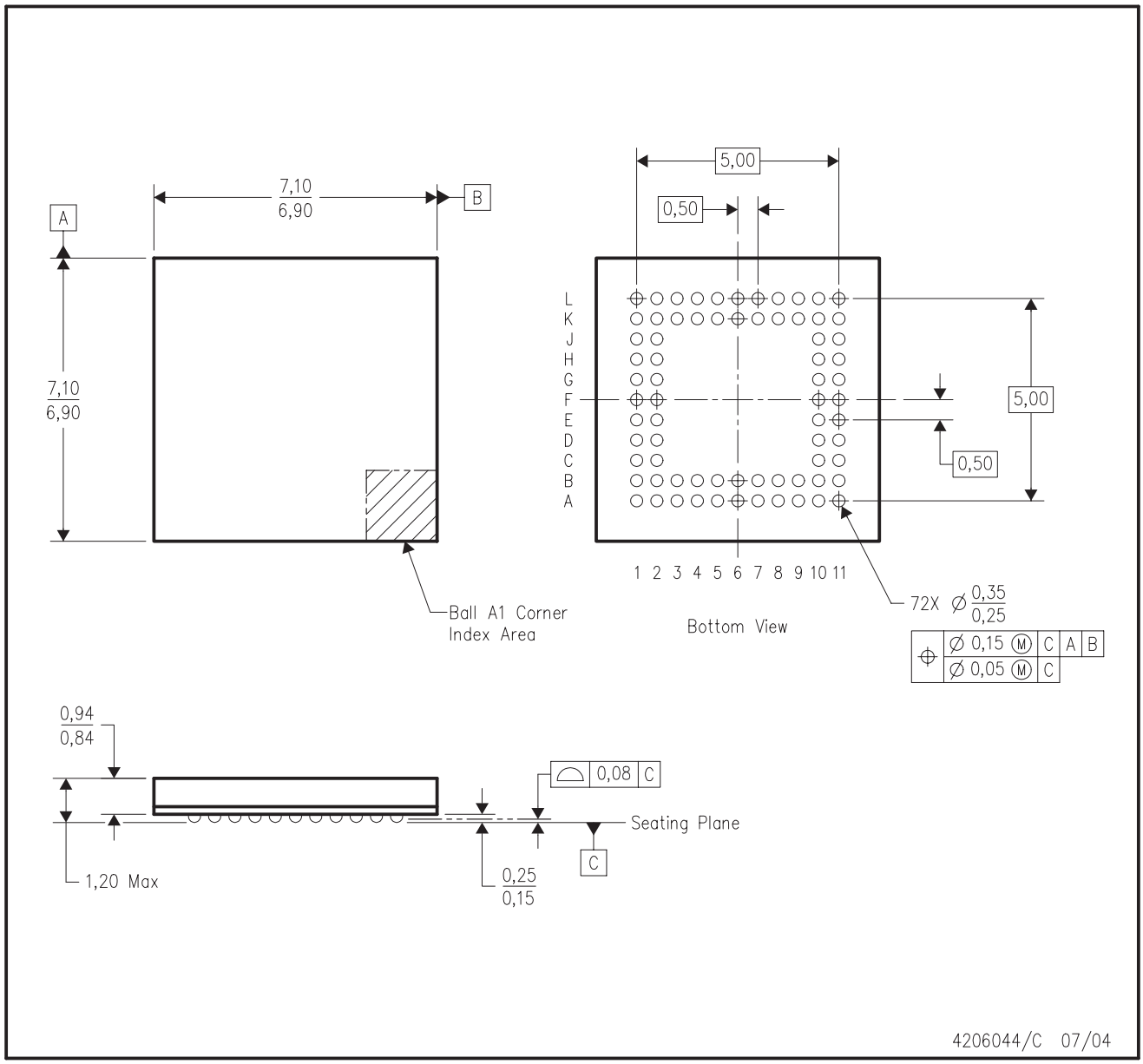


VOLTAGE WAVEFORMS
(t_{esk} and t_{pd}) (see Note C)

NOTES: A. C_L includes probe and jig capacitance.
B. t_{osk} is the difference in output voltage from channel to channel in a specific device.
C. t_{PLH} and t_{PHL} are the same as t_{pd} and $t_{esk} = |t_{PLH} - t_{PHL}|$
D. All input pulses are supplied by generators having the following characteristics: Z_{OS} = 50 Ω,rising and falling edge rate is 1 V/ns.
E. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Test Circuit and Voltage Waveforms

ZST (S–PBGA–N72) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC MO–225 registration is pending.
D. This package is lead–free. Refer to the 72 GST package (drawing 4206043) for tin–lead (SnPb).

PACKAGING INFORMATION

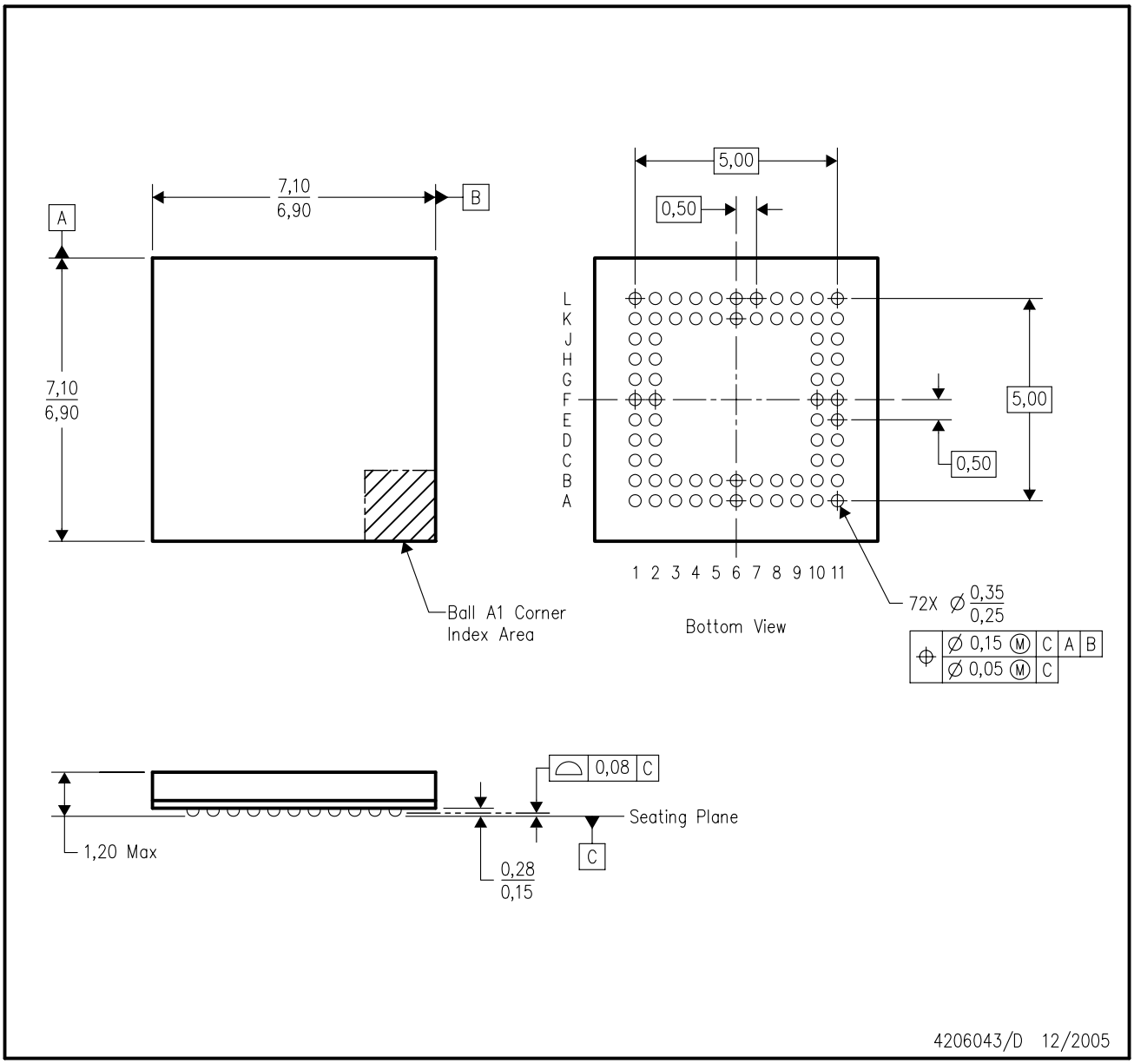
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74CBTU4411GSTR	PREVIEW	NFBGA	GST	72	2000	TBD	Call TI	Call TI
SN74CBTU4411ZSTR	ACTIVE	NFBGA	ZST	72	2000	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

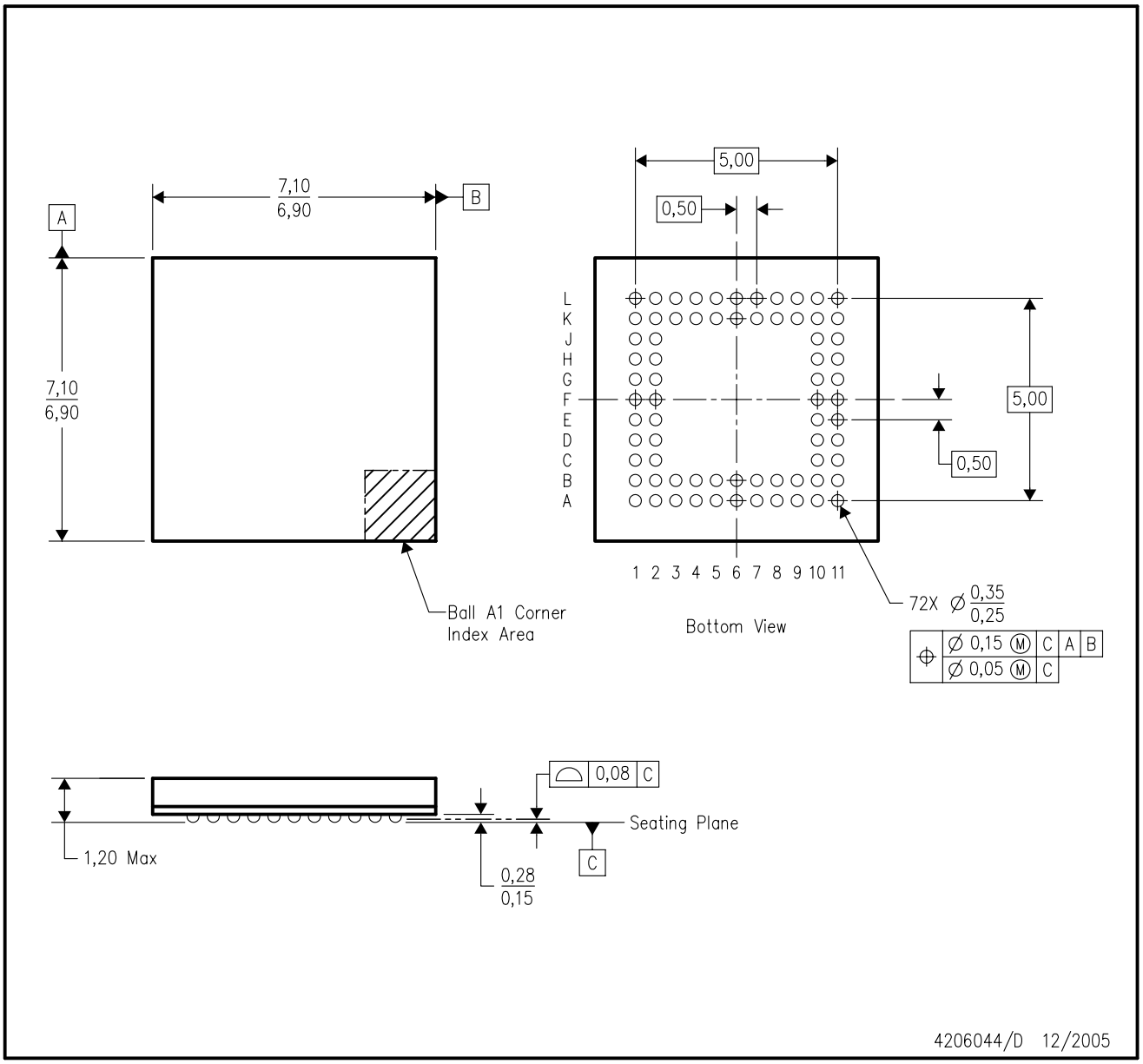
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

GST (S–PBGA–N72) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Complies to JEDEC MO–195 variation AD (depopulated).
D. This package is tin–lead (SnPb). Refer to the 72 ZST package (drawing 4206044) for lead–free.

ZST (S–PBGA–N72) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Complies to JEDEC MO–195 variation AD (depopulated).
D. This package is lead–free. Refer to the 72 GST package (drawing 4206043) for tin–lead (SnPb).

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