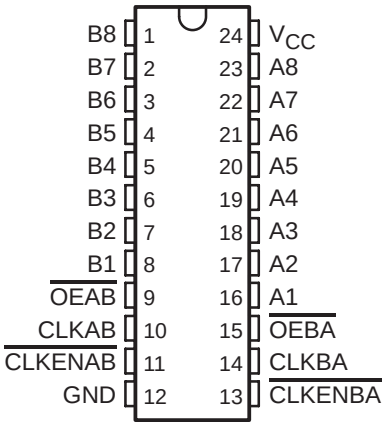
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Two 8-Bit, Back-to-Back Registers Store Data Flowing in Both Directions**
- **A Port Sinks 24 mA and Sources 3 mA**
- **B Port Sinks 64 mA and Sources 15 mA**
- **Noninverting Outputs**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN74BCT2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

The SN74BCT2952 is characterized for operation from 0°C to 70°C.

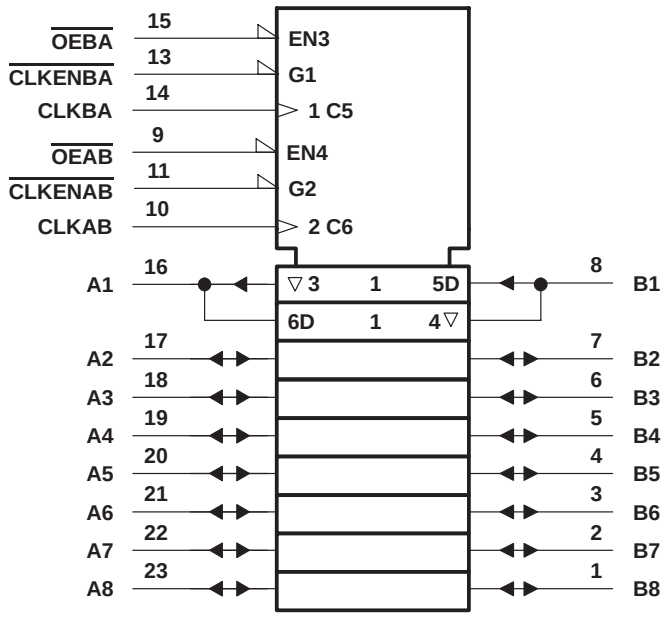
FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	B
H	X	L	X	B_0‡
X	H or L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.

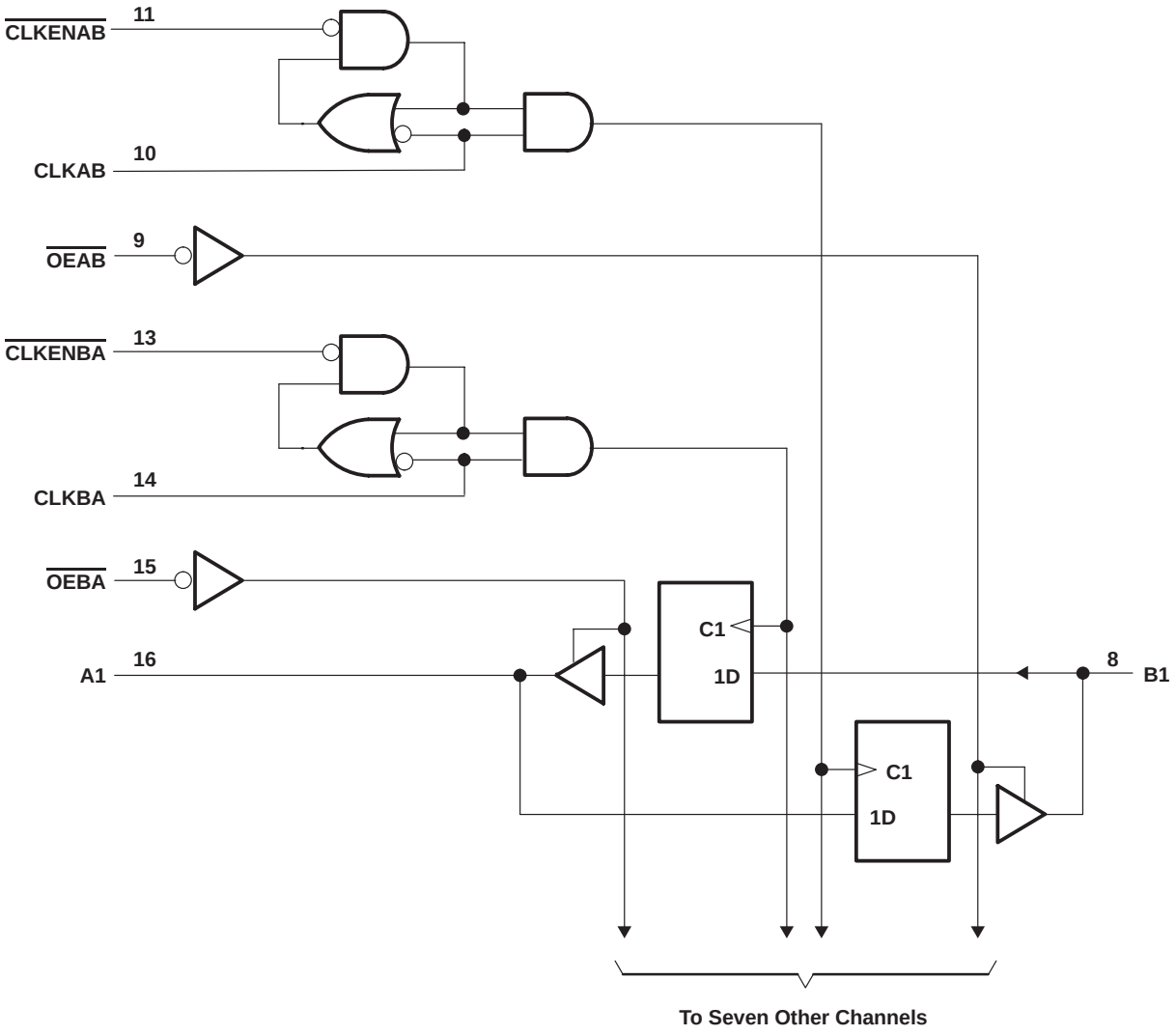
‡ Level of B before the indicated steady-state input conditions were established.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . −0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) . . . . . −30 mA
Current into any output in the low state . . . . . 128 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A ports			−3	mA
		B ports			−15	
I_{OL}	Low-level output current	A ports			24	mA
		B ports			64	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	A port	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		
	B port	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		
			I_{OH} = −15 mA	2	3.1		
		V_{CC} = 4.75 V,	I_{OH} = − 3 mA	2.7			
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 24 mA		0.35	0.5	V
	B port		I_{OL} = 64 mA		0.42	0.55	
I_I‡	Control inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			1	mA
	A or B ports					0.1	
I_{IH}‡	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			70	µA
	A or B ports					20	
I_{IL}‡	Control inputs	V_{CC} = 5.5 V,	V_I = 0.5 V			−70	µA
	A or B ports					−20	
I_{OS}§	Any A	V_{CC} = 5.5 V,	V_O = 0	−60		−150	mA
	Any B			−100		−250	
I_{CCH}¶		V_{CC} = 5.5 V			2	5	mA
I_{CCL}¶		V_{CC} = 5.5 V			38	55	mA
I_{CCZ}		V_{CC} = 5.5 V			2	5	mA
C_i	Control inputs	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6		pF
C_{io}	A or B ports	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		12.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-shoot output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ I_{CCH} and I_{CCL} are measured in the A-to-B mode.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency			125		125	MHz
t_w	Pulse duration, CLK high or low		4		4		ns
t_{su}	Setup time before CLK↑	A or B	2.5		2.5		ns
		$\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$	2		2		
t_h	Hold time after CLK↑	A or B	1.5		1.5		ns
		$\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$	2.5		2.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			125			125		MHz
t_{PLH}	CLKBA or CLKAB	A or B	3.5	5.7	7.5	3.5	9	ns
t_{PHL}			5	7	9.5	5	10.5	
t_{PZH}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	2.9	5.2	6.9	2.9	8.2	ns
t_{PZL}			5.2	7.6	11.4	5.2	12.9	
t_{PHZ}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	3.5	5.3	7.1	3.5	8.4	ns
t_{PLZ}			2.7	4.3	6	2.7	7	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74BCT2952DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74BCT2952DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74BCT2952NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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