MULTIPOINT-LVDS QUAD DIFFERENTIAL LINE DRIVER

FEATURES

- **Differential Line Drivers for 30-Ω to 55-Ω Loads and Data Rates(1) Up to 200 Mbps, Clock Frequencies up to 100 MHz**
- **Supports Multipoint Bus Architectures**
- **Operates from a Single 3.3-V Supply**
- **Characterized for Operation from –40°C to 85°C**
- **16-Pin SOIC (JEDEC MS-012) and 16-Pin TSSOP (JEDEC MS-153) Packaging**

APPLICATIONS

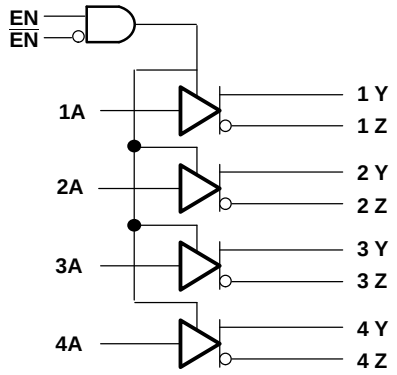
- **Clock Distribution**
- **Backplane or Cabled Multipoint Data Transmission in Telecommunications, Automotive, Industrial, and Other Computer Systems**
- **Cellular Base Stations**
- **Central-Office and PBX Switching**
- **Bridges and Routers**
- **Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485**(1)

(1) The data rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

DESCRIPTION

The SN65MLVD047 is a quadruple line driver. The output current of this device has been increased, in comparison to standard LVDS compliant devices, in order to support doubly terminated transmission lines and heavily loaded backplane bus applications. Backplane applications generally require impedance matching termination resistors at both ends of the bus. The effective impedance of a doubly terminated bus can be as low as 30 Ω due to the bus terminations, as well as the capacitive load of bus interface devices. SN65MLVD047 drivers allow for operation with loads as low as 30 Ω. The SN65MLVD047 devices allow for multiple drivers to be present on a single bus. Driver edge rate control is incorporated to support operation. The SN65MLVD047 provides 9-kV ESD protection on all bus pins.

LOGIC DIAGRAM (POSITIVE LOGIC)



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE/CARRIER
SN65MLVD047D	MLVD047	16-Pin SOIC/Tube
SN65MLVD047DR	MLVD047	16-Pin SOIC/Tape and Reel
SN65MLVD047PW	MLVD047	16-Pin TSSOP/Tube
SN65MLVD047PWR	MLVD047	16-Pin TSSOP/Tape and Reel

PACKAGE DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$ (1)	$T_A = 85°C$ POWER RATING
D(16)	Low-K (2)	898 mW	7.81 mW/°C	429 mW
PW(16)	Low-K (2)	592 mW	5.15 mW/°C	283 mw
	High-K (3)	945 mW	8.22 mW/°C	452 mw

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

				UNITS
V_{CC}	Supply voltage range (2)			–0.5 V to 4 V
V_I	Input voltage range	A, EN, $\overline{EN}$		–0.5 V to 4 V
V_O	Output voltage range	Y, Z		–1.8 V to 4 V
	Electrostatic discharge	Human Body Model (3)	Y and Z	±9 kV
			All pins	±4 kV
		Charged-Device Model (4)	All pins	±1500 V
		Machine Model (5)	All pins	200 V
T_J	Junction temperature			140°C
P_D	Continuous power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to the circuit ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

RECOMMENDED OPERATING CONDITIONS (see Figure 1)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
	Voltage at any bus terminal (separate or common mode) V_Y or V_Z	–1.4		3.8	V
R_L	Differential load resistance	30		55	Ω
$1/t_{UI}$	Signaling rate			200	Mbps
	Clock frequency			100	MHz
T_J	Junction temperature	–40		125	°C

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	Low-K board(1), no airflow	D		128		°C/W
		Low-K board(1), no airflow	PW		194.2		
		Low-K board(1), 150 LFM			146.8		
		Low-K board(1), 250 LFM			133.1		
		High-K board(2), no airflow			121.6		
θ_{JB}	Junction-to-board thermal resistance	High-K board(2)	D		51.1		°C/W
			PW		85.3		
θ_{JC}	Junction-to-case thermal resistance		D		45.4		°C/W
			PW		34.7		
P_D	Device power dissipation	EN = V_{CC}, $\overline{EN}$ = GND, R_L = 50 Ω, Input 100 MHz 50 % duty cycle square wave to 1A:4A, T_A = 85°C				288.5	mW

(1) In accordance with the Low-K thermal metric difinitions of EIA/JESD51-3.
(2) In accordance with the High-K thermal metric difinitions of EIA/JESD51-7.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
I_{CC}	Supply current	Driver enabled	EN = V_{CC}, $\overline{EN}$ = GND, R_L = 50 Ω, All inputs = V_{CC} or GND		59	70	mA
		Driver disabled	EN = GND, $\overline{EN}$ = V_{CC}, R_L = No load, All inputs = V_{CC} or GND		2	4	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) All typical values are at 25°C and with a 3.3-V supply voltage.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
LVTTL (EN, $\overline{EN}$, 1A:4A)						
$\|I_{IH}\|$	High-level input current	V_{IH} = 2 V or V_{CC}	0		10	µA
$\|I_{IL}\|$	Low-level input current	V_{IL} = GND or 0.8 V	0		10	µA
C_i	Input capacitance	V_I = 0.4 sin(30E6πt) + 0.5 V(3)		5		pF
M-LVDS (1Y/1Z:4Y/4Z)						
$\|V_{YZ}\|$	Differential output voltage magnitude	See Figure 2	480		650	mV
$\Delta\|V_{YZ}\|$	Change in differential output voltage magnitude between logic states		–50		50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	See Figure 3	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage				150	mV
$V_{Y(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 7	0		2.4	V
$V_{Z(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	See Figure 5			1.2 V_{SS}	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output		–0.2 V_{SS}			V
$\|I_{OS}\|$	Differential short-circuit output current magnitude	See Figure 4			24	mA
I_{OZ}	High-impedance state output current	–1.4 V ≤ (V_Y or V_Z) ≤ 3.8 V, Other output = 1.2 V	–15		10	µA
$I_{O(OFF)}$	Power-off output current	–1.4 V ≤ (V_Y or V_Z) ≤ 3.8 V, Other output = 1.2 V, V_{CC} = 0 V	–10		10	µA
C_Y or C_Z	Output capacitance	V_Y or V_Z = 0.4 sin(30E6πt) + 0.5 V,(3) Other input at 1.2 V, driver disabled		3		pF
C_{YZ}	Differential output capacitance	V_{YZ} = 0.4 sin(30E6πt) V,(3) Driver disabled			2.5	pF
$C_{Y/Z}$	Output capacitance balance, (C_Y/C_Z)		0.99	1.01		

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) All typical values are at 25°C and with a 3.3-V supply voltage.
(3) HP4194A impedance analyzer (or equivalent)

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 5	1	1.5	2.4	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	1.5	2.4	ns
t_r	Differential output signal rise time		1		1.9	ns
t_f	Differential output signal fall time		1		1.9	ns
$t_{sk(o)}$	Output skew				100	ps
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)			22	100	ps
$t_{sk(pp)}$	Part-to-part skew(2)				600	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(3)	All inputs 100 MHz clock input		0.2	1	ps
$t_{jit(c-c)}$	Cycle-to-cycle jitter(3)	All inputs 100 MHz clock input		5	36	ps
$t_{jit(pp)}$	Peak-to-peak jitter(3)(4)	All inputs 200 Mbps 2^{15}-1 PRBS input		46	158	ps
t_{PZH}	Enable time, high-impedance-to-high-level output	See Figure 6			7	ns
t_{PZL}	Enable time, high-impedance-to-low-level output				7	ns
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 6			8	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output				8	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) Stimulus jitter has been subtracted from the measurements.
(4) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).

PARAMETER MEASUREMENT INFORMATION

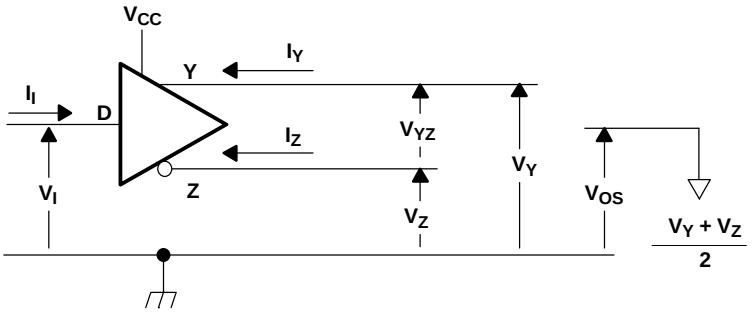
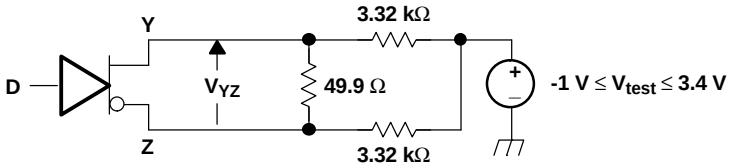
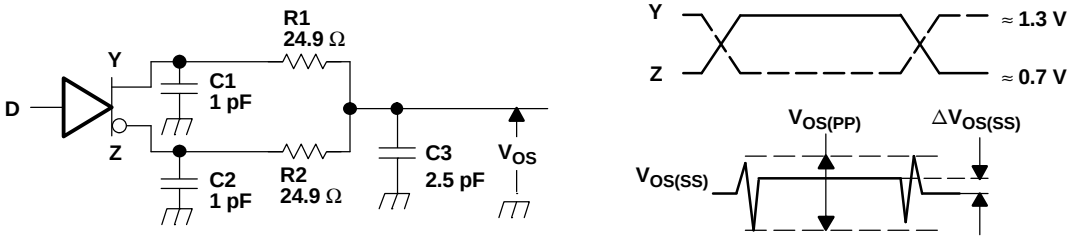


Figure 1. Driver Voltage and Current Definitions



NOTE: All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse frequency = 500 kHz, duty cycle = 50 ± 5%.

B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.

C. R1 and R2 are metal film, surface mount, ±1%, and located within 2 cm of the D.U.T.

D. The measurement of $V_{OS(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Common-Mode Output Voltage

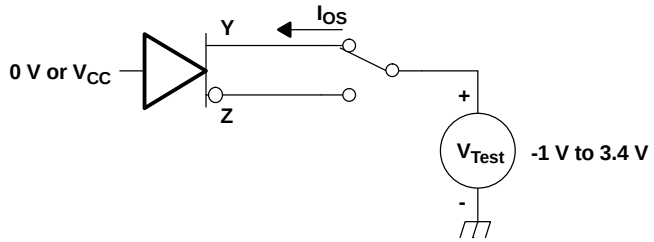
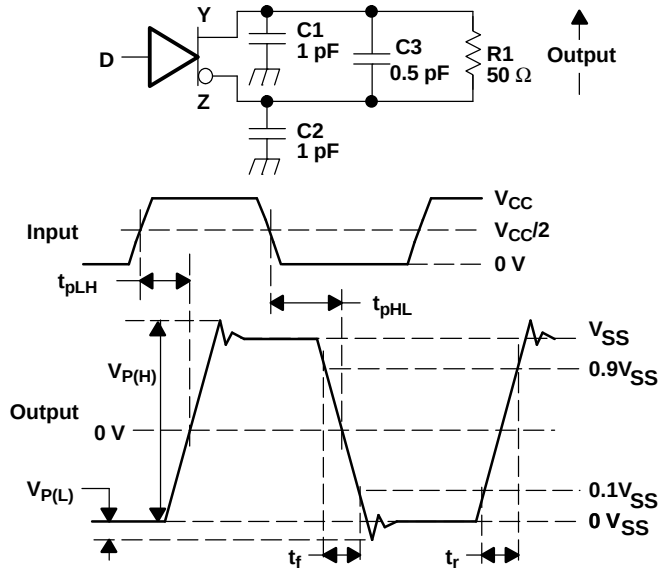


Figure 4. Short-Circuit Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



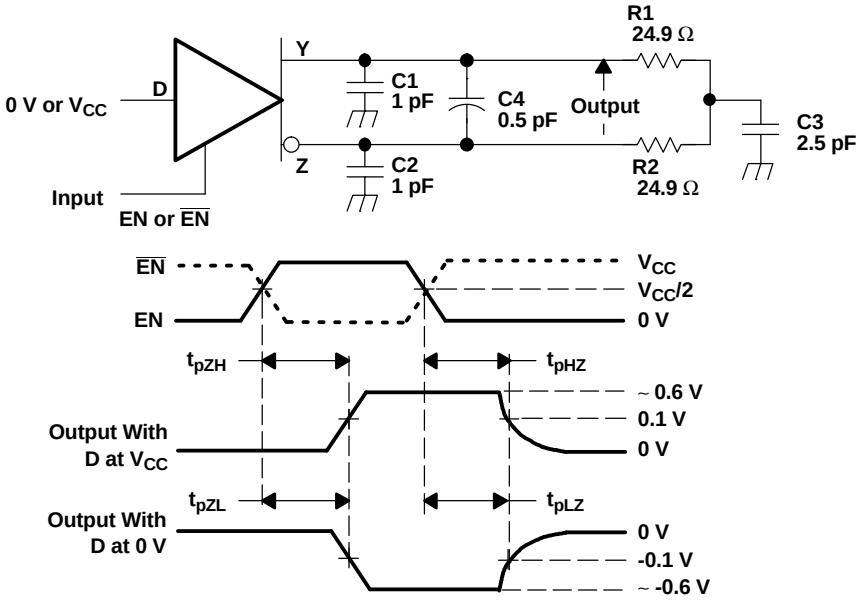
A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, frequency = 500 kHz, duty cycle = 50 ± 5%.

B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.

C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.

D. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, frequency = 500 kHz, duty cycle = 50 ± 5%.

B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.

C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.

D. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 6. Driver Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

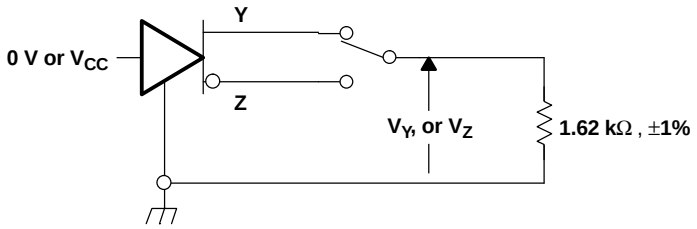
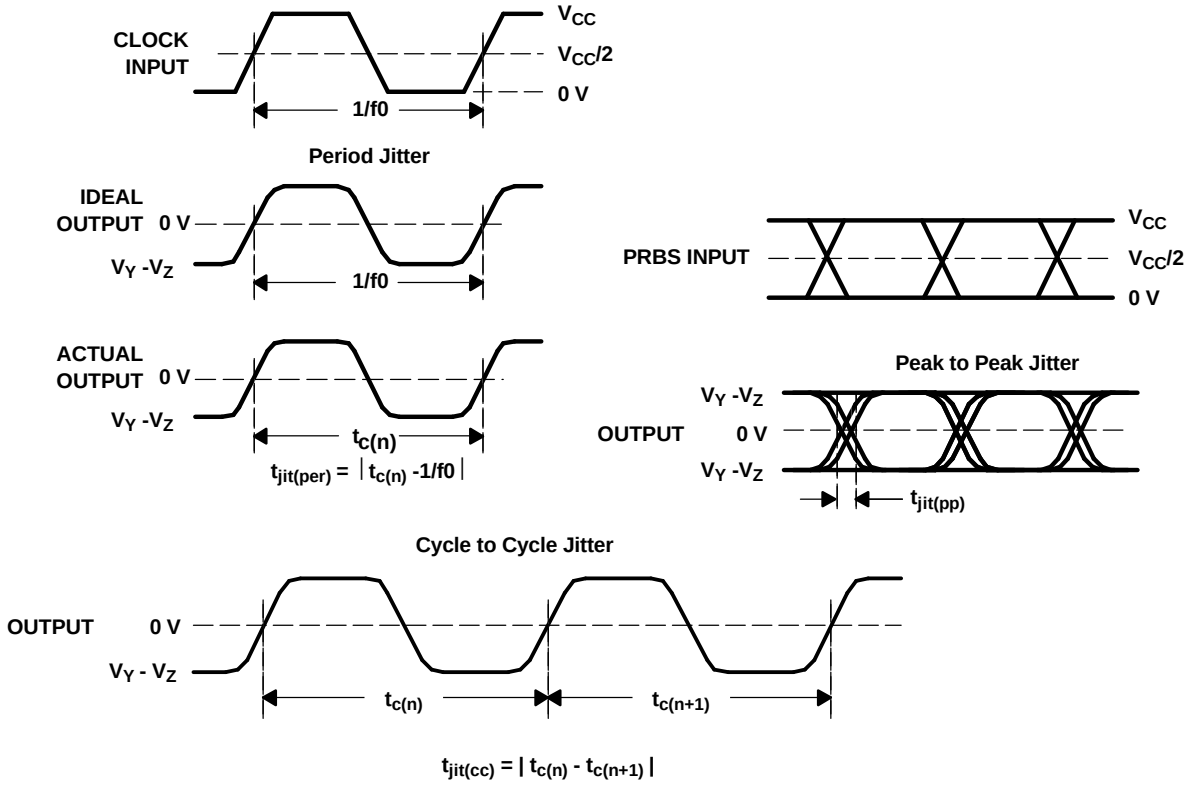


Figure 7. Driver Maximum Steady State Output Voltage



A. All input pulses are supplied by an Agilent 8304A Stimulus System.

B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software

C. Period jitter and cycle-to-cycle jitter are measured using a 100 MHz 50 ±1% duty cycle clock input.

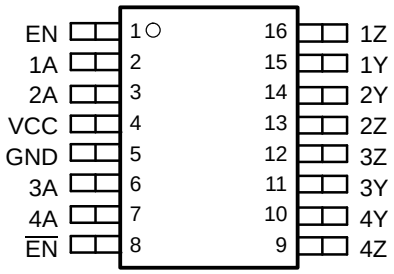
D. Peak-to-peak jitter is measured using a 200 Mbps 2^{15}– 1 PRBS input.

Figure 8. Driver Jitter Measurement Waveforms

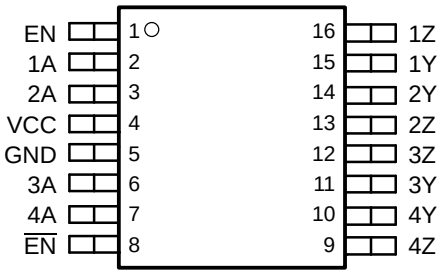
DEVICE INFORMATION

PIN ASSIGNMENTS

D PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



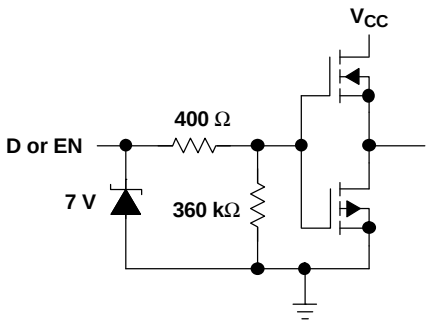
DEVICE FUNCTION TABLE

INPUTS(1)			OUTPUTS(1)	
D	EN	$\overline{EN}$	Y	Z
L	H	L	L	H
H	H	L	H	L
OPEN	H	L	L	H
X	L or OPEN	X	Z	Z
X	X	H or OPEN	Z	Z

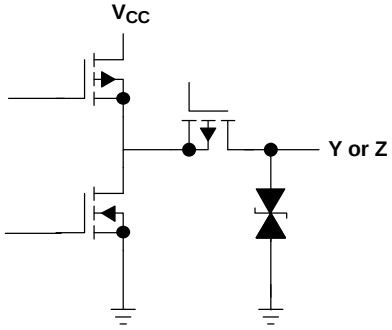
(1) H = high level, L = low level, Z = high impedance, X = Don't Care

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

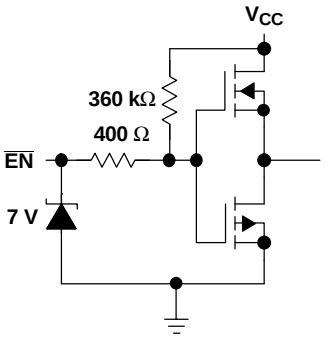
DRIVER INPUT AND POSITIVE DRIVER ENABLE



DRIVER OUTPUT



NEGATIVE DRIVER ENABLE



TYPICAL CHARACTERISTICS

RMS SUPPLY CURRENT
vs
INPUT FREQUENCY

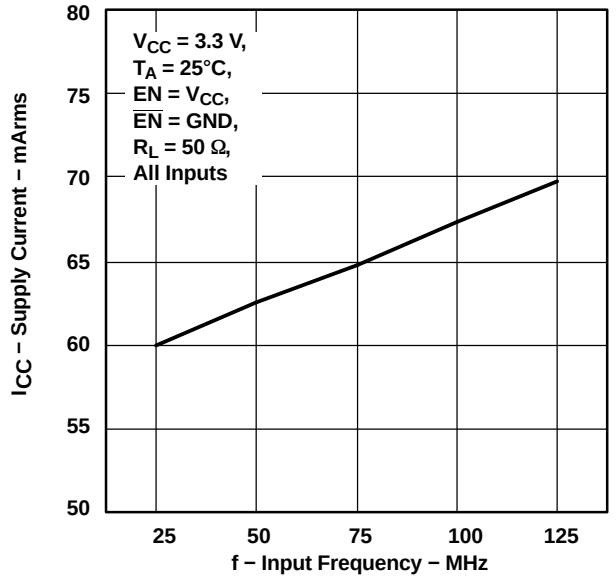


Figure 9.

RMS SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

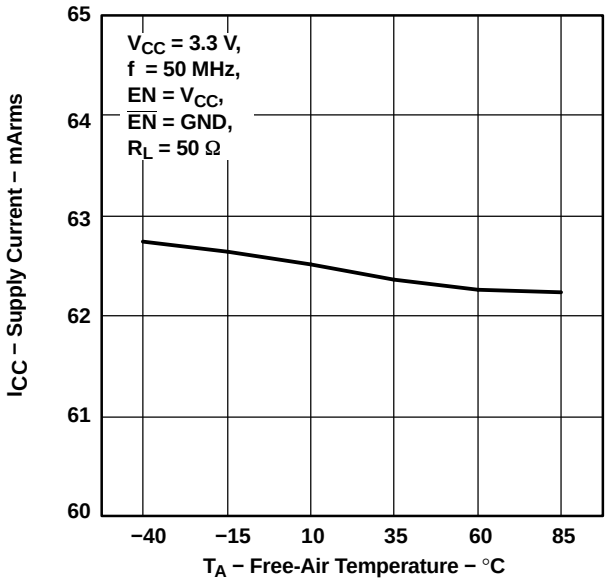


Figure 10.

DIFFERENTIAL OUTPUT VOLTAGE MAGNITUDE
vs
INPUT FREQUENCY

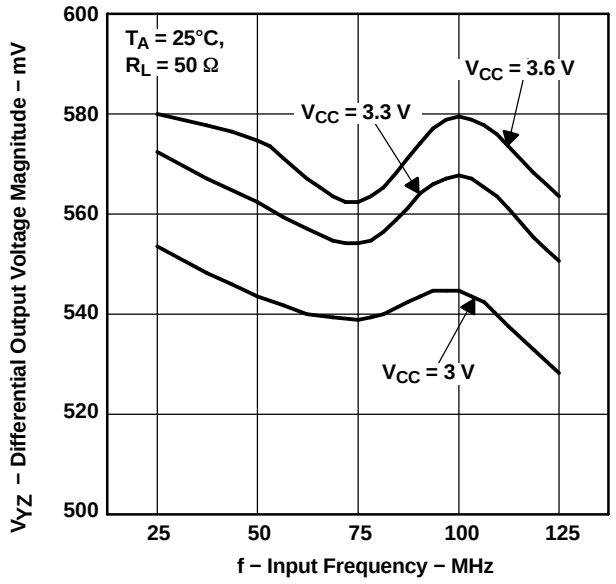


Figure 11.

DRIVER PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

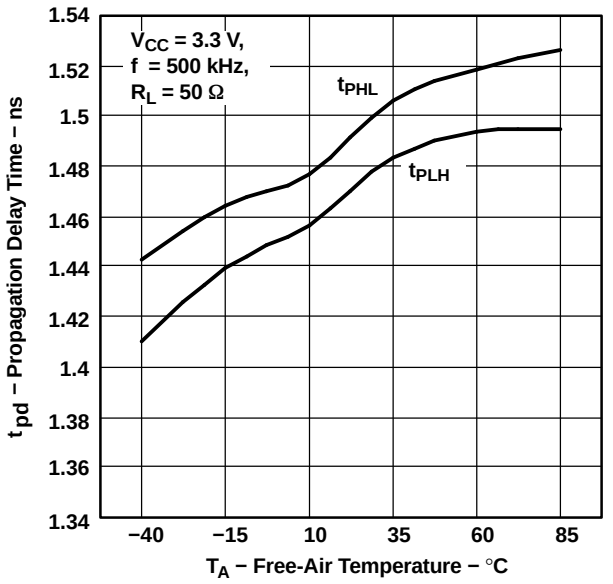


Figure 12.

TYPICAL CHARACTERISTICS (continued)

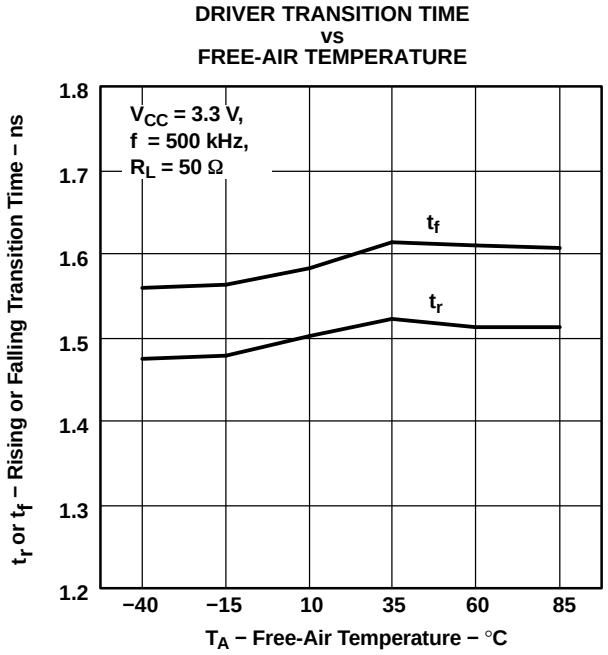


Figure 13.

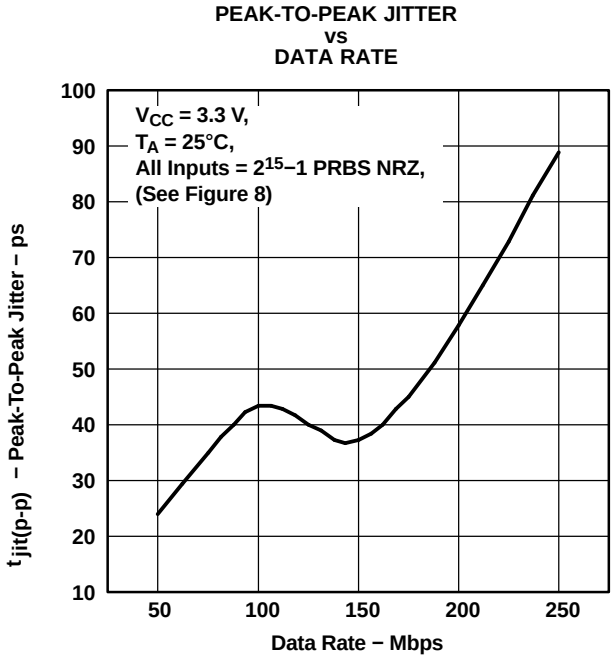


Figure 14.

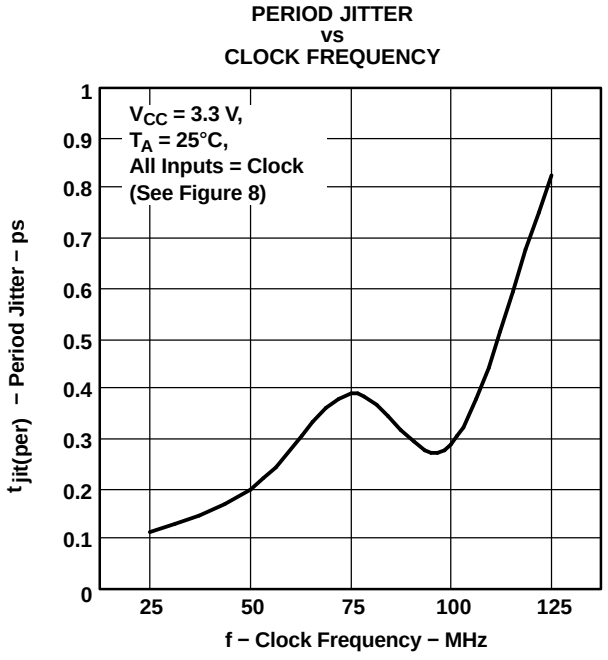


Figure 15.

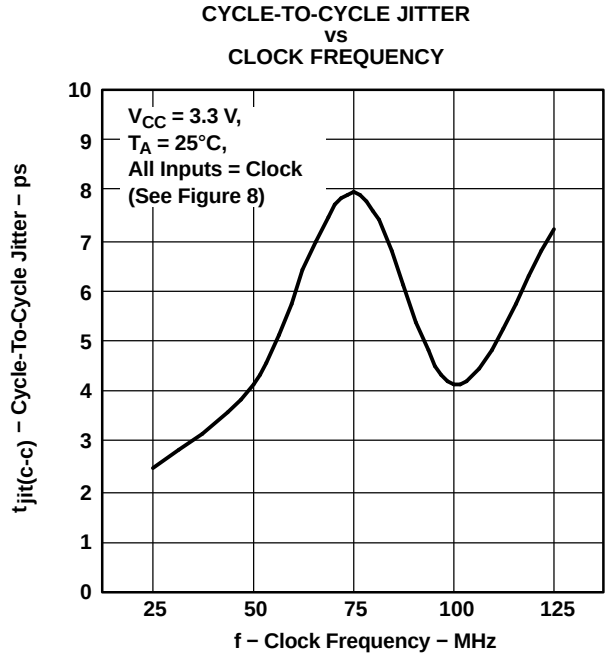


Figure 16.

APPLICATION INFORMATION

Multipoint Configuration

The SN65MLVD047 is designed to allow multipoint communication on a shared bus.

Multipoint is a bus configuration with multiple drivers and receivers present. An example is shown in Figure 17. The figure shows transceivers interfacing to the bus, but a combination of drivers, receivers, and transceivers is also possible. Termination resistors need to be placed on each end of the bus, with the termination resistor value matched to the loaded bus impedance.

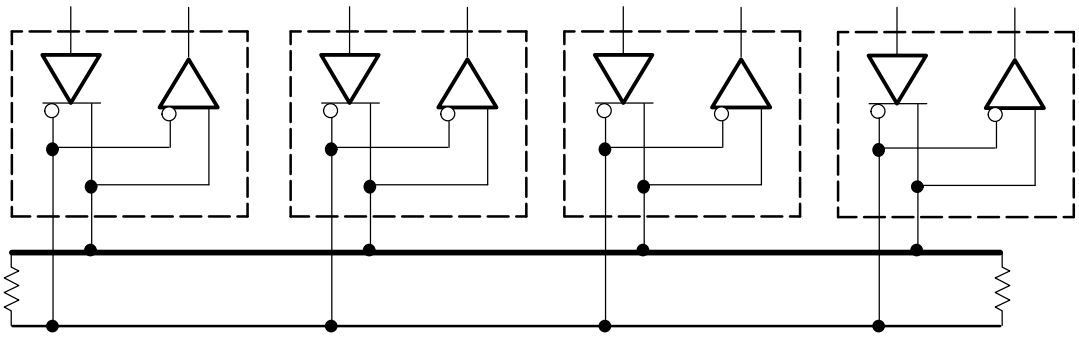


Figure 17. Multipoint Architecture

Multidrop Configuration

Multidrop configuration is similar to multipoint configuration, but only one driver is present on the bus. A multidrop system can be configured with the driver at one end of the bus, or in the middle of the bus. When a driver is located at one end, a single termination resistor is located at the far end, close to the last receiver on the bus. Alternatively, the driver can be located in the middle of the bus, to reduce the maximum flight time. With a centrally located driver, termination resistors are located at each end of the bus. In both cases the termination resistor value should be matched to the loaded bus impedance. Figure 18 shows examples of both cases.

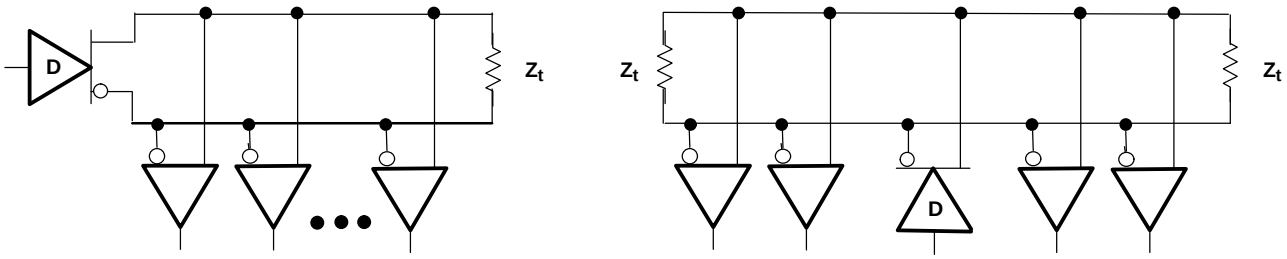


Figure 18. Multidrop Architectures With Different Driver Locations

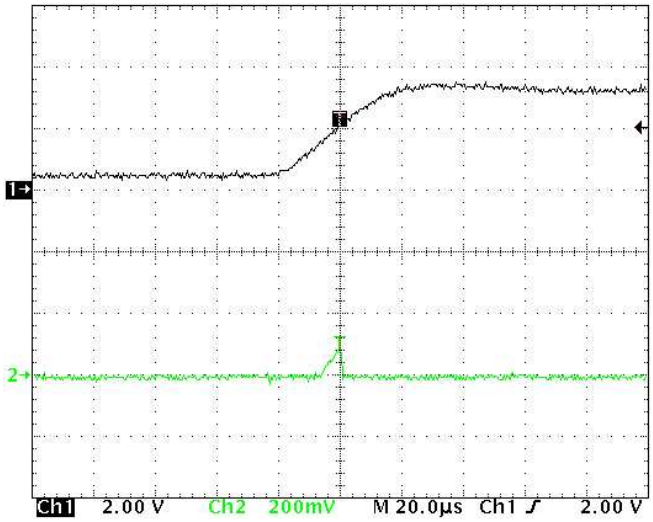
Unused Channel

The SN65MLVD047 is designed to allow multipoint communication on a standard bus. A 360-kΩ pull-down resistor is built in every LVTTL input. The unused driver inputs and outputs may be left floating.

Live Insertion/Glitch Free Power Up/Down

During a live insertion event or a power cycle the outputs of the SN65MLVD047 leave the high impedance state and possibly glitch the bus. Specifically when the V_{CC} applied to the device is between 1.3 and 2.0 VDC the output state (high or low) of the device reflects the input level at the corresponding A pin.

APPLICATION INFORMATION (continued)



Note: Channel 1: V_{CC}, Channel 2: Differential Bus Voltage

The output state of the part during this voltage range is independent of the EN and $\overline{EN}$ pins.

In order to insure that data is not corrupted during a live insertion event or the power cycling of an individual node on a multipoint bus it is important to isolate the outputs of the device from the bus until the V_{CC} has reached at least 2.0 VDC. At this voltage level the device output state accurately reflects the logic conditions as defined in the Device Function Table.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65MLVD047D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD047DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD047DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD047DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD047PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD047PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD047PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD047PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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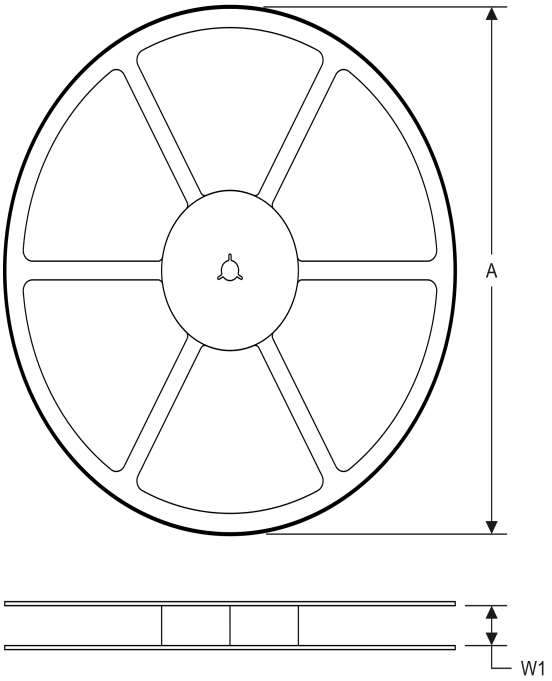
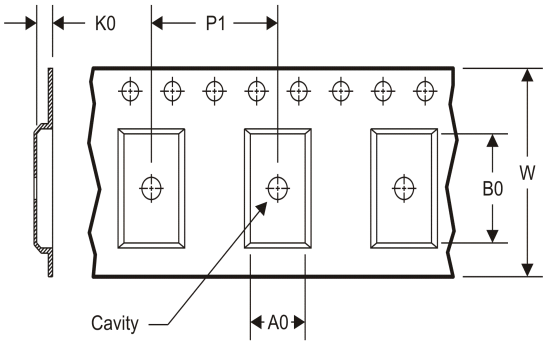
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



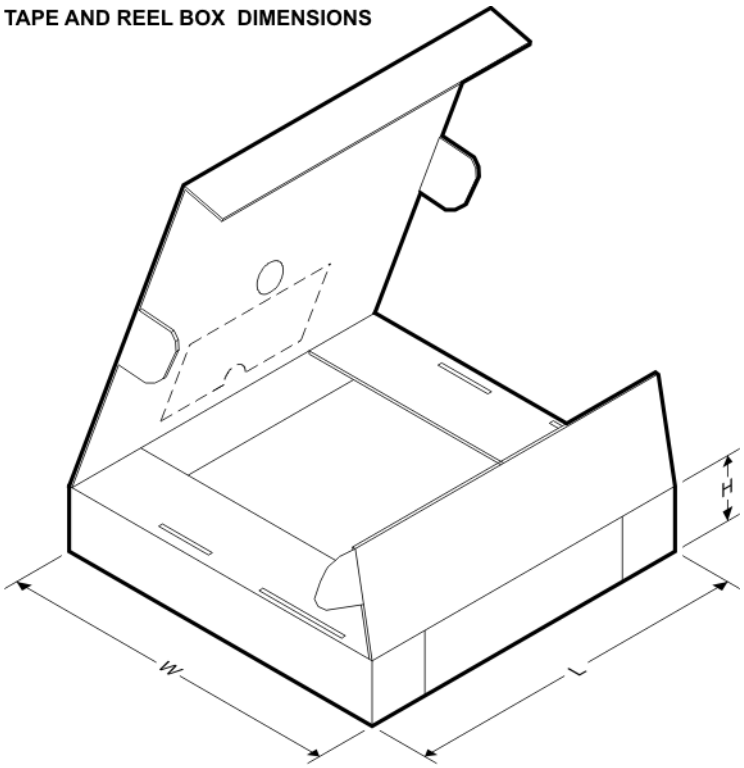
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD047DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65MLVD047PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

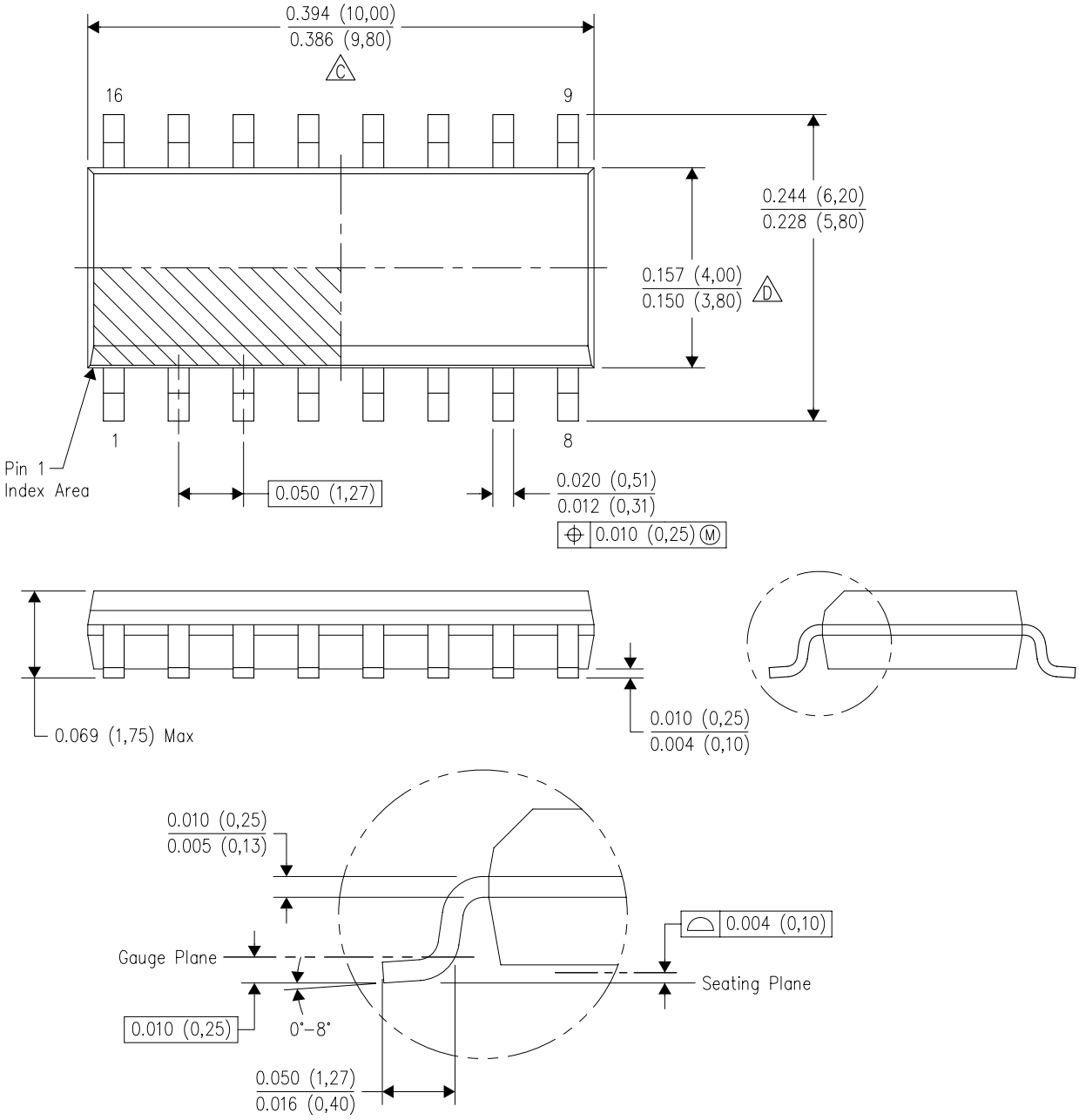
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

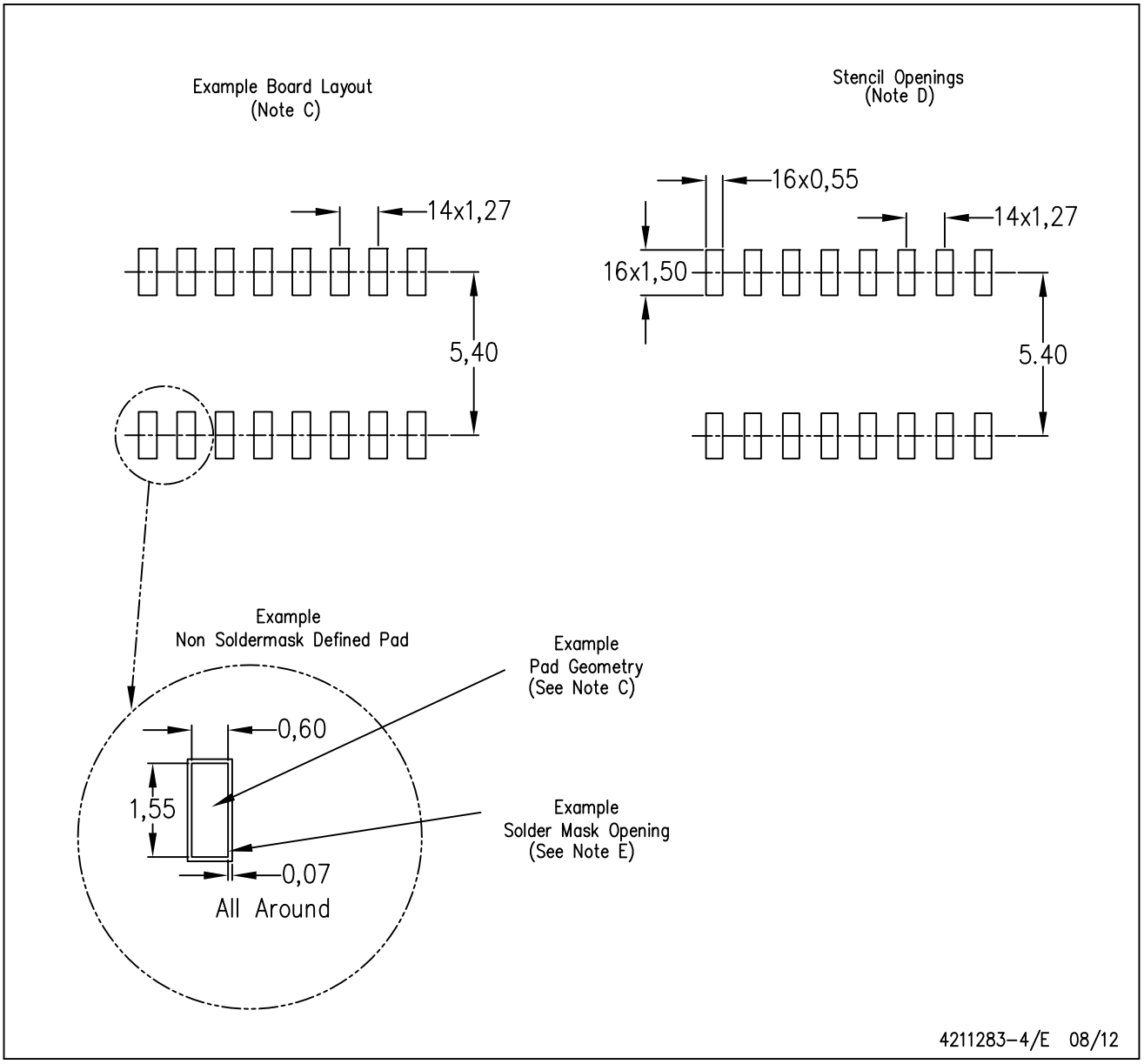
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD047DR	SOIC	D	16	2500	367.0	367.0	38.0
SN65MLVD047PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



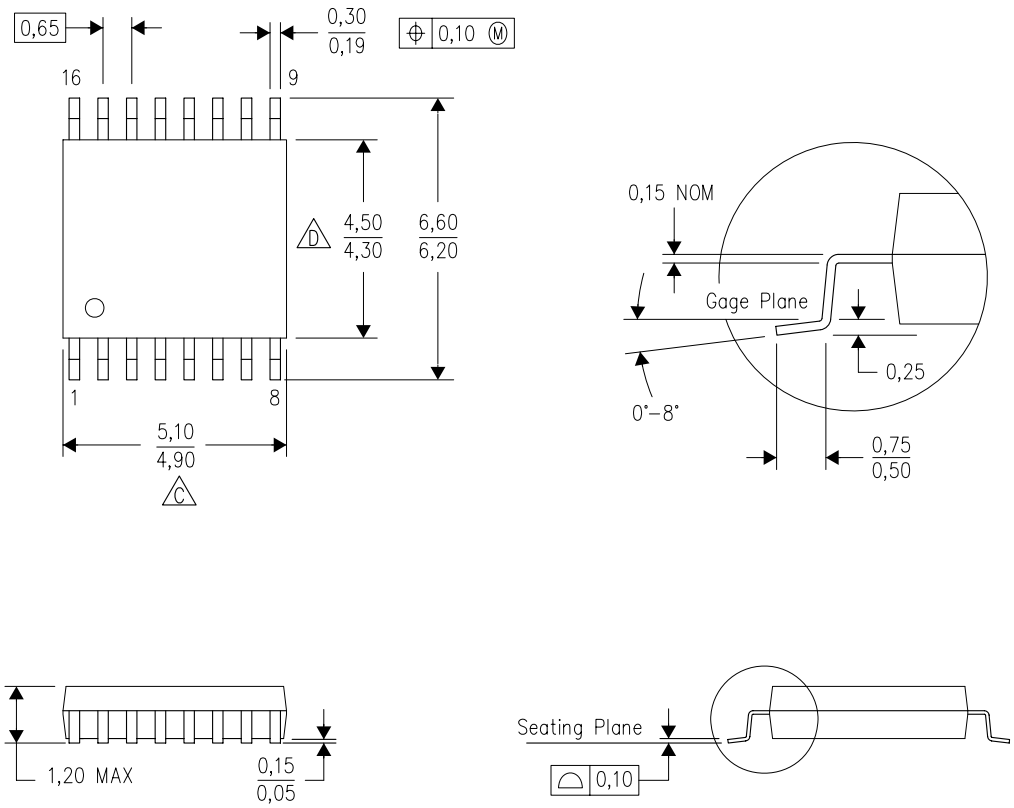
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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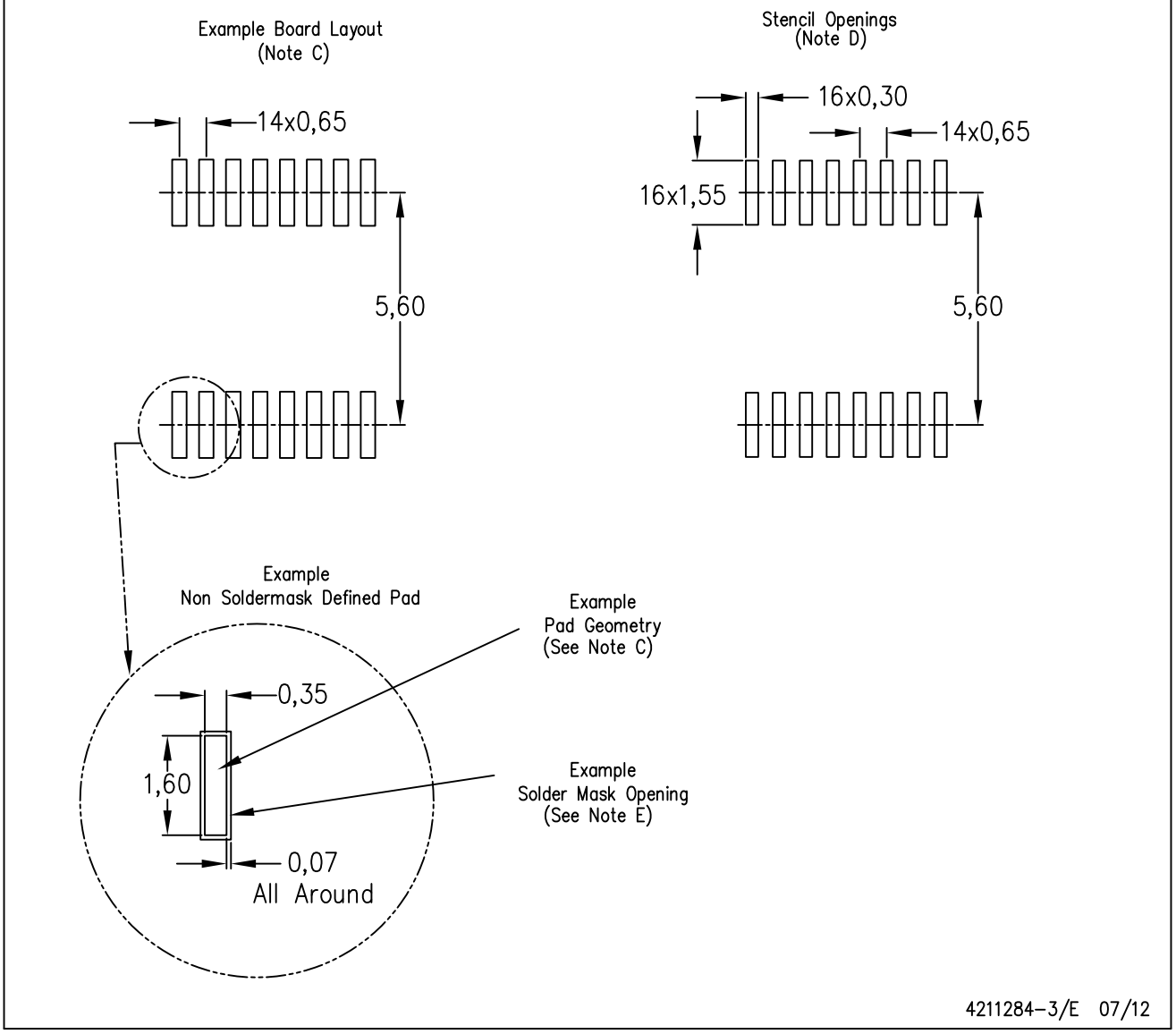
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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