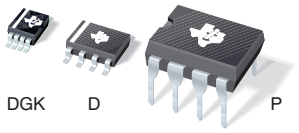


HALF-DUPLEX RS-485 TRANSCEIVER

FEATURES

- **Bus-Pin ESD Protection Up to 15 kV**
- **1/2 Unit Load–Up to 64 Nodes on a Bus**
- **Bus-Open-Failsafe Receiver**
- **Glitch-Free Power-Up/Down Bus Inputs and Outputs**
- **Available in Small MSOP-8 Package**
- **Meets or Exceeds the Requirements of the TIA/EIA-485A Standard**
- **Industry-Standard SN75176 Footprint**

APPLICATIONS

- **Motor Control**
- **Power Inverters**
- **Industrial Automation**
- **Building Automation Networks**
- **Industrial Process Control**
- **Battery-Powered Applications**
- **Telecommunications Equipment**

DESCRIPTION

The SN65HVD485E is a half-duplex transceiver designed for RS-485 data bus networks. Powered by a 5V supply, it is fully compliant with the TIA/EIA-485A standard. This device is suitable for data transmission up to 10Mbps over long twisted-pair cables and is designed to operate with very low supply current, typically less than 2mA, exclusive of the load. When in the inactive shutdown mode, the supply current drops below 1mA.

The wide common-mode range and high ESD protection levels of this device make it suitable for demanding applications such as, electrical inverters, status/command signals across telecom racks, cabled chassis interconnects, and industrial automation networks where noise tolerance is essential. The SN65HVD485E matches the industry-standard footprint of the SN75176. Power-on reset circuits keep the outputs in a high-impedence state until the supply voltage has stabilized. A thermal shutdown function protects the device from damage due to system fault conditions. The SN65HVD485E is characterized for operation from –40°C to 85°C air temperature.

IMPROVED REPLACEMENT FOR:		
PART NUMBER	**REPLACE WITH**	
ADM485	HVD485E:	Better ESD protection (±15 kV vs unspecified) Faster signaling rate (10 Mbps vs 5 Mbps) More nodes on a bus (64 vs. 32) Wider power supply tolerance (10% vs 5%)
SP485E	HVD485E:	More nodes on a bus (64 vs. 32) Wider power supply tolerance (10% vs. 5%)
LMS485E	HVD485E:	Higher signaling rate (10 Mbps vs 2.5 Mbps) More nodes on a bus (64 vs 32) Wider power supply tolerance (10% vs 5%)
DS485	HVD485E:	Higher signaling rate (10 Mbps vs 2.5 Mbps) Better ESD (±15 kV vs ±2 kV) More nodes on a bus (64 vs 32) Wider power supply tolerance (10% vs 5%)
LTC485	HVD485E:	Better ESD (±15 kV vs ±2 kV) Wider power supply tolerance (10% vs 5%)
MAX485E	HVD485E:	Higher signaling rate (10 Mbps vs 2.5 Mbps) More nodes on a bus (64 vs 32) Wider power supply tolerance (10% vs 5%)
ST485E	HVD485E:	Higher signaling rate (10 Mbps vs 5 Mbps) Wider power supply tolerance (10% vs 5%)
ISL8485E	HVD485:	More nodes on a bus (64 vs 32) Faster signaling rate (10 Mbps vs 5 Mbps)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE TYPE		
	P	D(1)	DGK(2)
–40°C to 85°C	SN65HVD485EP Marked as 65HVD485	SN65HVD485ED Marked as VP485	SN65HVD485EDGK Marked as NWJ

(1) The D package is available taped and reeled. Add an R suffix to the device type (i.e., SN65HVD485EDR).
(2) The DGK package is available taped and reeled. Add an R suffix to the device type (i.e., SN65HVD485EDGKR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)(2)

		VALUE	UNIT
V_{CC}	Supply voltage range,	-0.5 to 7	V
	Voltage range at A or B	-9 to 14	V
	Voltage range at any logic pin	–0.3 to V_{CC} + 0.3	V
	Receiver output current	–24 to 24	mA
	Voltage input range, transient pulse, A and B, through 100Ω (see Figure 13)	–50 V to 50	V
	Storage temperature range	–65 to 130	°C
T_J	Junction temperature	170	°C
	Continuous total power dissipation	Refer to Package Dissipation Table	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

PACKAGE DISSIPATION RATINGS

PACKAGE(1)	JEDEC BOARD MODEL	T_A < 25°C POWER RATING	DERATING FACTOR(2) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	Low k(3)	507 mW	4.82 mW/°C	289 mW	217 mW
	High k(3)	824 mW	7.85 mW/°C	471 mW	353 mW
P	Low k(3)	686 mW	6.53 mW/°C	392 mW	294 mW
DGK	Low k(3)	394 mW	3.76 mW/°C	255 mW	169 mW
	High k(4)	583 mW	5.55 mW/°C	333 mW	250 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(3) In accordance with the low-k thermal metric definitions of EIA/JESD51-3.
(4) In accordance with the high-k thermal metric definitions of EIA/JESDS1-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)		–7		12	V
V_{IH}	High-level input voltage (D, DE, or RE inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (D, DE, or RE inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate		0		10	Mbps
T_A	Operating free-air temperature		–40		85	°C
T_J	Junction temperature(2)		–40		130	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) See thermal characteristics table for information on maintenance of this specification for the DGK package.

SUPPLY CURRENT

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Driver and receiver enabled	D at V_{CC} or open or 0V,	DE at V_{CC}, RE at 0V, No load			2	mA
	Driver and receiver disabled	D at V_{CC} or open,	DE at 0V, RE at V_{CC}			1	mA

(1) All typical values are at 25°C and with a 5-V supply.

ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Human body model	Bus terminals and GND		±15		kV
Human body model(2)	All pins		±4		kV
Charged-device-model(3)	All pins		±1		kV

(1) All typical values at 25°C
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage	I_O = 0, No load	3	4.3		V
		R_L = 54 W, See Figure 1	1.5	2.3		
		V_{TEST} = –7 V to 12 V, See Figure 2	1.5			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	See Figure 1 and Figure 2	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		–0.1	0	0.1	V
$V_{OC(PP)}$	Common-mode output voltage	See Figure 3		500		mV
I_{OZ}	High-impedance output current	See receiver input currents				µA
I_I	Input current	D, DE	–100		100	µA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V, See Figure 7	–250		250	mA

(1) All typical values are at 25°C and with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See Figure 4			30	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	
t_r	Differential output signal rise time				25	
t_f	Differential output signal fall time				25	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				5	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V, See Figure 5			150	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output				100	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V See Figure 6			150	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				100	
$t_{PZH(SHN)}$	Propagation delay time, shutdown-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at VCC, See Figure 5			2600	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at VCC, See Figure 6			2600	ns

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA		–85	–10	mV
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA	–200	–115		mV
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})			30		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA, See Figure 8	4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OH} = 8 mA, See Figure 8		0.15	0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 to V_{CC}, $\overline{RE}$ = V_{CC}	–1		1	µA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V			0.5	mA
		V_{IH} = 12 V, V_{CC} = 0			0.5	
		V_{IH} = –7 V, V_{CC} = 5 V	–0.4			
		V_{IH} = –7 V, V_{CC} = 0	–0.4			
I_{IH}	High-level input current ($\overline{RE}$)	V_{IH} = 2 V	–60	–30		µA
I_{IL}	Low-level input current ($\overline{RE}$)	V_{IL} = 0.8 V	–60	–30		µA
C_{diff}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		7		pF

(1) All typical values are at 25°C and with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, See Figure 9			200	ns
t_{PHL}	Propagation delay time, high-to-low-level output				200	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			6		
t_r	Output signal rise time				3	ns
t_f	Output signal fall time				3	
t_{PZH}	Output enable time to high level	C_L = 15 pF, DE at 3 V, See Figure 10 and Figure 11			50	ns
t_{PZL}	Output enable time to low level				50	
t_{PHZ}	Output enable time from high level				50	
t_{PLZ}	Output enable time from low level				50	
$t_{PZH(SHDN)}$	Propagation delay time, shutdown-to-high-level output	C_L = 15 pF, DE at 0 V, See Figure 12			3500	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output				3500	

PARAMETER MEASUREMENT INFORMATION

NOTE:

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise and fall time <6 ns, pulse rate 100kHz, 50% duty cycle. Z_O = 50Ω (unless otherwise specified).

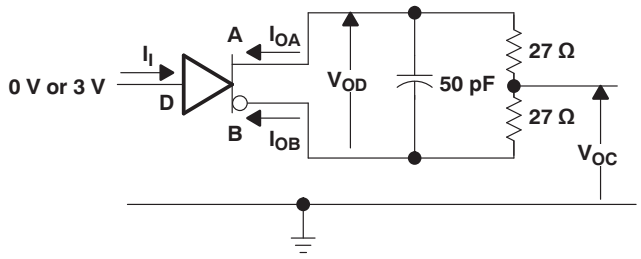


Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

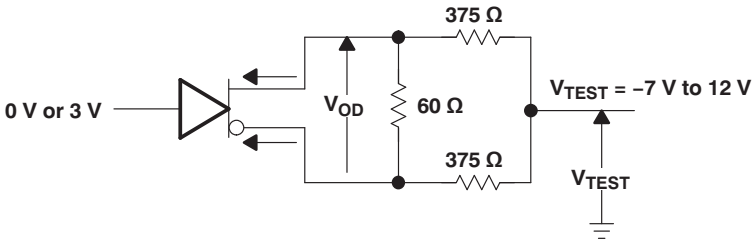


Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading

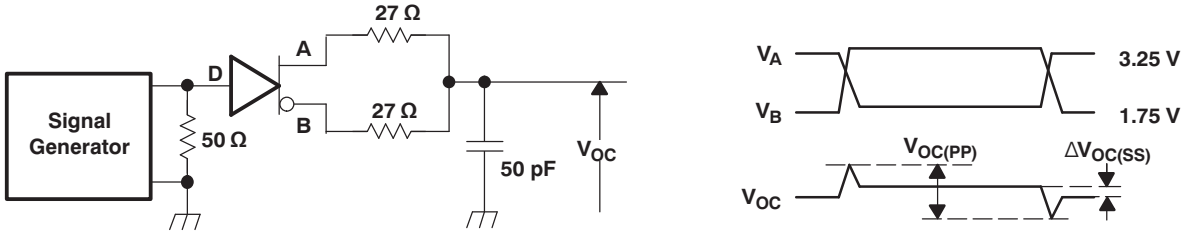


Figure 3. Driver V_{OC} Test Circuit and Waveforms

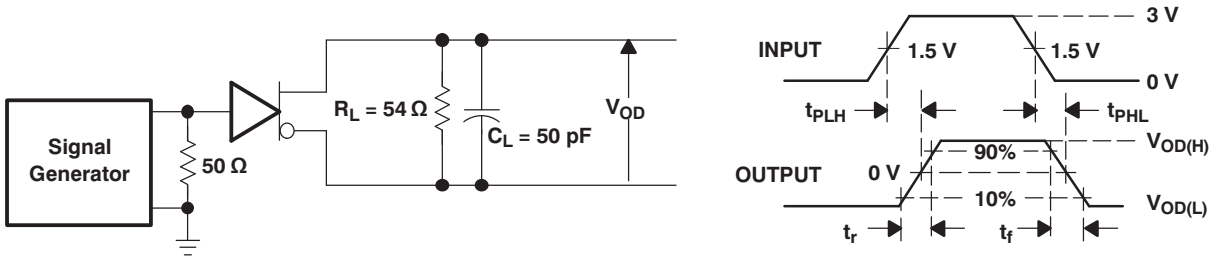


Figure 4. Driver Switching Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

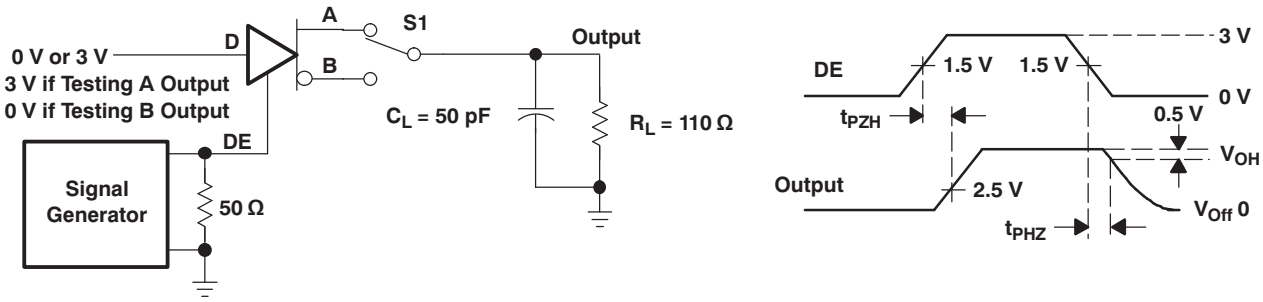


Figure 5. Driver Enable/Disable Test Circuit and Waveforms, High Output

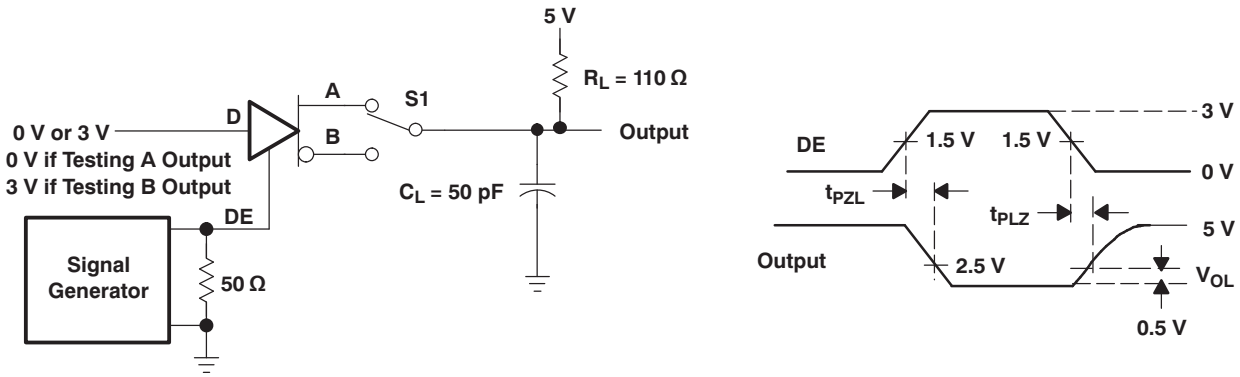


Figure 6. Driver Enable/Disable Test Circuit and Waveforms, Low Output

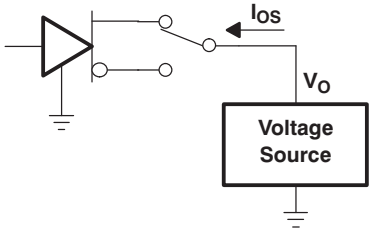


Figure 7. Driver Short-Circuit Test

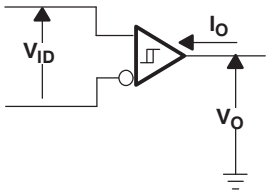
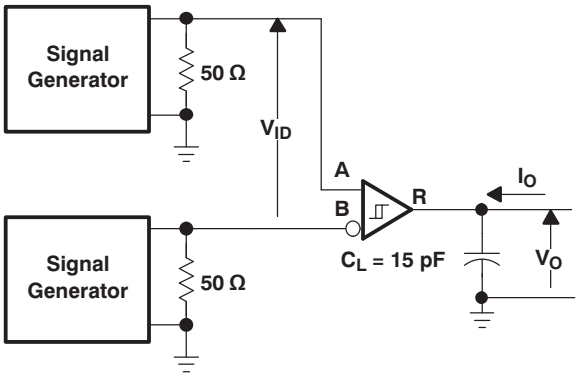


Figure 8. Receiver Parameter Definitions



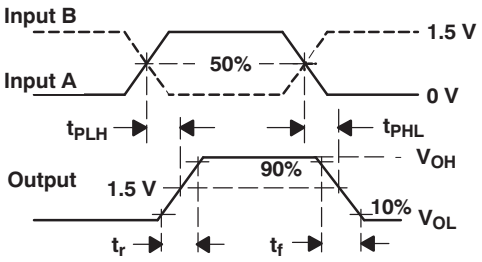


Figure 9. Receiver Switching Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

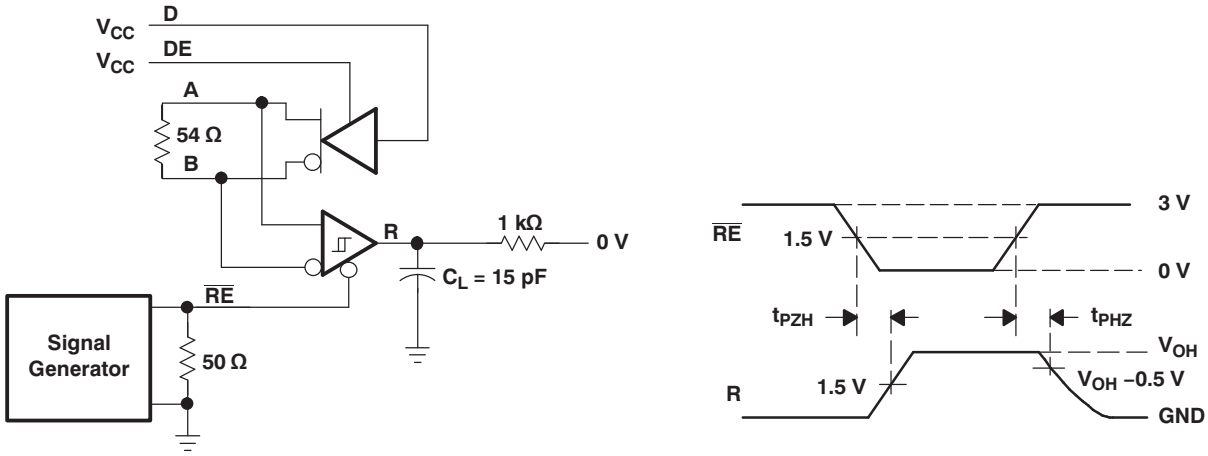


Figure 10. Receiver Enable/Disable Test Circuit and Waveforms, Data Output High

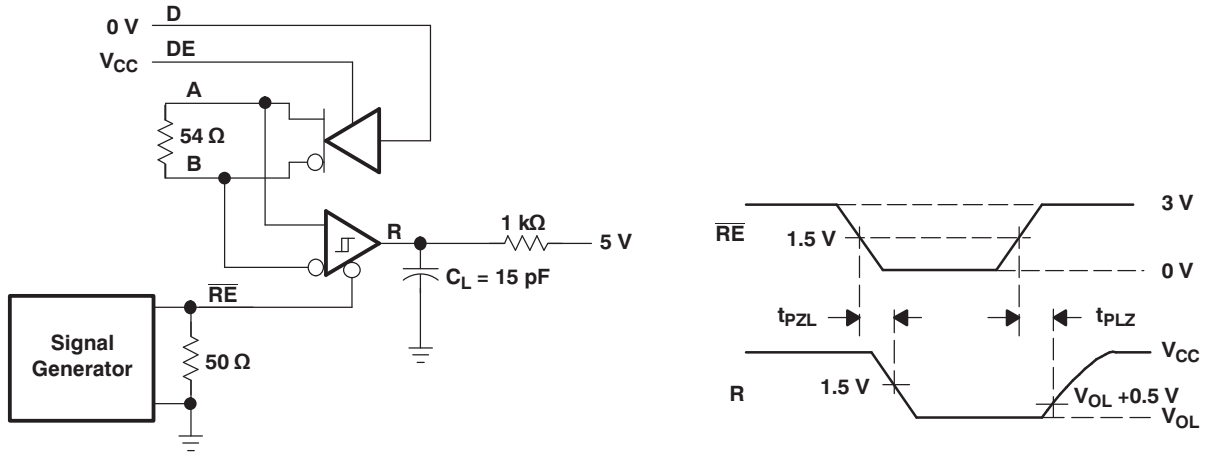


Figure 11. Receiver Enable/Disable Test Circuit and Waveforms, Data Output Low

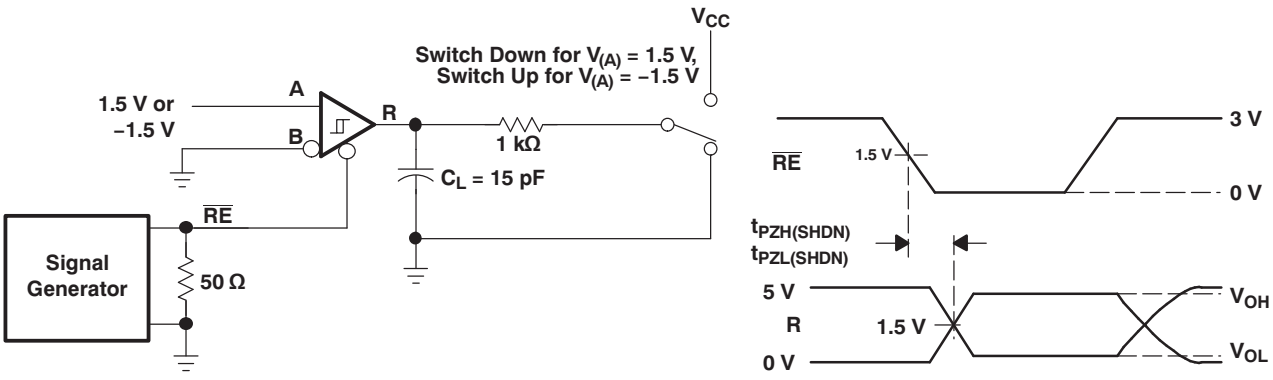


Figure 12. Receiver Enable From Shutdown Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

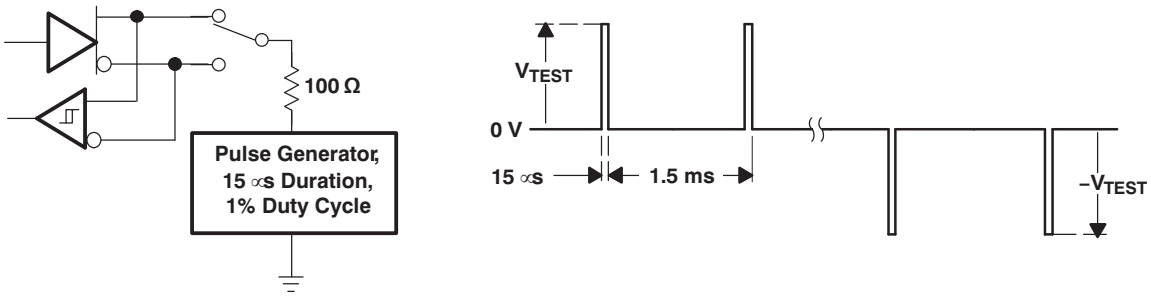
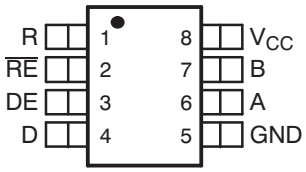


Figure 13. Test Circuit and Waveforms, Transient Over-Voltage Test

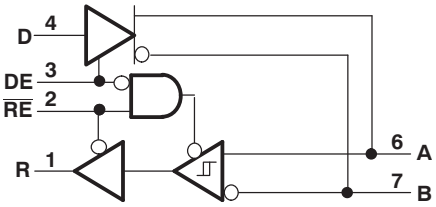
DEVICE INFORMATION

PIN ASSIGNMENTS

D, P OR DGK PACKAGE
(TOP VIEW)



LOGIC DIAGRAM (POSITIVE LOGIC)

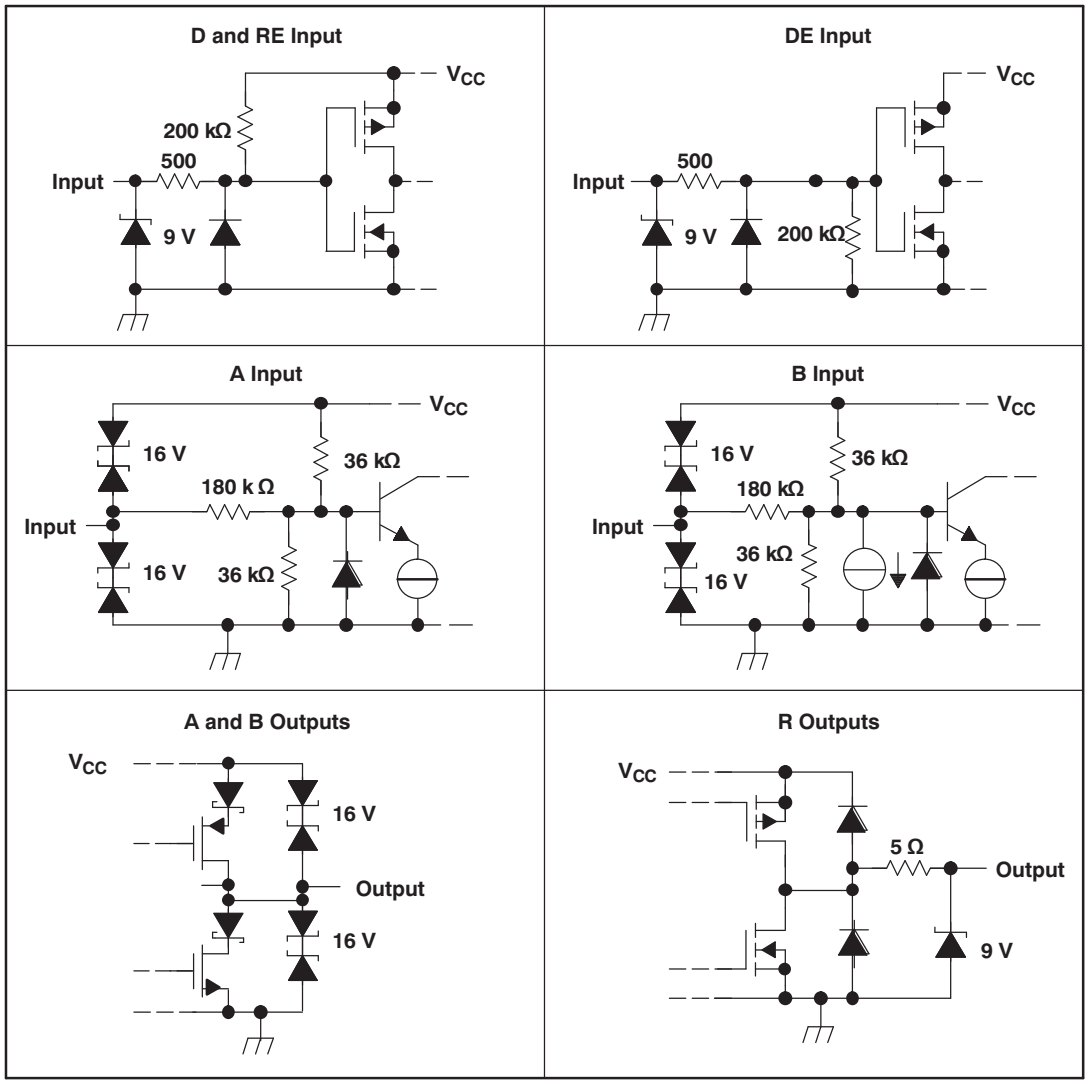


FUNCTION TABLE(1)

DRIVER				RECEIVER		
INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B	DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
H	H	H	L	$V_{ID} \leq -0.2$ V	L	L
L	H	L	H	-0.2 V $< V_{ID} < -0.01$ V	L	?
X	L	Z	Z	-0.01 V $\leq V_{ID}$	L	H
Open	H	H	L	X	H	Z
X	Open	Z	Z	Open circuit	L	H
				X	Open	Z

(1) H= high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



THERMAL CHARACTERISTICS

DGK PACKAGE						
PARAMETER			MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(1)	Low-k(2) board, no air flow		266		°C/W
		High-k(3) board, no air flow		180		
θ_{JB}	Junction-to-board thermal resistance	High-k(3) board, no air flow		108		°C/W
θ_{JC}	Junction-to-case thermal resistance			66		
$P_{(AVG)}$	Average power dissipation	R_L = 54Ω, Input to D is a 10 Mbps 50% duty cycle square wave V_{CC} at 5.5 V, T_J = 130°C			219	mW
T_A	Ambient air temperature	JEDEC High K board model	–40		93	°C
		JEDEC Low K board model	–40		75	°C
T_{SD}	Thermal shut-down junction temperature			165		°C

(1) See TI application note SZZA003, Package Thermal Characterization Methodologies, for an explanation of this parameter.
(2) JESD51-3 Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
(3) JESD51-7 High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

TYPICAL CHARACTERISTICS

BUS INPUT CURRENT vs BUS INPUT VOLTAGE

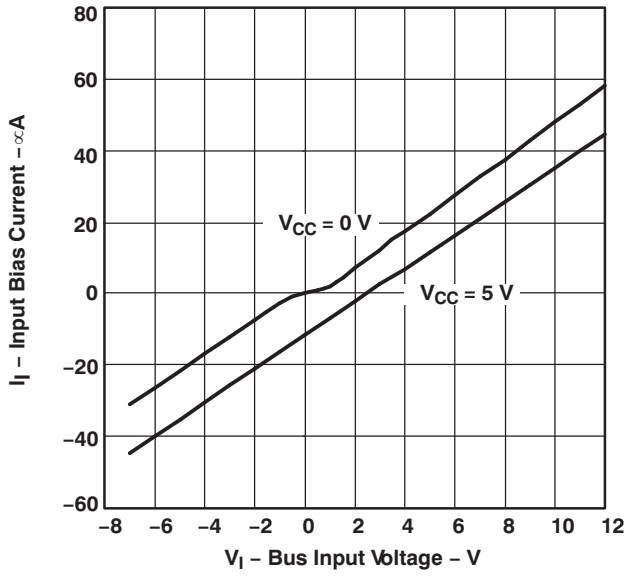


Figure 14.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs DIFFERENTIAL OUTPUT CURRENT

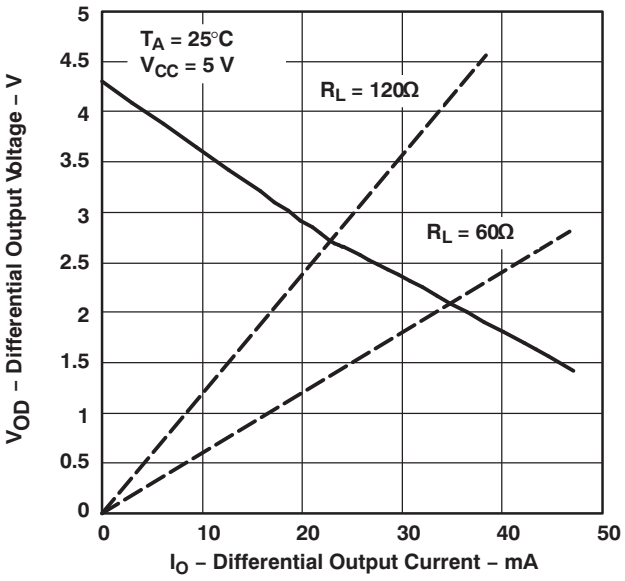
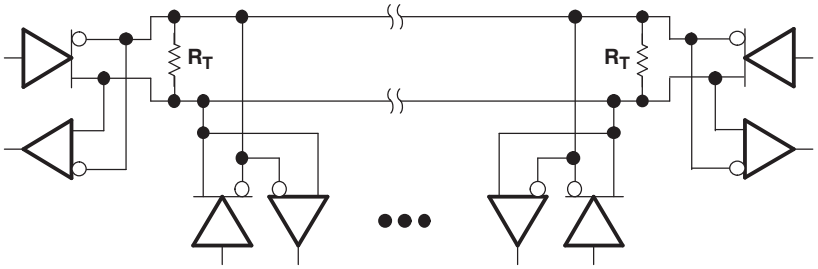


Figure 15.

APPLICATION INFORMATION



NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 16. Typical Application Circuit

POWER USAGE IN AN RS-485 TRANSCEIVER

Power consumption is a concern in many applications. Power supply current is delivered to the bus load as well as to the transceiver circuitry. For a typical RS-485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes, plus the termination resistors at each end of the bus.

The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485-A standard defines a unit load as allowing up to 1mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32mA. The HVD485E is rated as a 1/2 unit load device, so up to 64 can be connected on a bus.

The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5V of differential signal. For a bus terminated with one standard 120-Ω resistor at each end, this sums to 25 mA differential output current whenever the bus is active. Typically the HVD485E can drive more than 25mA to a 60Ω load, resulting in a differential output voltage higher than the minimum required by the standard. (See Figure 15.)

Supply current increases with signaling rate primarily due to the totum pole outputs of the driver. When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting and this creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

APPLICATION INFORMATION (continued)

THERMAL CHARACTERISTICS OF IC PACKAGES

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives average in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives best case in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 17).

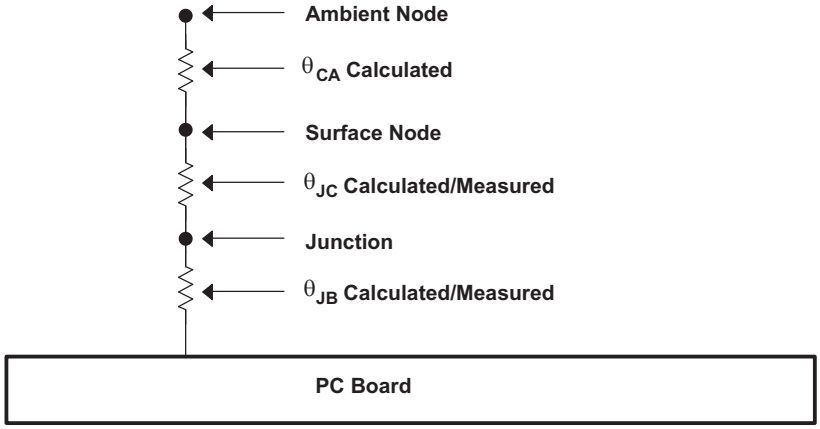


Figure 17. Thermal Resistance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65HVD485ED	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD485EDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD485EDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD485EDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD485EDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD485EDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD485EDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD485EDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD485EP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN65HVD485EPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

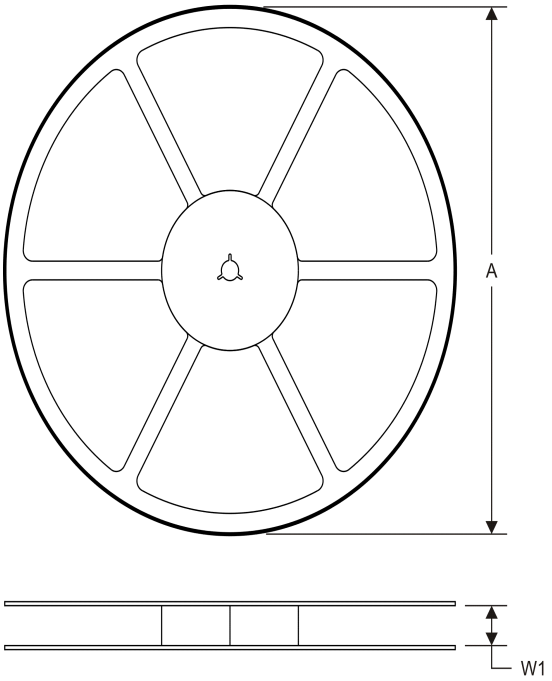
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

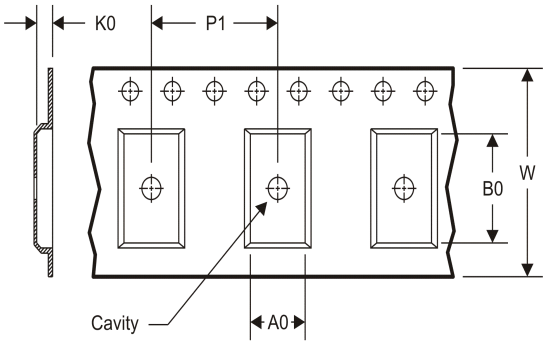
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



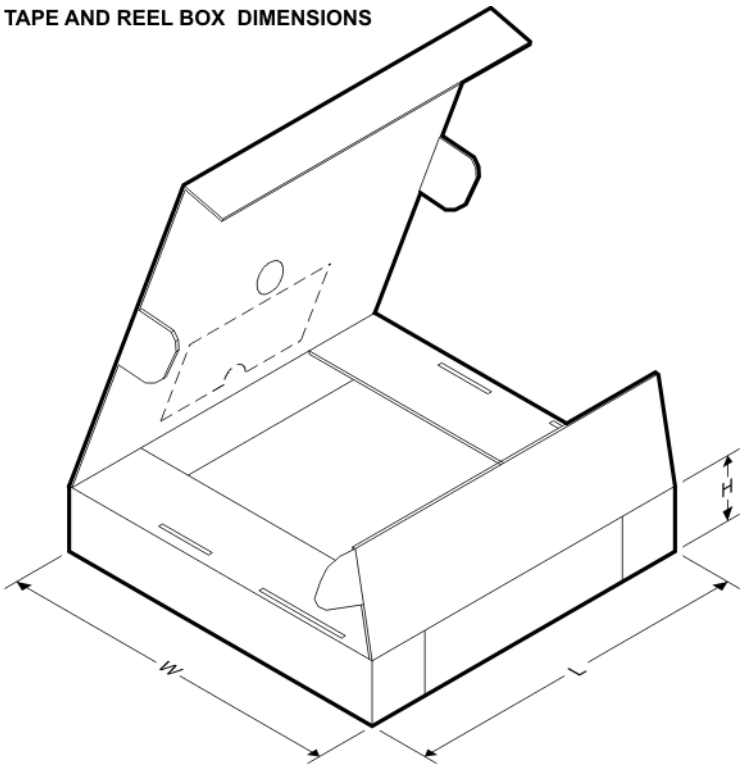
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD485EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD485EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

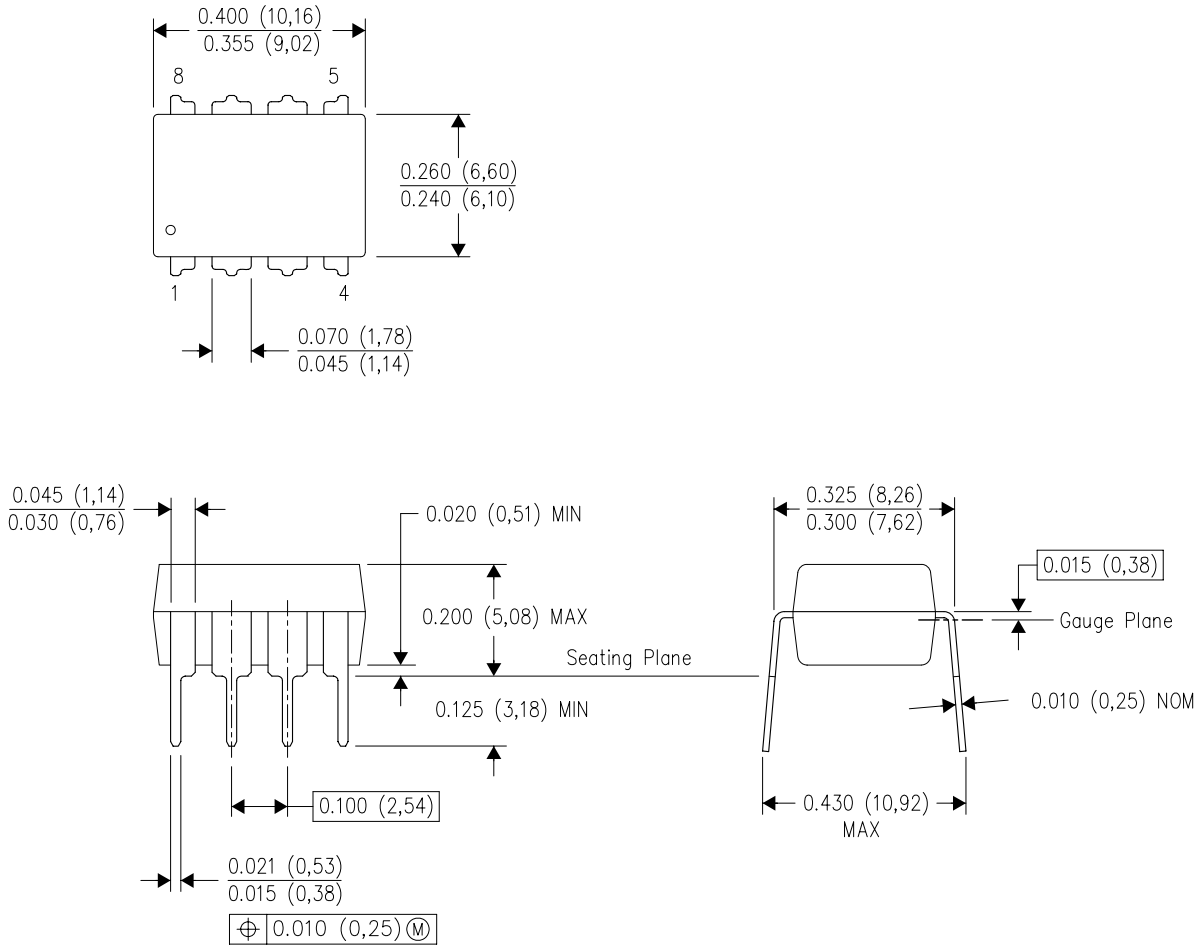
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

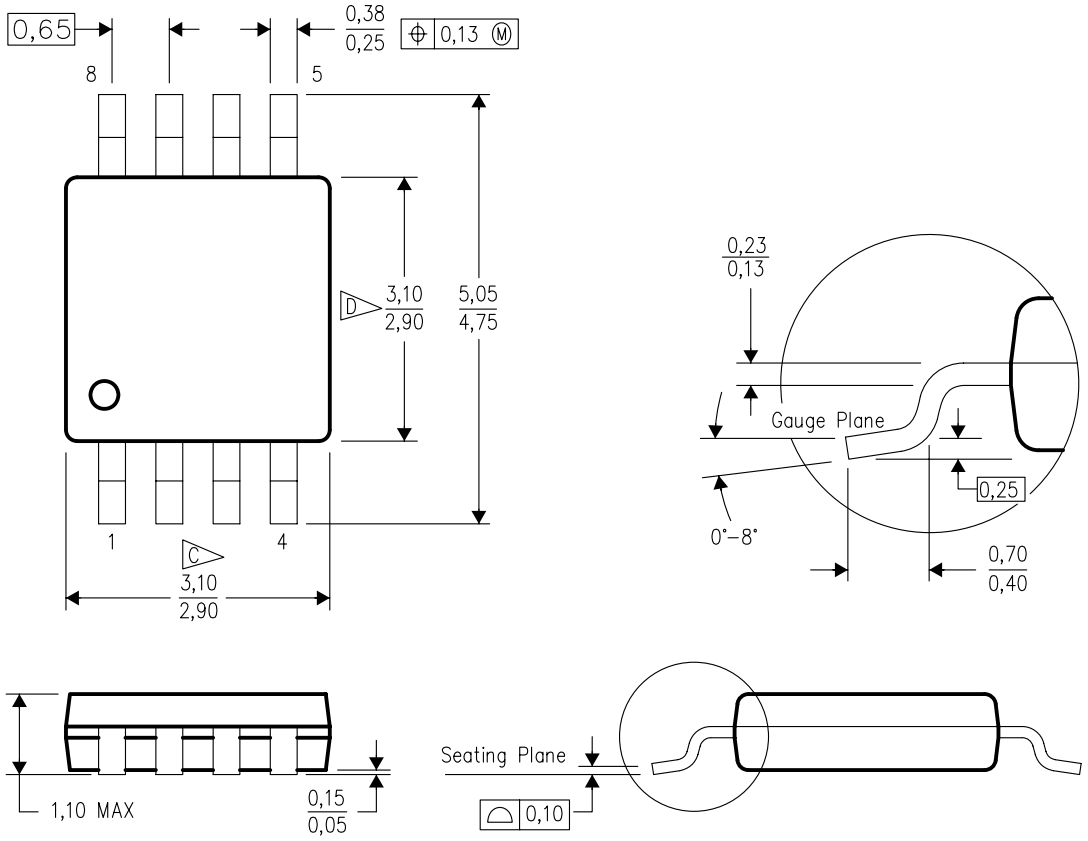
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD485EDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65HVD485EDR	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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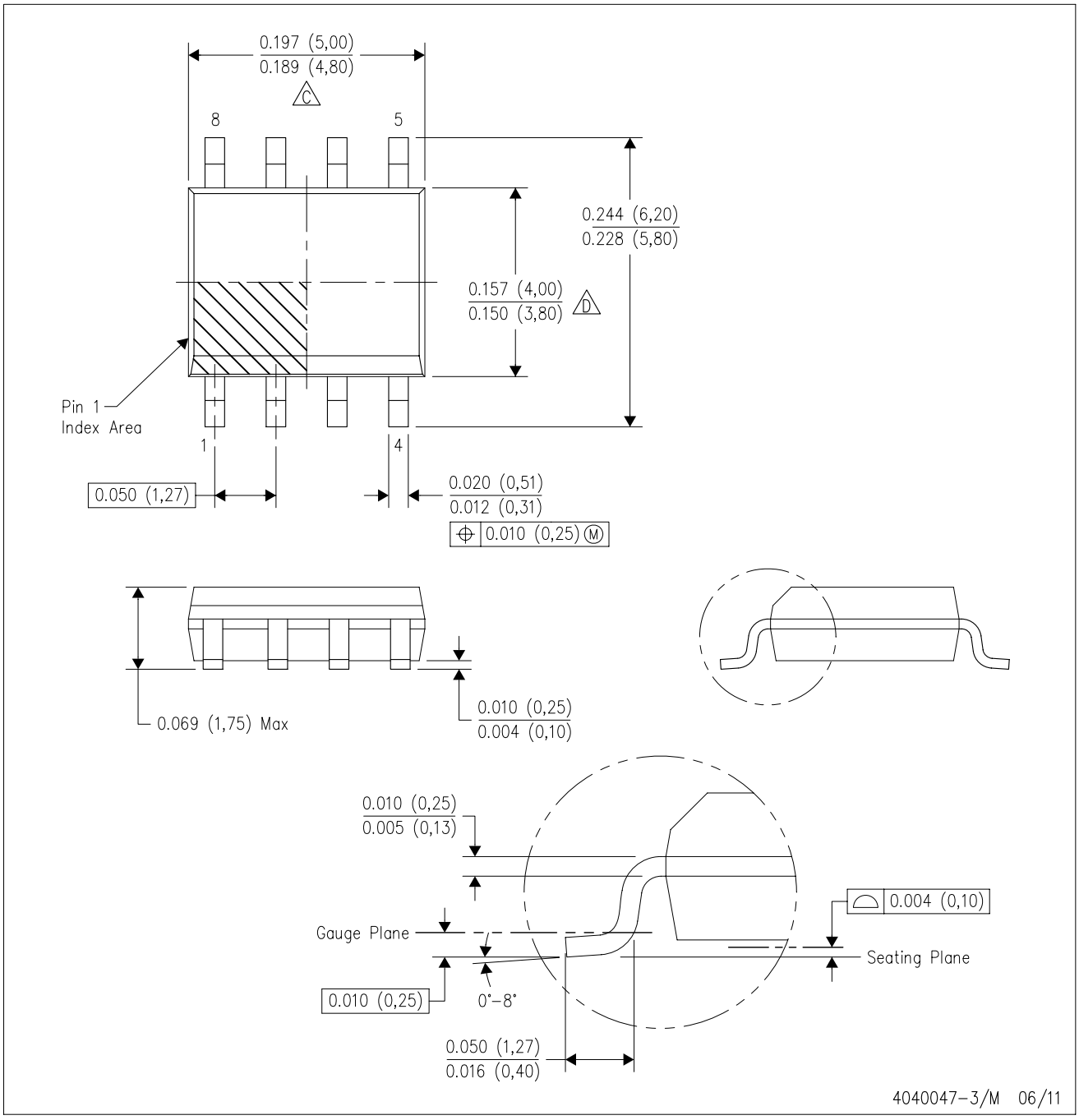
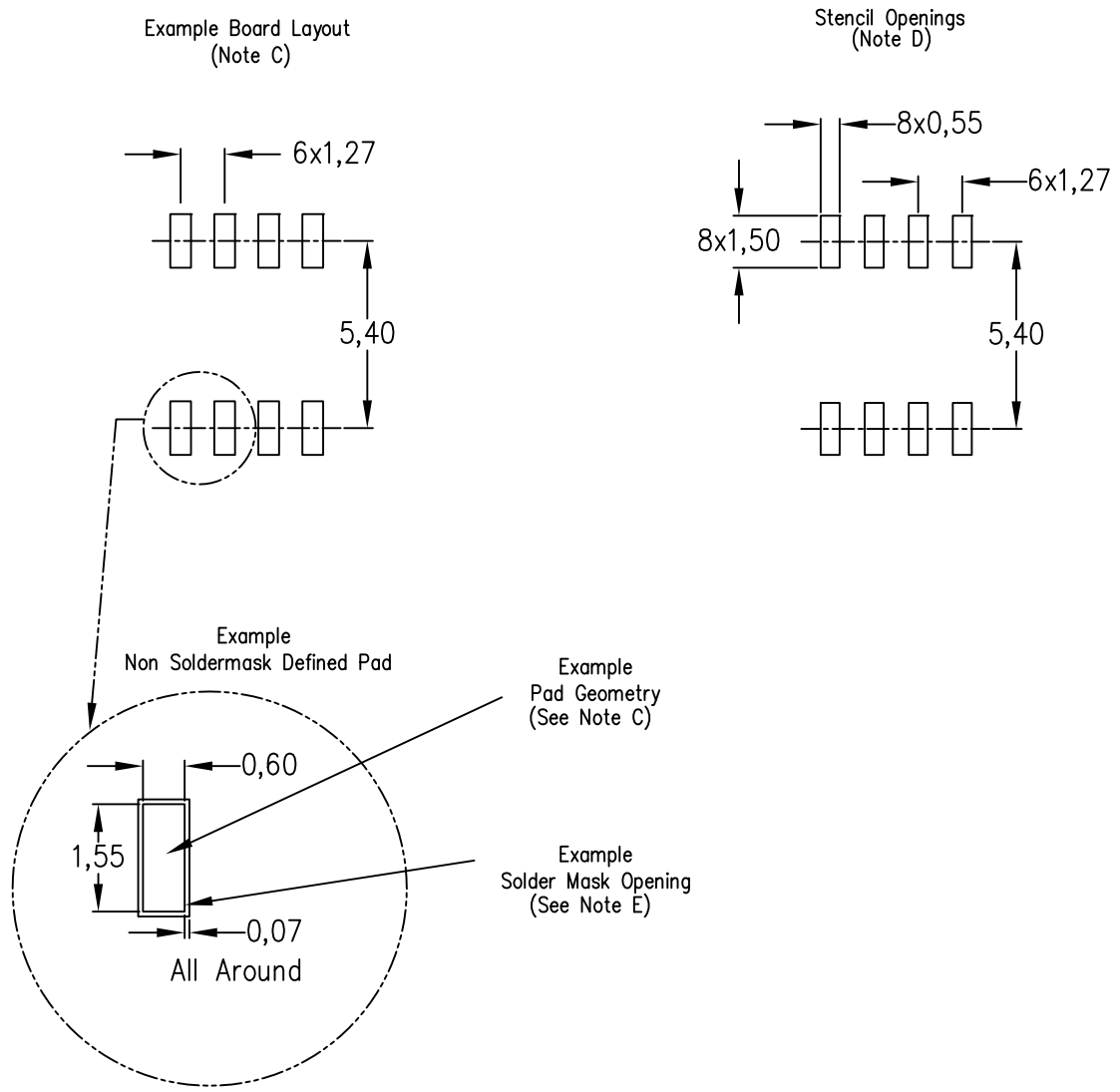
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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