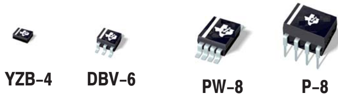


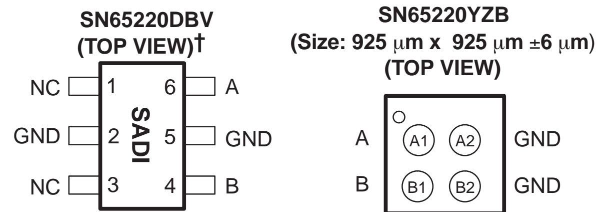
USB PORT TRANSIENT SUPPRESSORS

FEATURES

- **Design to Protect Submicron 3-V or 5-V Circuits from Noise Transients**
- **Port ESD Protection Capability Exceeds:**
  - **15-kV Human Body Model**
  - **2-kV Machine Model**
- **Available in a WCSP Chip-Scale Package**
- **Stand-Off Voltage . . . 6 V Min**
- **Low Current Leakage . . . 1 µA Max at 6 V**
- **Low Capacitance . . . 35 pF Typical**

APPLICATIONS

- **USB Full−Speed Host, Hub, or Peripheral Ports**



NC – No internal connection
†When read horizontally, Pin 1 is the bottom left pin.

DESCRIPTION

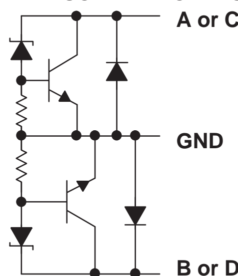
The SN65220 is a single transient voltage suppressor and the SN65240 and SN75240 are dual transient voltage suppressors designed to provide electrical noise transient protection to Universal Serial Bus (USB) full−speed ports. Note that the input capacitance of the device makes it unsuitable for high-speed USB 2.0 applications.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the USB transceiver and/or the USB ASIC if they are of sufficient magnitude and duration.

USB ports are typically implemented in 3-V or 5-V digital CMOS with very limited ESD protection. The SN65220, SN65240, and SN75240 can significantly increase the port ESD protection level and reduce the risk of damage to the circuits of the USB port.

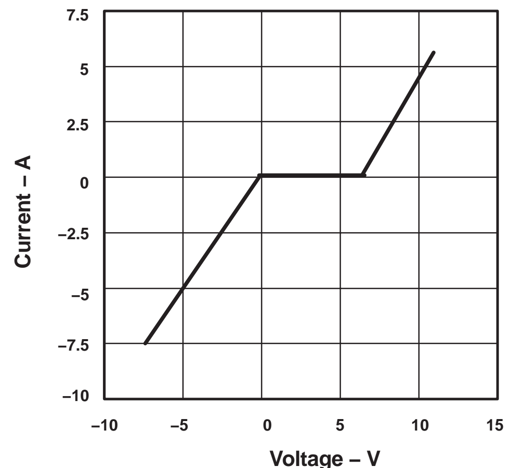
The IEC1000-4-2 ESD performance of the SN65220, SN65240, and SN75240 is measured at the system level. Therefore, system design impacts the results of these tests. A high compliance level may be attained with proper board design and layout.

EQUIVALENT SCHEMATIC DIAGRAM



(One Suppressor Shown)

NOTE: All GND terminals should be connected to ground.



NOTE A: Typical current versus voltage curve was derived using the IEC 1.2/50-µs surge waveform.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

IEC1000-4-2 COMPLIANCE LEVEL

IEC1000-4-2 COMPLIANCE LEVEL	MAXIMUM TEST VOLTAGE	
	CONTACT DISCHARGE (kV)	AIR DISCHARGE (kV)
1	2	2
2	4	4
3	6	8
4	8	15

PACKAGE/ORDERING INFORMATION

PRODUCT	SUPRESSORS	T_A	PACKAGE	PACKAGE DESIGNATOR	MARKED AS	ORDER NUMBER
SN65220	1	−40°C to 85°C	WCSP−4	YZB	NWP or 65220	SN65220YZBR (Reel)
						SN65220YZBT (Mini Reel)
			SOT23−6	DBV	SADI	SN65220DBVR (Reel)
						SN65220DBVT (Mini Reel)
SN65240	2	−40°C to 85°C	DIP−8	P	A65240	SN65240P (Rail)
			TSSOP−8	PW		SN65240PW (Rail)
						SN65240PWR (Reel)
SN75240	2	0°C to 70°C	DIP−8	P	A75240	SN75240P (Rail)
			TSSOP−8	PW		SN75240PW (Rail)
						SN75240PWR (Reel)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNIT
Continuous power dissipation	See Dissipation Rating Table
Electrostatic discharge	15 kV(2), 2 kV(3)
Peak power dissipation, $P_{D(peak)}$	60 W
Peak forward surge current, I_{FSM}	3 A
Peak reverse surge current, I_{RSM}	−9 A
Storage temperature range, T_{stg}	−65°C to 150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Human Body Model – Tested in accordance with JEDEC Standard 22, Test Method A114−A.

(3) Charged Device Model – Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	385 mW	3.1 mW/°C	246 mW	200 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW
PW	520 mW	4.2 mW/°C	331 mW	268 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

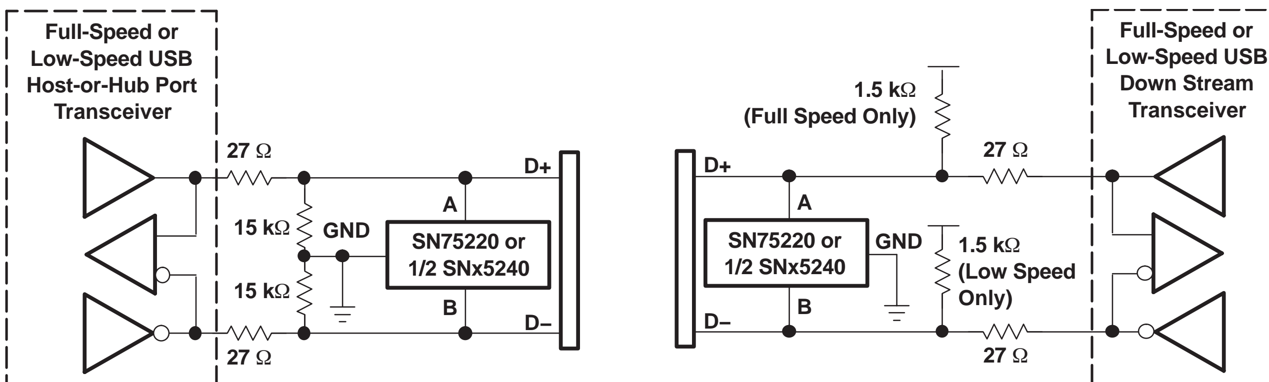
recommended operating conditions

		MIN	MAX	UNIT
Operating free-air temperature, T_A	SN75240	0	70	°C
	SN65220, SN65240	–40	85	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{lkg}	Leakage current	V_I = 6 V at A, B, C, or D terminals			1	µA
$V_{(BR)}$	Breakdown voltage	V_I = 1 mA at A, B, C, or D terminals	6.5	7	8	V
C_{IN}	Input capacitance to ground	V_I = 0.4 sin (4E6πt) + 0.5 V		35		pF

APPLICATION INFORMATION



PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65220DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65220DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65220DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65220DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65220YZBR	ACTIVE	DSBGA	YZB	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
SN65220YZBT	ACTIVE	DSBGA	YZB	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
SN65240P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65240PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65240PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65240PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65240PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65240PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75240P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75240PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75240PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75240PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75240PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
SN75240PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75240PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN65220 :

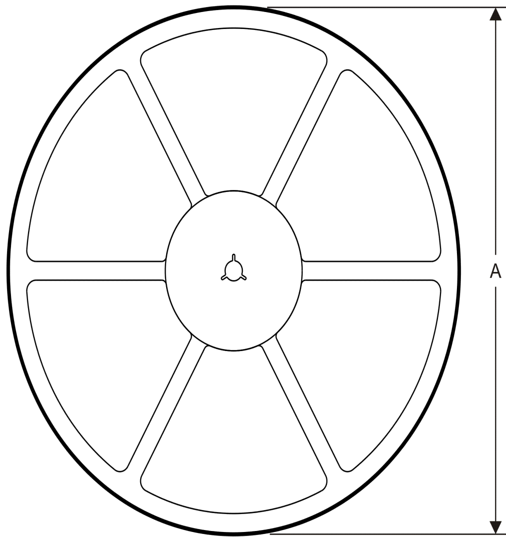
- Automotive: SN65220-Q1

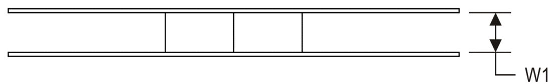
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

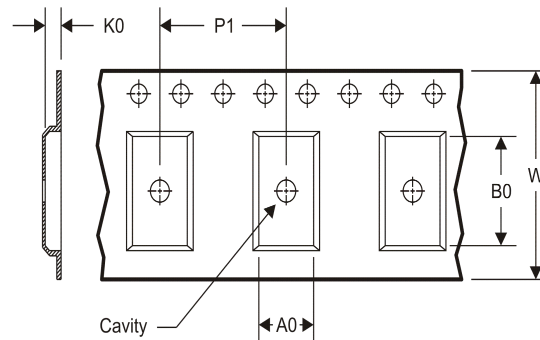
TAPE AND REEL INFORMATION

REEL DIMENSIONS





TAPE DIMENSIONS



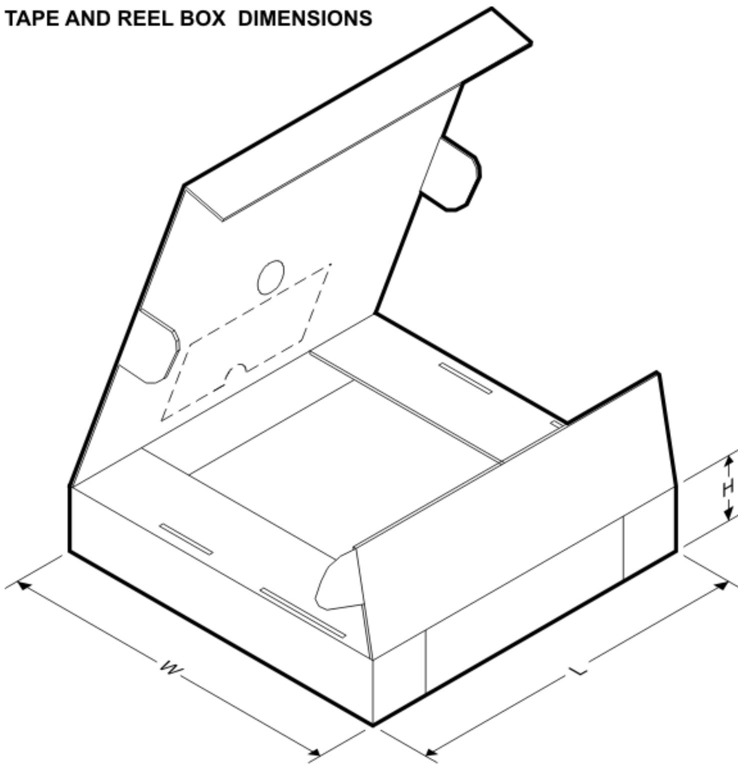
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65220DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
SN65220DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
SN65220YZBR	DSBGA	YZB	4	3000	178.0	8.4	1.06	1.06	0.81	4.0	8.0	Q1
SN65220YZBT	DSBGA	YZB	4	250	178.0	8.4	1.06	1.06	0.81	4.0	8.0	Q1
SN65240PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN75240PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

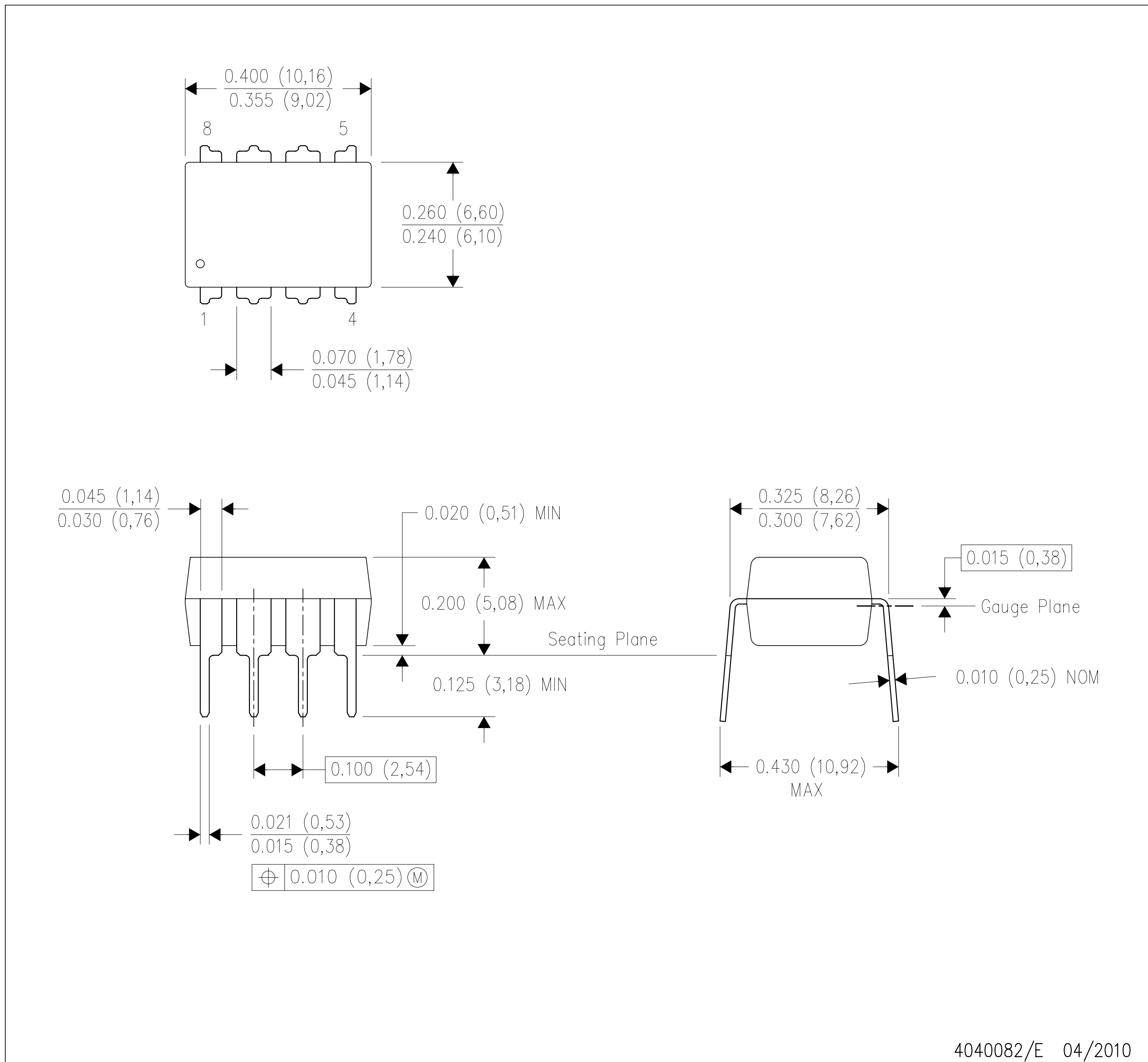
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

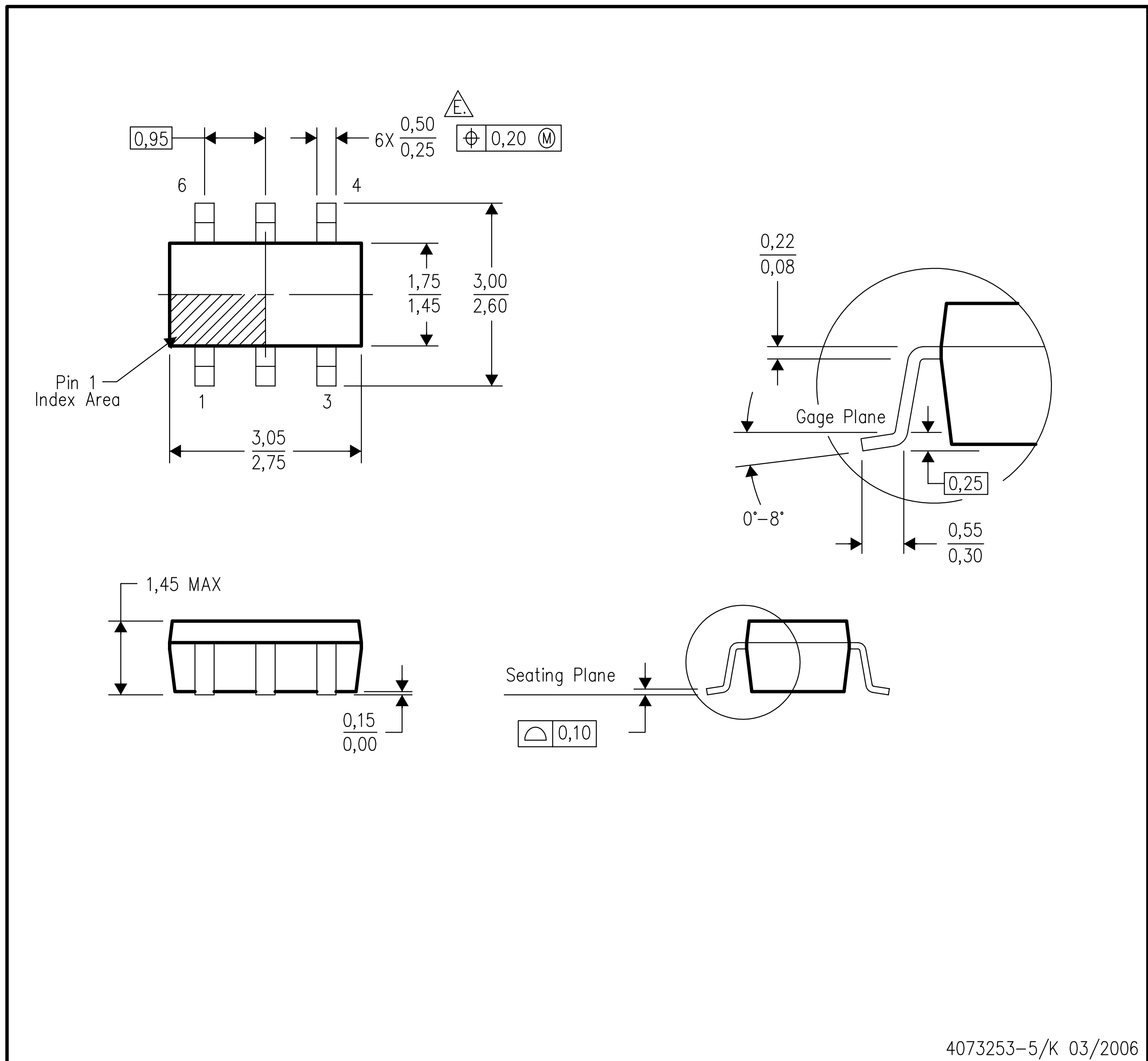
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65220DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
SN65220DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
SN65220YZBR	DSBGA	YZB	4	3000	217.0	193.0	35.0
SN65220YZBT	DSBGA	YZB	4	250	217.0	193.0	35.0
SN65240PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
SN75240PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



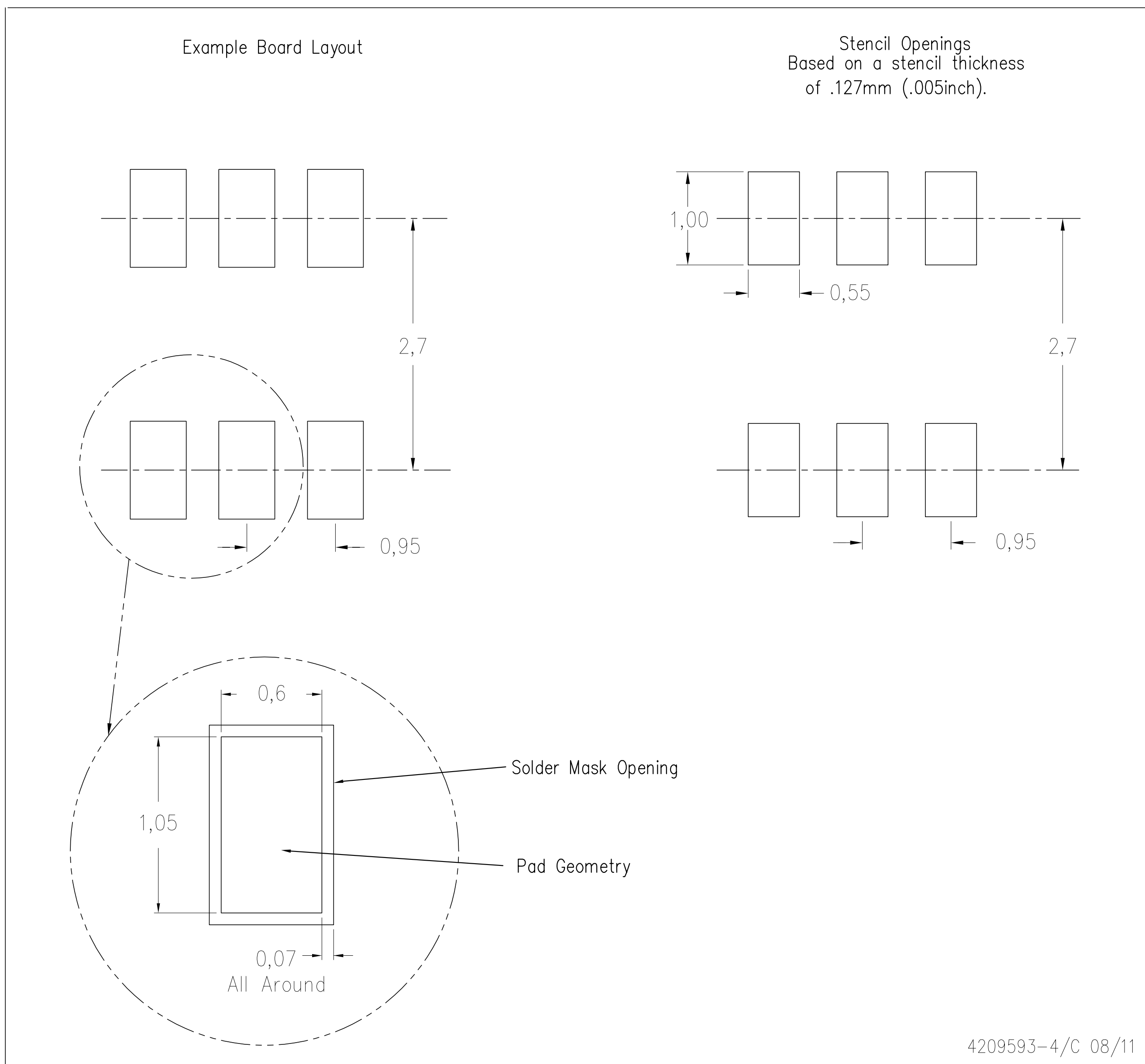
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

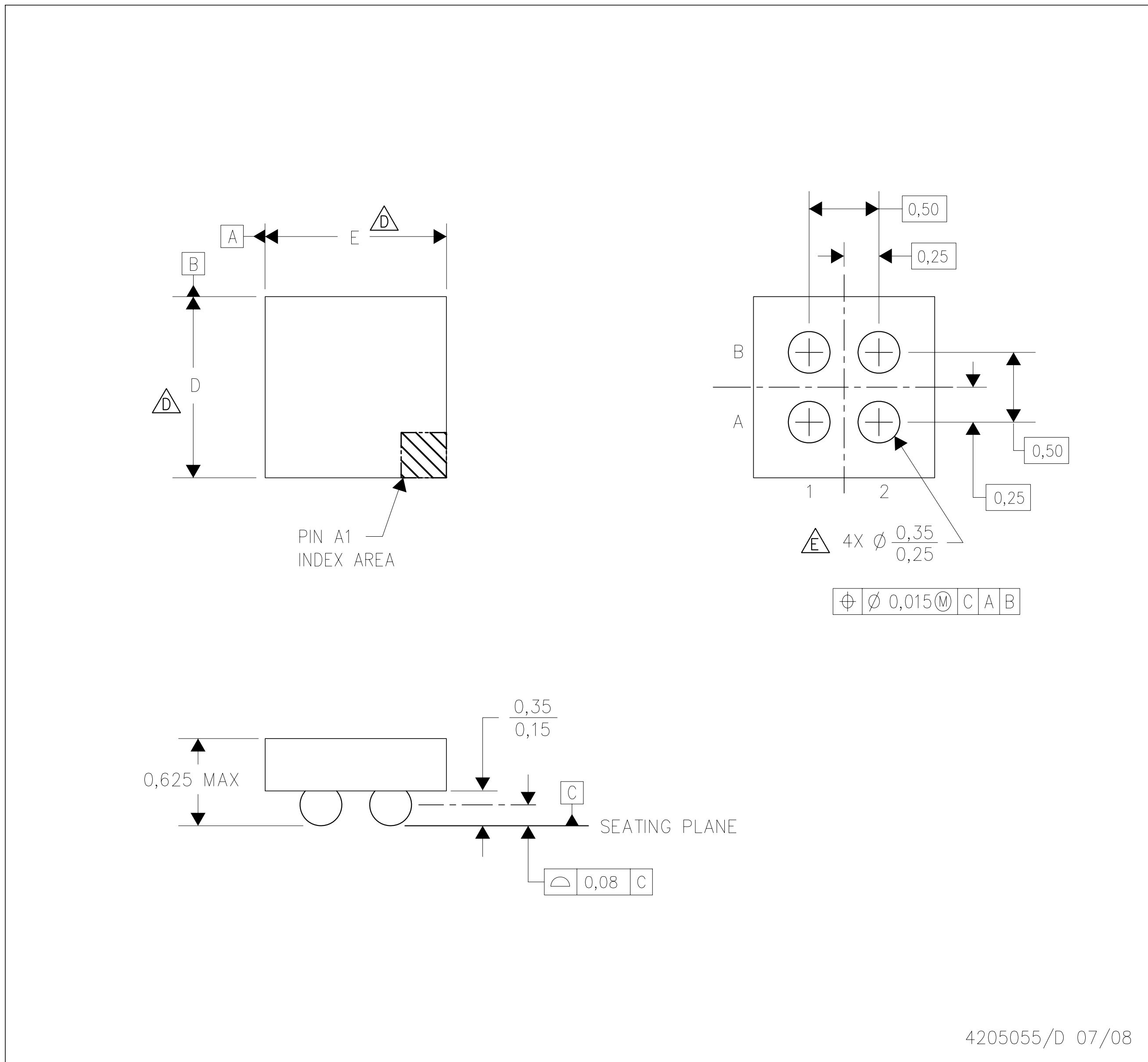
PW (R-PDSO-G8) PLASTIC SMALL OUTLINE

0,65 | 8 | 5 | 0,30 / 0,19 | ⌖ 0,10 Ⓜ | D 4,50 / 4,30 | 6,60 / 6,20 | 1 | 4 | 3,10 / 2,90 C | 0,15 NOM | Gage Plane | 0,25 | 0°–8° | 0,75 / 0,50 | 1,20 MAX | 0,15 / 0,05 | Seating Plane | ⌓ 0,10

4040064-2/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

YZB (S-XBGA-N4) DIE-SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZB package can have dimension D ranging from 0.94 to 1.65 mm and dimension E ranging from 0.94 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
F. This package contains lead-free balls. Refer to YEB (Drawing #4204178) for tin-lead (SnPb) balls.

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