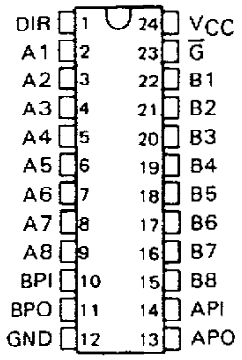
SN54HCT664, SN54HCT665, SN74HCT664, SN74HCT665
OCTAL BUS TRANSCEIVERS WITH PARITY

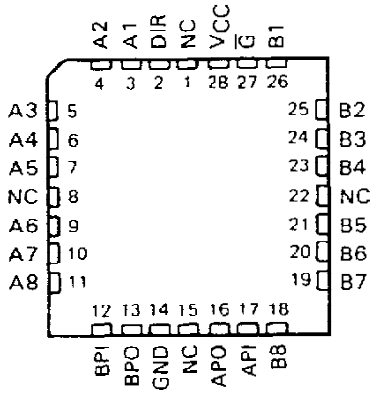
D2839, MARCH 1984—REVISED SEPTEMBER 1987

- Inputs are TTL-Voltage Compatible
- Bus Transceivers with Inverting Outputs ('HCT664) or True Outputs ('HCT665)
- Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HCT664, SN54HCT665 . . . JT PACKAGE
SN74HCT664, SN74HCT665 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HCT664, SN54HCT665 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input, $\overline{G}$, can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry. For further information, see the Typical Application Data on the 'HC664, and 'HC665 data sheet.

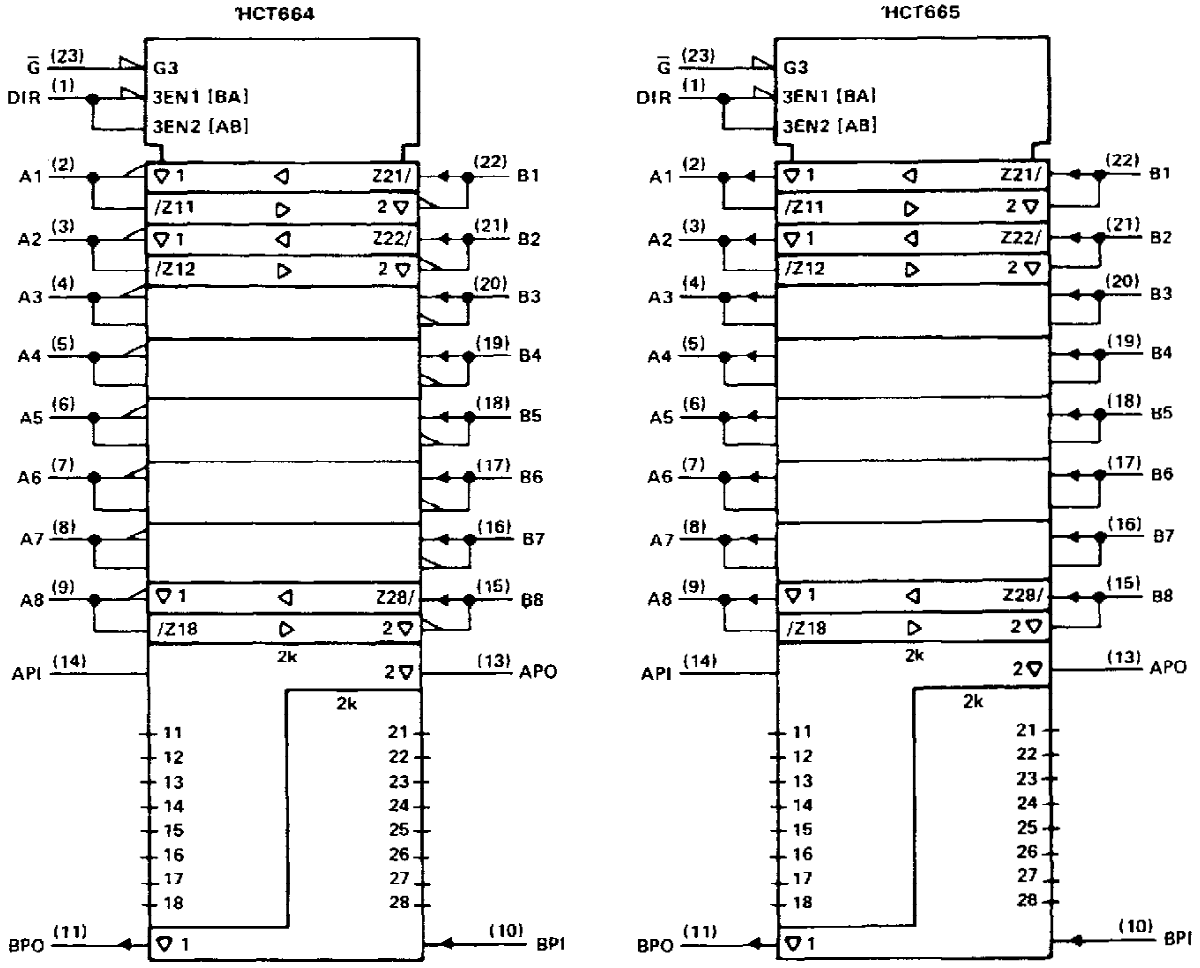
The input threshold voltages on these devices are adjusted to be TTL compatible, allowing direct interface to TTL levels on the bus or to memories with TTL output voltage levels.

The SN54HCT664 and SN54HCT665 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT664 and SN74HCT665 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

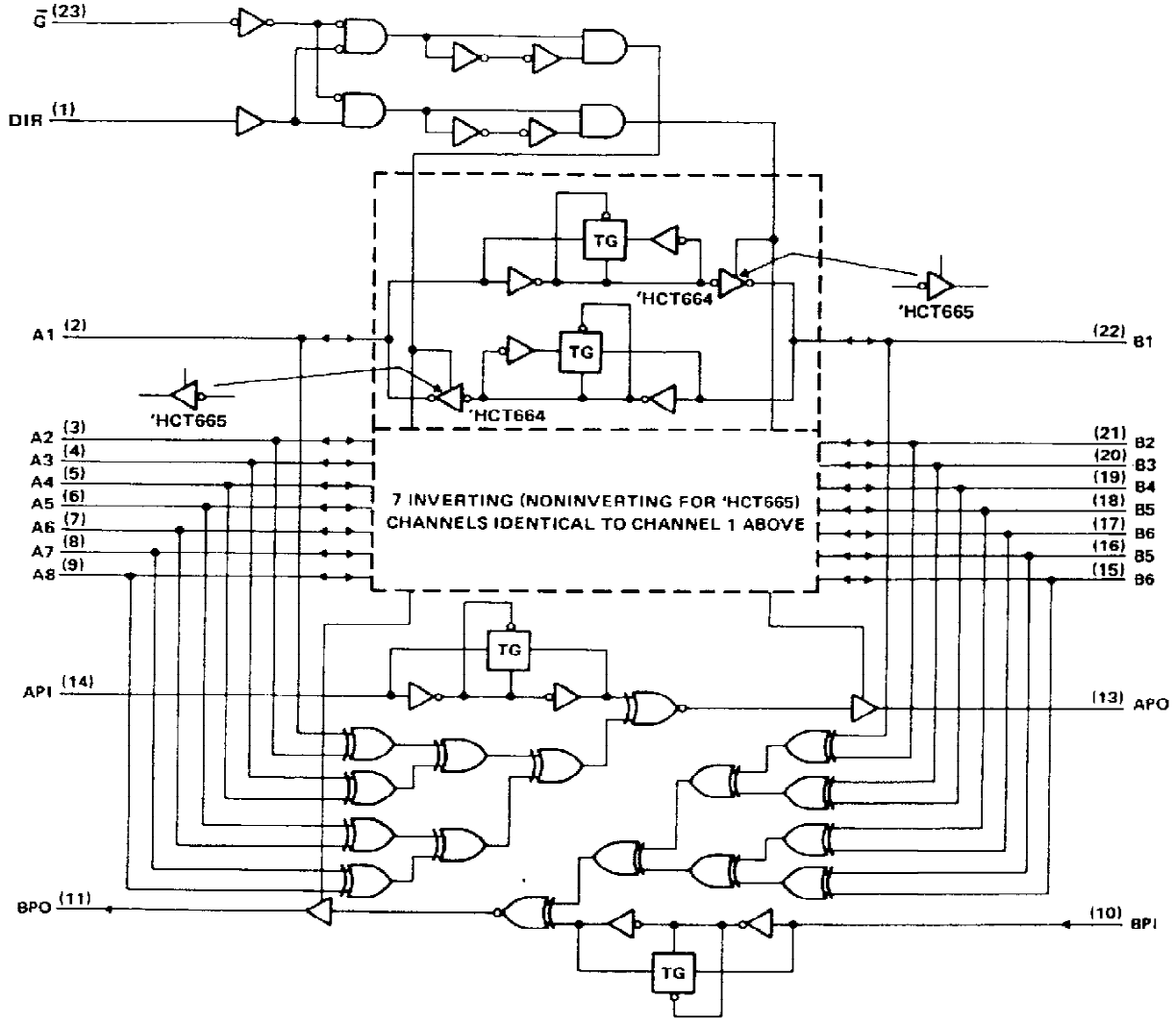
CONTROL INPUTS		NUMBER OF HIGH INPUTS ON	NUMBER OF HIGH INPUTS ON	OUTPUTS		OPERATION	
$\overline{G}$	DIR	B BUS AND BPI	A BUS AND API	APO	BPO	'HCT664	'HCT665
L	L	X	0, 2, 4, 6, 8	Z	H	$\overline{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
L	H	0, 2, 4, 6, 8	X	H	Z	$\overline{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	X	X	X	Z	Z	Isolation	Isolation

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT664 SN54HCT665			SN74HCT664 SN74HCT665			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT664 SN54HCT665		SN74HCT664 SN74HCT665		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i§		4.5 to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.
§ This parameter, C_i, does not apply to I/O ports.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT664		SN74HCT664		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		15	30		45		38	ns
			5.5 V		13	27		41		34	
t_{pd}	A or B	APO or BPO	4.5 V		23	46		69		58	ns
			5.5 V		20	41		62		52	
t_{pd}	API or BPI	APO or BPO	4.5 V		15	31		47		39	ns
			5.5 V		14	28		42		35	
t_{en}	$\overline{G}$	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{dis}	$\overline{G}$	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{en}	DIR	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{dis}	DIR	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_t		Any	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	62 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT664		SN74HCT664		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		23	47		71		59	ns
			5.5 V		21	42		64		53	
t_{pd}	A or B	APO or BPO	4.5 V		31	63		95		79	ns
			5.5 V		28	56		85		71	
t_{pd}	API or BPI	APO or BPO	4.5 V		24	48		73		60	ns
			5.5 V		21	43		65		54	
t_{en}	$\overline{G}$	A or B	4.5 V		34	68		103		85	ns
			5.5 V		30	61		92		77	
t_{en}	DIR	A or B	4.5 V		34	68		103		85	ns
			5.5 V		30	61		92		77	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

For typical application data and a description of the unique input structure, see the 'HC664 series data sheet.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT665		SN74HCT665		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		14	28		61		50	ns
			5.5 V		12	25		42		35	
t_{pd}	A or B	APO or BPO	4.5 V		23	46		69		58	ns
			5.5 V		20	41		62		52	
t_{pd}	API or BPI	APO or BPO	4.5 V		15	31		47		39	ns
			5.5 V		14	28		42		35	
t_{en}	$\overline{G}$	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{dis}	$\overline{G}$	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{en}	DIR	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{dis}	DIR	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_t		Any	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	62 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT665		SN74HCT665		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		22	45		84		69	ns
			5.5 V		20	40		68		56	
t_{pd}	A or B	APO or BPO	4.5 V		31	63		95		79	ns
			5.5 V		28	56		85		71	
t_{pd}	API or BPI	APO or BPO	4.5 V		24	48		73		60	ns
			5.5 V		21	43		65		54	
t_{en}	$\overline{G}$	A or B	4.5 V		34	68		103		85	ns
			5.5 V		30	61		92		77	
t_{en}	DIR	A or B	4.5 V		34	68		103		85	ns
			5.5 V		30	61		92		77	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

For typical application data and a description of the unique input structure, see the 'HC664 series data sheet.

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.