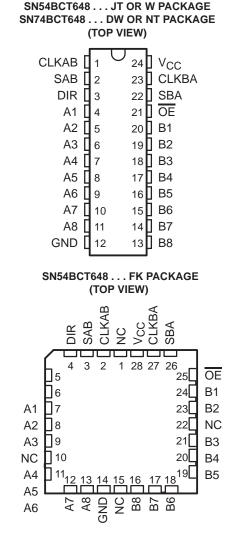
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- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Power-Up High-Impedance Mode
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPS (JT, NT)

description

These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental busmanagement functions that can be performed with the 'BCT648.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select control (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when \overline{OE} is active (low). In the isolation mode (\overline{OE} high), A data may be stored in the other register.



NC - No internal connection

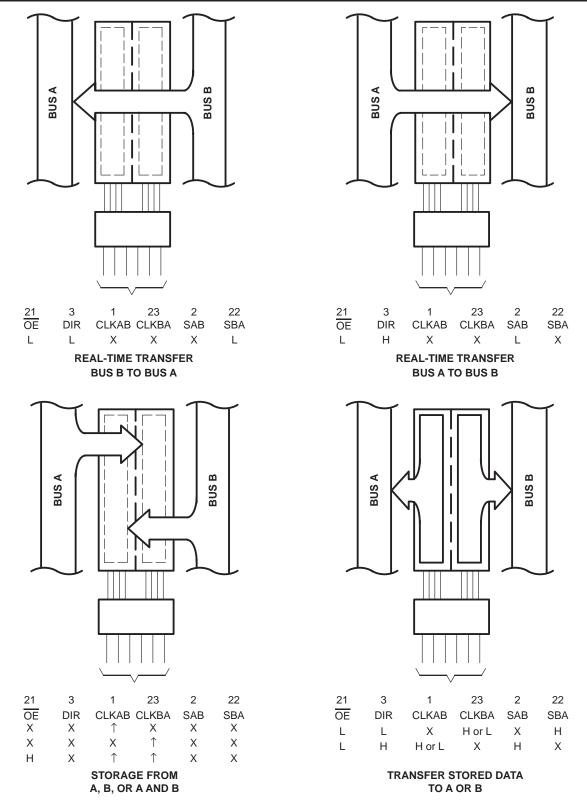
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54BCT648 is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74BCT648 is characterized for operation from 0°C to 70°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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Pin numbers shown are for the DW, JT, NT, and W packages.

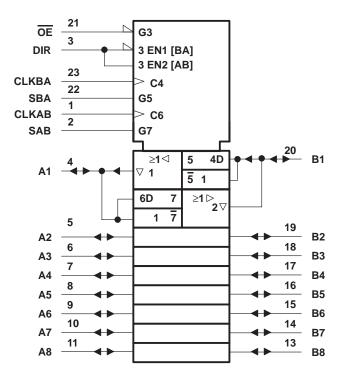


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FUNCTION TABLE								
		INP	UTS			DAT	A I/O	
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8 B1 THRU B8		OPERATION OR FUNCTION
Х	Х	\uparrow	Х	Х	Х	Input	Unspecified [†]	Store A, B unspecified [†]
х	Х	Х	\uparrow	Х	Х	Unspecified [†]	Input	Store B, A unspecified [†]
Н	Х	\uparrow	\uparrow	Х	Х	Input	Input	Store A and B data
н	Х	H or L	H or L	Х	Х	Input	Input	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A Bus
L	L	Х	H or L	Х	Н	Output	Input	Stored \overline{B} data to A Bus
L	Н	Х	Х	L	Х	Input	Output	Real-time \overline{A} data to B Bus
L	Н	H or L	Х	Н	Х	Input	Output	Stored \overline{A} data to B Bus

[†] The data output functions may be enabled or disabled by various signals at the $\overline{\text{OE}}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol[‡]

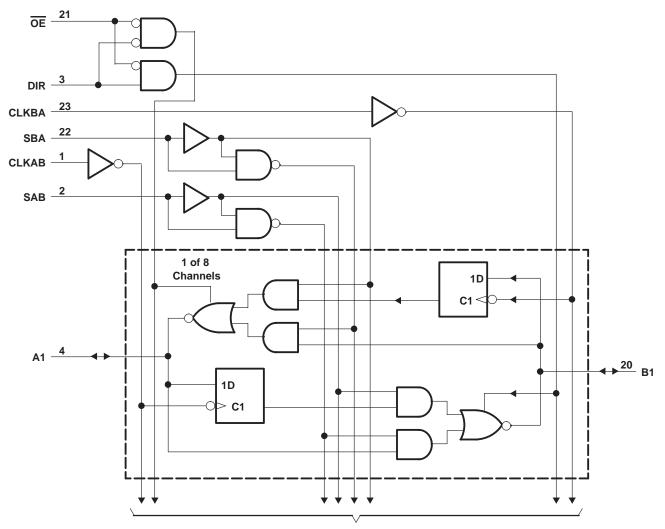


[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, NT, and W packages.



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logic diagram (positive logic)



To Seven Other Channels

Pin numbers shown are for the DW, JT, NT, and W packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Operating free-air temperature range:	e 1)) (see Note 1) ne disabled or power-off state, V _O ne high state, V _O SN54BCT648 SN74BCT648 SN54BCT648	$\begin{array}{cccc} & - \ 0.5 \ V \ to \ 5.5 \ V \\ & - \ 0.5 \ V \ to \ 7 \ V \\ & - \ 0.5 \ V \ to \ 5.5 \ V \\ & - \ 0.5 \ V \ to \ 5.5 \ V \\ & - \ 0.5 \ V \ to \ V_{CC} \\ & 96 \ mA \\ & 128 \ mA \\ & - \ 55^\circ C \ to \ 125^\circ C \end{array}$
Storage temperature range	SN74BCT648	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54BCT648			SN			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Iк	Input clamp current			-18			-18	mA
ЮН	High-level output current			-12			-15	mA
IOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				SN	54BCT6	48	SN			
		TEST CONDITIONS			TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA			-1.2			-1.2	V
			$I_{OH} = -3 \text{ mA}$	2.4	3.3		2.4	3.3		
VOH		$V_{CC} = 4.5 V$	$I_{OH} = -12 \text{ mA}$	2	3.2					V
			I _{OH} = -15 mA				2	3.1		
Max			I _{OL} = 48 mA		0.38	0.55				V
VOL		V _{CC} = 4.5 V	I _{OL} = 64 mA					0.42	0.55	V
	A or B port					1			1	mA
1j	Control inputs	V _{CC} = 5.5 V,	V _I = 5.5 V			1			1	
†	A or B port		V 07V			70			70	
IIH‡	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μA
. +	A or B port					-0.7			-0.7	
ı _{IL} ‡	Control inputs	V _{CC} = 5.5 V,	V _I = 0.5 V			-0.7			-0.7	mA
los§	_	V _{CC} = 5.5 V,	$V_{O} = 0$	-100		-225	-100		-225	mA
ICCL	A or B port	V _{CC} = 5.5 V,	V _I = GND		42	66		42	66	mA
ІССН	A or B port	V _{CC} = 5.5 V,	V _I = 4.5 V		8	13		8	13	mA
ICCZ	A or B port	V _{CC} = 5.5 V,	VI = GND		10	16	_	10	16	mA
Ci	Control inputs	V _{CC} = 5 V,	V _I = 2.5 V or 0.5 V		6			6		pF
Cio	A or B port	V _{CC} = 5 V,	$V_{O} = 2.5 \text{ V or } 0.5 \text{ V}$		12			12		pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. [‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current. § Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 5 V, T _A = 25°C		SN54BCT648		SN74BCT648	
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	67	0	67	0	67	MHz
	Dube duration	CLK high	7.5		4.3		7.5		
tw	Pulse duration CLK low				7.5		7.5		ns
t _{su}	Setup time, A or B before CLK [↑]		6		6		6		ns
t _h	Hold time, A or B after $CLK\uparrow$		1		1		1		ns



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Note 2)

PARAMETER	FROM	TO		V _{CC} = 5 V, T _A = 25°C		SN54BCT648		SN74BCT648		UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			67	110		67		67		MHz
^t PLH		A an D	3.7	7.4	10.3	3.7	13.4	3.7	12.1	
^t PHL	CLKBA or CLKAB	A or B	4.3	7.8	10.6	4.3	13.2	4.3	12.5	ns
^t PLH	A or B	B or A	3.8	7.4	9.9	3.8	12.8	3.8	12.2	20
^t PHL		BOIA	3.3	6.5	8.9	3.3	11.2	3.3	10.1	ns
^t PLH	SAB or SBA [†] (with A or B high)	A or B	3.3	6.2	8.4	3.3	10.7	3.3	9.7	ns
^t PHL			5.3	9.6	12.6	5.3	16.5	5.3	15.5	
^t PLH	SBA or SAB [†]	A or B	4.6	8.8	11.7	4.6	16.5	4.6	14.3	ns
^t PHL	(with A or B low)		4.9	8.4	11.1	4.9	13.8	4.9	13	
^t PZH	OE	A co D	4.5	8.4	11	4.5	14.4	4.5	13.5	
^t PZL	UE	A or B	4.9	9.2	12.2	4.9	16	4.9	15	ns
^t PHZ	OE	A se D	4	7.3	9.7	4	12	4	11.2	
^t PLZ	UE	A or B	3.5	6.6	9.3	3.5	11.6	3.5	10.5	ns
^t PZH	DID	A	3.1	7.4	11	3.1	14.1	3.1	13.4	
^t PZL	DIR	A or B	3.8	8.3	12.2	3.8	15.5	3.8	14.7	ns
^t PHZ	DIR	A or B	4.3	8.3	11.6	3.5	14.3	4.3	13.9	ns
^t PLZ		AUD	2.7	6.7	9.9	2.7	12.8	2.7	11.9	115

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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