NIPPON PRECISION CIRCUITS INC.

SM6453AB

3-wire Serial Data Volume Control for Headphone Amplifier IC

OVERVIEW

The SM6453AB is a stereo headphone amplifier IC with built-in electronic volume controlled by 3-wire serial data. Two switchable input systems are supported. It features bass boost function, automatic gain control (AGC) function, power-down function, and beep sound input/output function, making it ideal for use in portable electronic products.

FEATURES

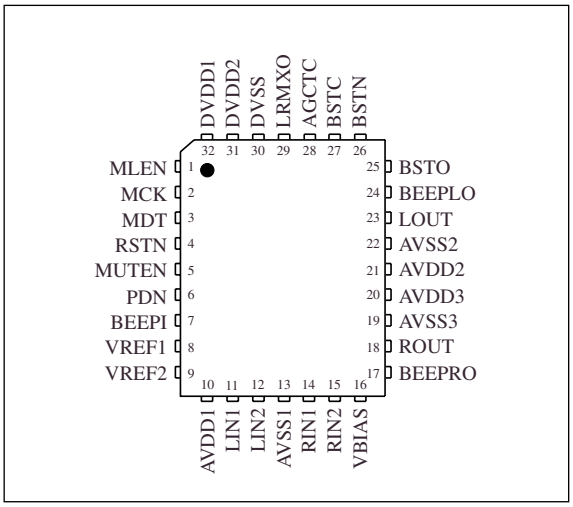
- 2 stereo system inputs, selectable 1 output system
- Headphone amplifier function
  - +12dB to -68dB output voltage gain range (G_{CNT})
  - +12dB headphone amplifier gain (G_{HPA})
- Attenuation function
  - 1.0dB step width, 81 steps, 0 to –80dB range (G_{EVR})
- Mute function
- Bass boost function (2 boost characteristics controlled by external RC network)
- Auto gain control function (AGC)
- Beep sound input/output circuit
- 26mW+26mW maximum output power (1kHz, THD + N = 10%, 16Ω load, 2.0V supply voltage)
- Power-down function
- 1.8 to 3.6V operating supply voltage range
- Low current consumption (2.3mA total, 2.4V supply voltage)
- Silicon-gate CMOS process
- 32-pin QFN package

ORDERING INFORMATION

Device	Package
SM6453AB	32-pin QFN

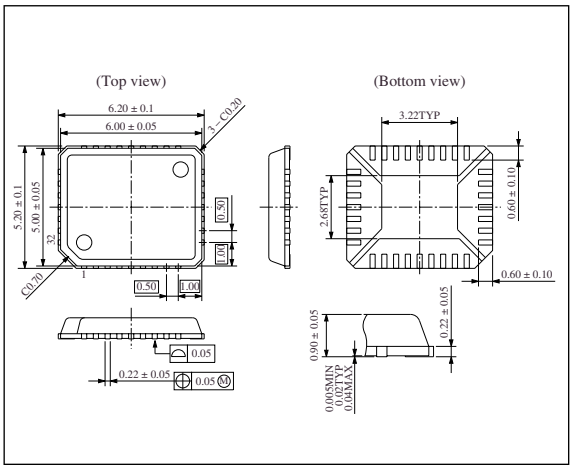
PINOUT

(Top view)



PACKAGE DIMENSIONS

(Unit: mm)



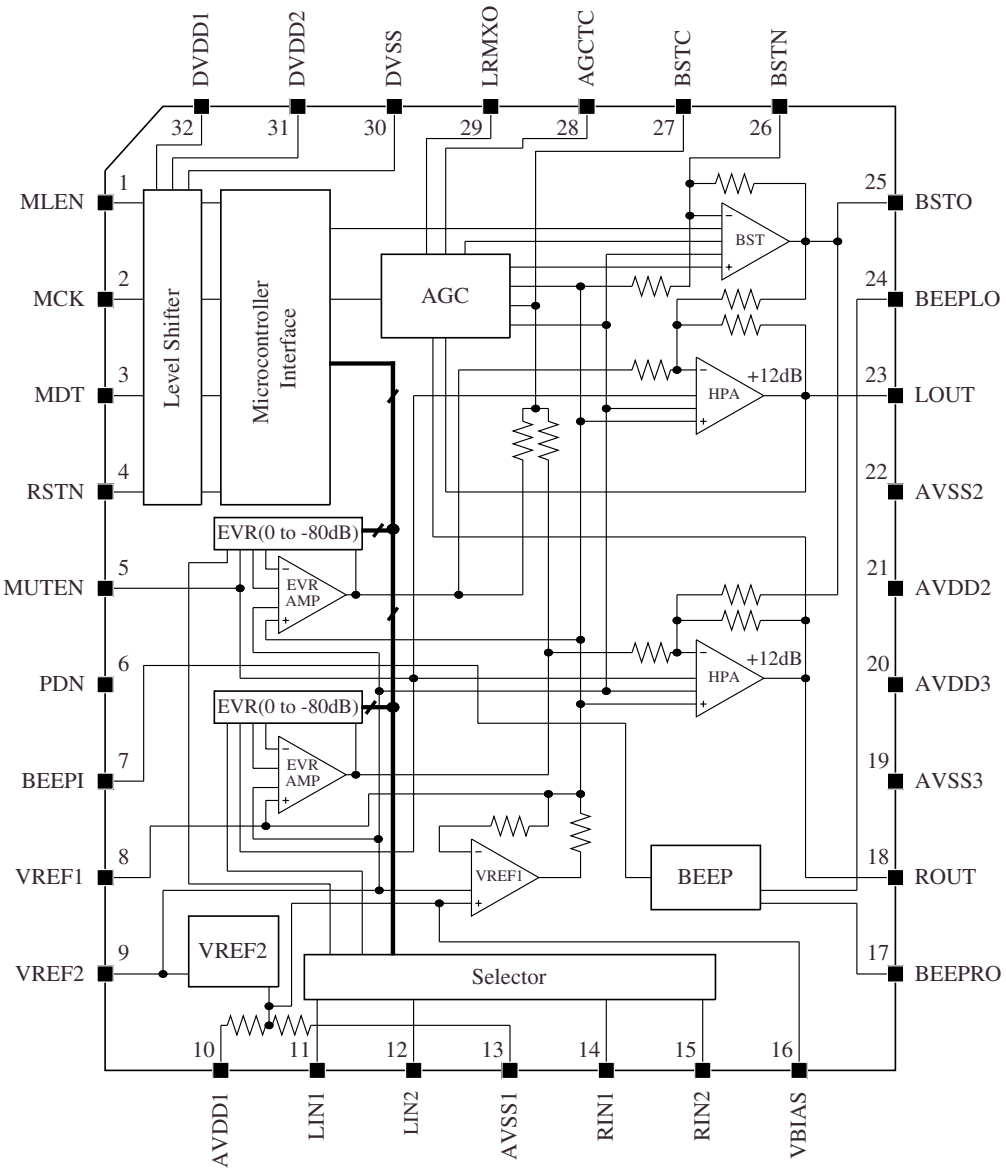
PIN DESCRIPTION

Number	Name	I/O[1]	Description	V_{DD}
1	MLEN	Ip	Microcontroller latch enable input	V_{DD2}
2	MCK	Ip	Microcontroller clock input	
3	MDT	Ip	Microcontroller data input	
4	RSTN	Ip	System reset (LOW-level reset)	
5	MUTEN	I	Mute input (LOW-level mute)	
6	PDN	I	Power-down mode select (LOW-level power-down)	
7	BEEPI	I	Beep signal input	
8	VREF1	O	Reference voltage 1	V_{DD1}
9	VREF2	O	Reference voltage 2	
10	AVDD1	–	EVR-stage analog VDD	
11	LIN1	I	Left-channel analog input 1	
12	LIN2	I	Left-channel analog input 2	
13	AVSS1	–	EVR-stage analog VSS	
14	RIN1	I	Right-channel analog input 1	
15	RIN2	I	Right-channel analog input 2	
16	VBIAS	O	EVR-stage bias voltage	
17	BEEPRO	O	Right-channel beep signal output	
18	ROUT	O	Right-channel output	
19	AVSS3	–	Headphone amplifier right-channel analog VSS	
20	AVDD3	–	Headphone amplifier right-channel analog VDD	
21	AVDD2	–	Headphone amplifier left-channel analog VDD	
22	AVSS2	–	Headphone amplifier left-channel analog VSS	
23	LOUT	O	Left-channel output	
24	BEEPLO	O	Left-channel beep signal output	
25	BSTO	O	Bass boost auxiliary output	
26	BSTN	I	Bass boost auxiliary input	
27	BSTC	O	Bass boost capacitor connection	
28	AGCTC	O	AGC time constant set capacitor connection	
29	LRMXO	O	Left and right-channel mixer detector output	
30	DVSS	–	Digital VSS	
31	DVDD2	–	Digital VDD2	
32	DVDD1	–	Digital VDD1	V_{DD2}

1. Ip = input with pull-up resistance

V_{DD1}, V_{DD2}, V_{SS} definitions
V_{DD1} = DVDD2 = AVDD1 = AVDD2 = AVDD3
V_{DD2} = DVDD1
V_{SS} = DVSS = AVSS1 = AVSS2 = AVSS3

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD1}, V_{DD2}	– 0.3 to 4.6	V
Digital system input voltage[1]	V_{IND}	V_{SS} – 0.3 to V_{DD2} + 0.3	V
Analog system input voltage[2]	V_{INA}	V_{SS} – 0.3 to V_{DD1} + 0.3	V
Storage temperature	T_{STG}	– 55 to 125	°C
Output current	I_O	100	mA
Power dissipation[3]	P_D	370	mW

1. Digital system inputs: MLEN, MDT, MCK, RSTN, MUTEN, PDN, BEEPI
2. Analog system inputs: LIN1, LIN2, RIN1, RIN2, BSTN
3. NPC specified value θ_{Ja} = 107.6°C/W
   $P_D = \{(T_{JMAX} - Ta)/\theta_{Ja}\}$ (T_{JMAX} = 125°C, Ta = 85°C)

Recommended Operating Conditions

V_{SS} = DVSS = AVSS1 = AVSS2 = AVSS3 = 0V, V_{DD1} = DVDD2 = AVDD1 = AVDD2 = AVDD3, V_{DD2} = DVDD1

Parameter	Symbol	Conditions	Unit
Supply voltage 1	V_{DD1}	1.8 to 3.6	V
Supply voltage 2	V_{DD2}	1.8 to 3.6	V
Supply voltage difference	DVDD2-AVDD1, DVDD2-AVDD2, DVDD2-AVDD3, AVDD1-AVDD2, AVDD1-AVDD3, AVDD2-AVDD3	± 0.1	V
Operating temperature	Ta	– 40 to 85	°C

DC Characteristics

AVSS1 = AVSS2 = AVSS3 = DVSS = 0V, AVDD1 = AVDD2 = AVDD3 = DVDD2 = 1.8 to 3.6V,
DVDD1 = 1.8 to 3.6V, Ta = – 40 to 85°C unless otherwise noted.

Parameter	Pins	Symbol		Condition	Rating			Unit
					min	typ	max	
Current consumption	DVDD1	I_{DDD1A}		(Note 1)	–	0.03	0.06	mA
		I_{DDD1S}		(Note 2)	–	0.2	1.0	µA
	DVDD2	I_{DDD2A}		(Note 1)	–	0.05	0.3	mA
		I_{DDD2S}		(Note 2)	–	0.2	1.0	µA
	AVDD1 + AVDD2 + AVDD3	I_{DDAA}		(Note 1)	–	2.3	3.6	mA
		I_{DDAS}		(Note 2)	–	13.0	25.0	µA
		I_{DDAM1}		(Note 3)	–	1.7	3.1	mA
		I_{DDAM2}		(Note 4)	–	0.5	–	mA
		I_{DDAT}		(Note 5)	–	7.0	10.0	mA
Input voltage 1	(*1)	H-level	V_{IH1}		0.8×DVDD1	–	–	V
		L-level	V_{IL1}		–	–	0.2×DVDD1	V
Input voltage 2	(*2)	H-level	V_{IH2}		1.2	–	–	V
		L-level	V_{IL2}		–	–	0.4	V
Input current 1	(*1)	I_{IL1}		V_{IN} = 0V	–	25	90	µA
Input current 2	(*3)	I_{IH1}		$V_{IN} = V_{DD1}$	–	280	900	µA
Input leakage current 1	(*1)	I_{IH2}		$V_{IN} = V_{DD1}$	–	–	1.0	µA
Input leakage current 2	(*2)	I_{IL2}		V_{IN} = 0V	–	–	1.0	µA
Input leakage current 3	(*2)	I_{IH3}		$V_{IN} = V_{DD1}$	–	–	1.0	µA
Input leakage current 4	(*3)	I_{IL3}		V_{IN} = 0V	–	–	1.0	µA

(Note 1) MUTEN = HIGH, PDN = HIGH, 600Ω resistor connected between VREF1 and all analog inputs (LIN1, LIN2, RIN1, RIN2), G_{EVR} = 0dB, Microcontroller clock frequency = 4MHz, data transfer from microcontroller.
(Note 2) MUTEN = LOW, PDN = LOW, 600Ω resistor connected between VREF1 and all analog inputs (LIN1, LIN2, RIN1, RIN2), G_{EVR} = 0dB, data transfer from microcontroller stopped, Pins (*1) = V_{DD2}.
(Note 3) MUTEN = LOW, PDN = HIGH, 600Ω resistor connected between VREF1 and all analog inputs (LIN1, LIN2, RIN1, RIN2), G_{EVR} = 0dB, data transfer from microcontroller stopped, Pins (*1) = V_{DD2}. Other than idling current of final stage of headphone amplifiers.
(Note 4) MUTEN = HIGH, PDN = HIGH, 600Ω resistor connected between VREF1 and all analog inputs (LIN1, LIN2, RIN1, RIN2), G_{EVR} = 0dB, data transfer from microcontroller stopped, Pins (*1) = V_{DD2}. Idling current of final stage of headphone amplifiers only.
(Note 5) MUTEN = HIGH, PDN = HIGH, reference voltage see "Measurement circuit", All analog inputs (LIN1, LIN2, RIN1, RIN2) connected reference input voltage, Bass boost = OFF, AGC = OFF, Frequency = 1kHz, P_O = 0.5mW + 0.5mW

Pin types

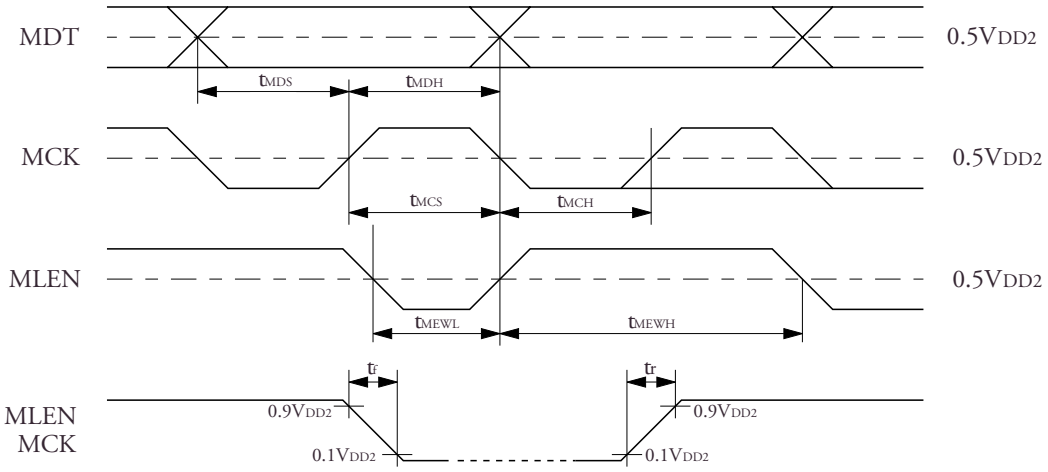
Pin types	Name
(*1)	MLEN, MDT, MCK, RSTN
(*2)	MUTEN, PDN
(*3)	BEEPI

AC Characteristics

AVDD1 = AVDD2 = AVDD3 = DVDD1 = DVDD2 = 1.8 to 3.6V, AVSS1 = AVSS2 = AVSS3 = DVSS = 0V, Ta = – 40 to 85°C unless otherwise noted.

Serial inputs (MDT, MCK, MLEN)

Parameter		Symbol	Rating			Unit
			min	typ	max	
MCK, MLEN rise time		t_r	–	–	100	ns
MCK, MLEN fall time		t_f	–	–	100	ns
MDT setup time		t_{MDS}	50	–	–	ns
MDT hold time		t_{MDH}	50	–	–	ns
MLEN	Setup time	t_{MCS}	50	–	–	ns
	Hold time	t_{MCH}	50	–	–	ns
	LOW-level pulsewidth	t_{MEWL}	50	–	–	ns
	HIGH-level pulsewidth	t_{MEWH}	50	–	–	ns



Reset input (RSTN)

Parameter	Symbol	Rating			Unit
		min	typ	max	
RSTN LOW-level pulsewidth	t_{RSTN}	100	–	–	ns

AC Analog Characteristics

V_{DD1} = V_{DD2} = 2.0V, analog input amplitude = 0.025Vrms, input frequency = 1kHz, Ta = 25°C, Measurement circuit, PDN = HIGH, MUTEN = HIGH, MDT D0 to D12 = LOW, unless otherwise noted.

Analog input characteristics (LIN1, RIN1, LIN2, RIN2)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reference input amplitude	V_{AI}	G_{EVR} = 0dB, P_O = 0.5mW + 0.5mW	0.015	0.025	0.035	Vrms
Input resistance	R_{IN}		18	23	–	kΩ
Input clipping voltage	V_{CLP}	G_{EVR} = 0dB, P_O = 26mW + 26mW	0.17	0.21	–	Vrms

Analog output characteristics (LOUT, ROUT)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Residual noise voltage	V_{NS}	G_{EVR} = 0dB, A-WTD	–	26	38	μVrms
Total harmonic distortion + noise	THD + N	P_O = 0.5mW + 0.5mW	–	0.3	1.0	%
Reference output power	P_{OREF}		0.4	0.5	0.6	mW
Reference output voltage	V_{OREF}		0.08	0.09	0.098	Vrms
Maximum output power	P_{OMAX}	G_{EVR} = 0dB, THD + N = 10%	22	26	–	mW
Maximum output voltage	V_{OMAX}	G_{EVR} = 0dB, THD + N = 10%	0.516	0.645	–	Vrms
Bass boost response	B_{BST1}	(Note 1)	+ 5.2	+ 7.2	+ 9.2	dBr
	B_{BST2}	(Note 2)	+ 12.0	+ 14.0	+ 16.0	dBr
AGC detection level	V_{AGC}	0.5V_{DD1} reference voltage output	+ 0.30	+ 0.48	+ 0.66	V
Step width	G_{STEP}		0.1	1.0	1.6	dB
Attenuation error (1kHz)	G_{ERR1}	G_{EVR} = 0dB to – 60dB	– 2.8	– 0.8	1.2	dB
	G_{ERR2}	G_{EVR} = – 61dB to – 72dB	– 2.0	0	2.0	dB
	G_{ERR3}	G_{EVR} = – 73dB to – 80dB	– 1.2	0.8	2.8	dB
Absolute attenuation (1kHz)	G_{O1}	G_O = + 12dB (G_{EVR} = 0dB)	+ 9.2	+ 11.2	+ 13.2	dB
	G_{O2}	G_O = – 8dB (G_{EVR} = – 20dB)	– 10.6	– 8.6	– 6.6	dB
	G_{O3}	G_O = – 28dB (G_{EVR} = – 40dB)	– 30.6	– 28.6	– 26.6	dB
	G_{O4}	G_O = – 48dB (G_{EVR} = – 60dB)	– 50.4	– 48.4	– 46.4	dB
	G_{O5}	G_O = – 68dB (G_{EVR} = – 80dB)	– 70.5	– 66.0	– 61.5	dB
Mute factor (1kHz)	G_{MUTE}	(Note 3)	– 100.0	– 120.0	–	dB
Channel crosstalk	CT_1	(Note 4)	– 69.0	– 75.0	–	dB
	CT_2	(Note 5)	– 29.0	– 35.0	–	dB
	CT_3	(Note 6)	– 30.0	– 36.0	–	dB
Power supply ripple rejection ratio	PSRR1	(Note 7)	83.0	93.0	–	dB
	PSRR2	(Note 8)	45.0	55.0	–	dB
	PSRR3	(Note 9)	34.0	44.0	–	dB

(Note 1) Microcontroller data bit D9 = HIGH, D10 = LOW, D11 = LOW, 55Hz frequency, V_{OREF} output
(Note 2) Microcontroller data bit D9 = HIGH, D10 = HIGH, D11 = LOW, 55Hz frequency, V_{OREF} output
(Note 3) G_{EVR} = 0dB, MDT D0 to D7 are muted, MUTEN = HIGH, V_{OREF} output
(Note 4) Microcontroller data bit D9 = LOW, D11 = LOW, G_{EVR} = 0dB, cross-channel leakage signal with V_{OREF} output and standard voltage input on one channel only
(Note 5) Microcontroller data bit D9 = HIGH, D10 = LOW, D11 = LOW, G_{EVR} = 0dB, cross-channel leakage signal with V_{OREF} output and standard voltage input on one channel only, Frequency = 10kHz
(Note 6) Microcontroller data bit D9 = HIGH, D10 = HIGH, D11 = LOW, G_{EVR} = 0dB, cross-channel leakage signal with V_{OREF} output and standard voltage input on one channel only, Frequency = 10kHz
(Note 7) PDN = LOW, MUTEN = HIGH, MDT = muted, ripple frequency = 100Hz and ripple amplitude = 0.1Vrms on AVDD1/AVDD2/AVDD3
(Note 8) PDN = HIGH, MUTEN = LOW, MDT = muted, ripple frequency = 100Hz and ripple amplitude = 0.1Vrms on AVDD1/AVDD2/AVDD3
(Note 9) PDN = HIGH, MUTEN = HIGH, MDT D0 to D12 = LOW, ripple frequency = 100Hz and ripple amplitude = 0.1Vrms on AVDD1/AVDD2/AVDD3

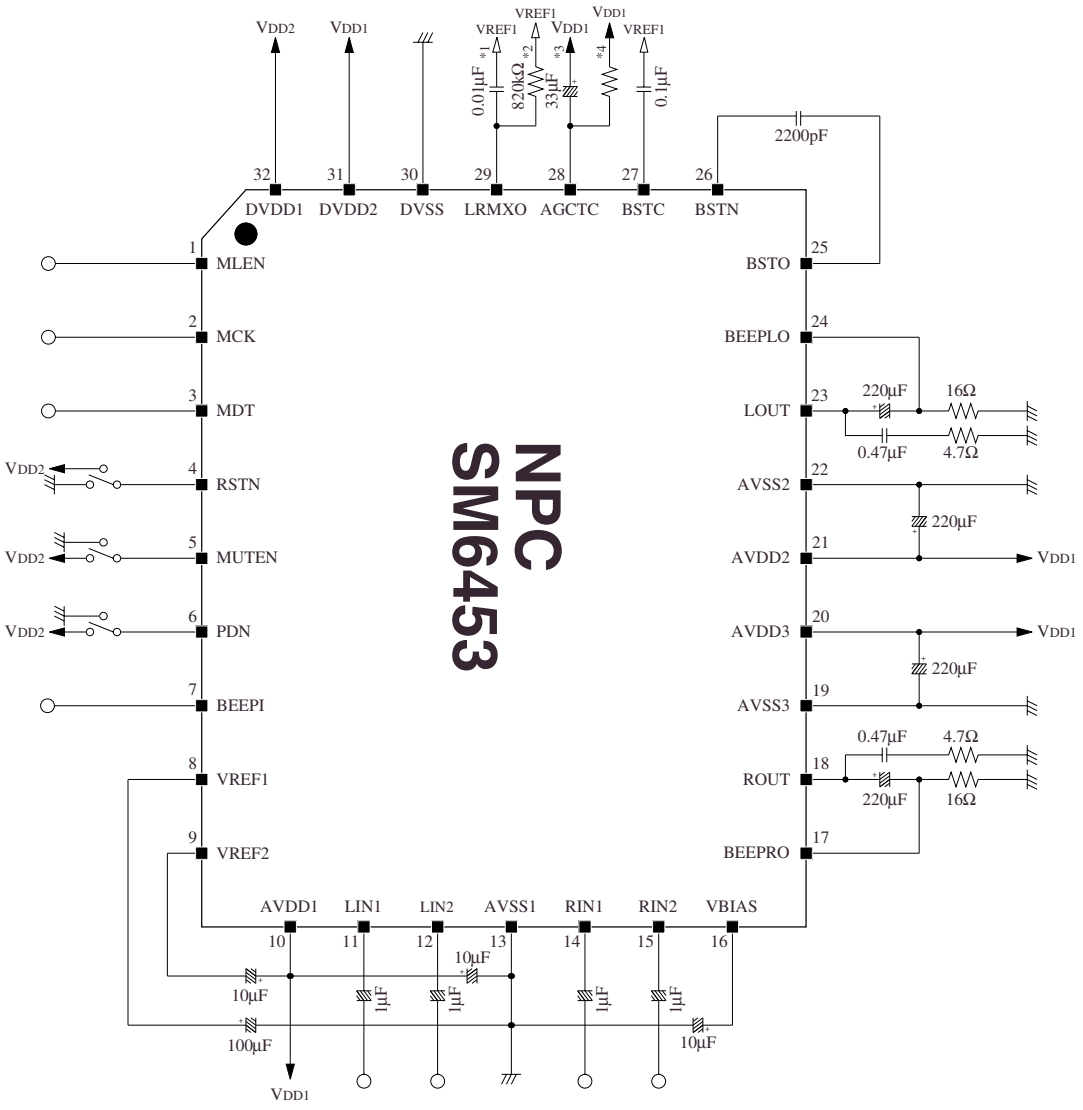
Analog output characteristics (BEEPLO, BEEPRO)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BEEP output voltage	V_{BO}	$2V_{P-O}$ amplitude, 50% duty, 400Hz rectangular wave	– 55	– 49.3	– 44	dBv

Reference voltage characteristics (VREF1, VREF2, VBIAS)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reference voltage output 1	V_{REF1}		$0.45V_{DD1}$	$0.5V_{DD1}$	$0.55V_{DD1}$	V
Reference voltage output 2	V_{REF2}		–	$V_{DD1} - 0.815$	–	V
Bias voltage output	V_{BIAS}		$0.45V_{DD1}$	$0.5V_{DD1}$	$0.55V_{DD1}$	V

Measurement circuit



*1 to *4: AGC time constant setting components. Measured with *4 open circuit.

FUNCTIONAL DESCRIPTION

Microcontroller Interface

The SM6453AB uses a serial microcontroller interface comprising MDT (data), MCK (clock), MLEN (latch enable).

Data format

The data transfer format is shown in figure 1.

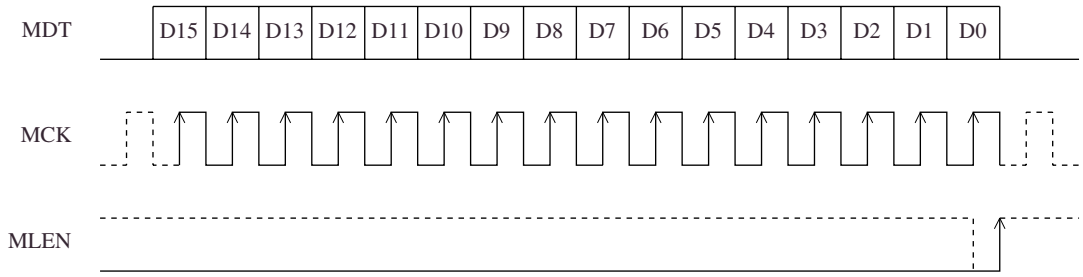


Figure 1. Microcontroller data input timing

The internal shift register shifts data on the rising edge of MCK, and the data is loaded and updated on the rising edge of MLEN (dotted lines also indicate valid data timing).
Each cycle is completed by 16 or more MCK input cycles, even if there are unused data bits.

Microcontroller data description

Definition: “L” = V_{IL1} level, “H” = V_{IH1} level

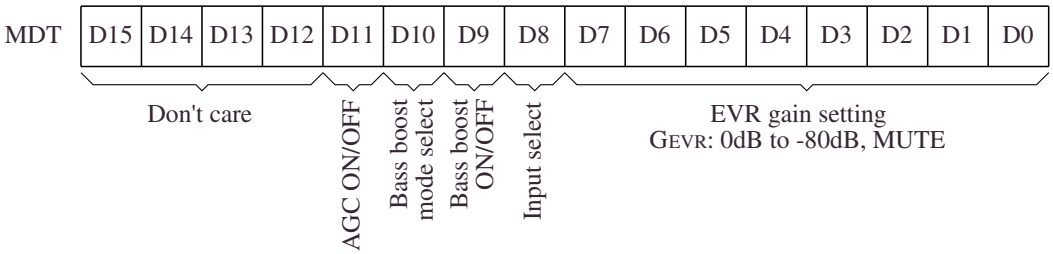


Figure 2. Microcontroller data description

- D15 to D12: Not used (don’t care) bits. Can be either “L” or “H”.
- D11: AGC bit. OFF when “L”, and ON when “H”. AGC = OFF when system reset (see “Automatic gain control function”).

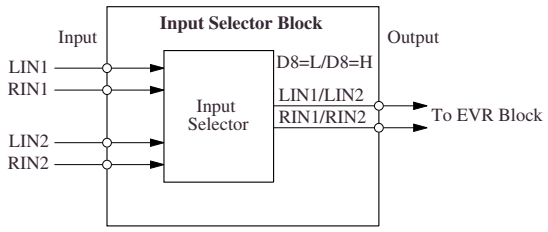
D11	AGC function
LOW	OFF
HIGH	ON

- D10, D9: Bass boost control bits. Bass boost = OFF and bass boost mode = BB1 when system reset (see “Bass boost function”).

D9	D10	Bass boost characteristics
LOW	LOW	OFF
	HIGH	
HIGH	LOW	BB1
	HIGH	BB2

- D8: Input select bit. LIN1 and RIN1 when “L”, and LIN2 and RIN2 when “H”. LIN1 and RIN1 input when system reset.

D8	Selected inputs
LOW	LIN1, RIN1
HIGH	LIN2, RIN2



■ D7 to D0: EVR gain control bits. MUTE when system reset.

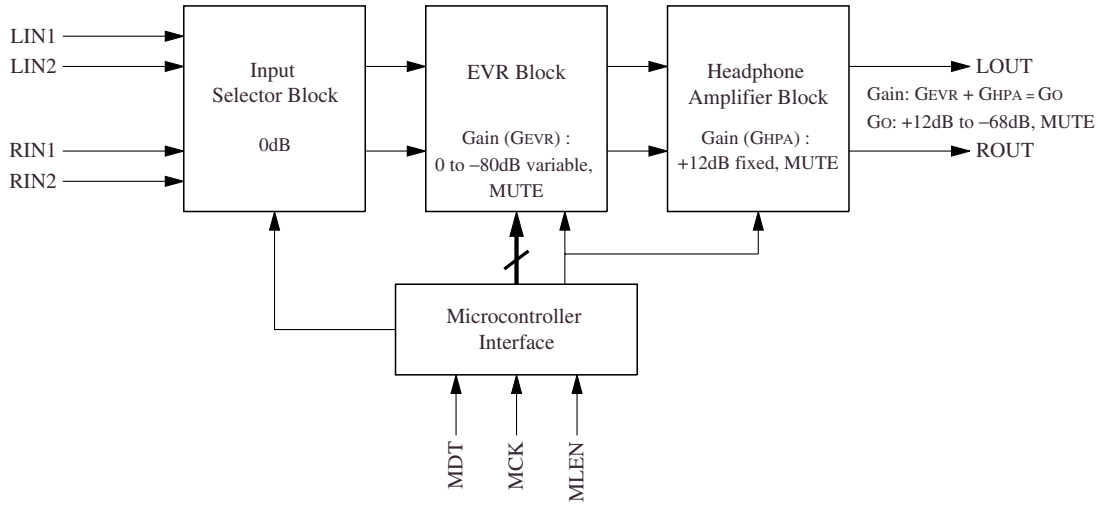


Figure 3. Electronic volume gain (G_{EVR}) setting and output voltage gain (G_O)

EVR gain (G_{EVR})	LOUT, ROUT gain (G_O)	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0dB	+ 12dB	L	L	L	L	L	L	L	L	00
– 1dB	+ 11dB	L	L	L	L	L	L	L	H	01
– 2dB	+ 10dB	L	L	L	L	L	L	H	L	02
:	:	:	:	:	:	:	:	:	:	:
– 15dB	– 3dB	L	L	L	L	H	H	H	H	0F
– 16dB	– 4dB	L	L	L	H	L	L	L	L	10
– 17dB	– 5dB	L	L	L	H	L	L	L	H	11
:	:	:	:	:	:	:	:	:	:	:
– 63dB	– 51dB	L	L	H	H	H	H	H	H	3F
– 64dB	– 52dB	L	H	L	L	L	L	L	L	40
– 65dB	– 53dB	L	H	L	L	L	L	L	H	41
:	:	:	:	:	:	:	:	:	:	:
– 79dB	– 67dB	L	H	L	L	H	H	H	H	4F
– 80dB	– 68dB	L	H	L	H	L	L	L	L	50
MUTE	MUTE	L	H	L	H	L	L	L	H	51
MUTE	MUTE	L	H	L	H	L	L	H	L	52
:	:	:	:	:	:	:	:	:	:	:
MUTE	MUTE	H	H	H	H	H	H	H	L	FE
MUTE	MUTE	H	H	H	H	H	H	H	H	FF

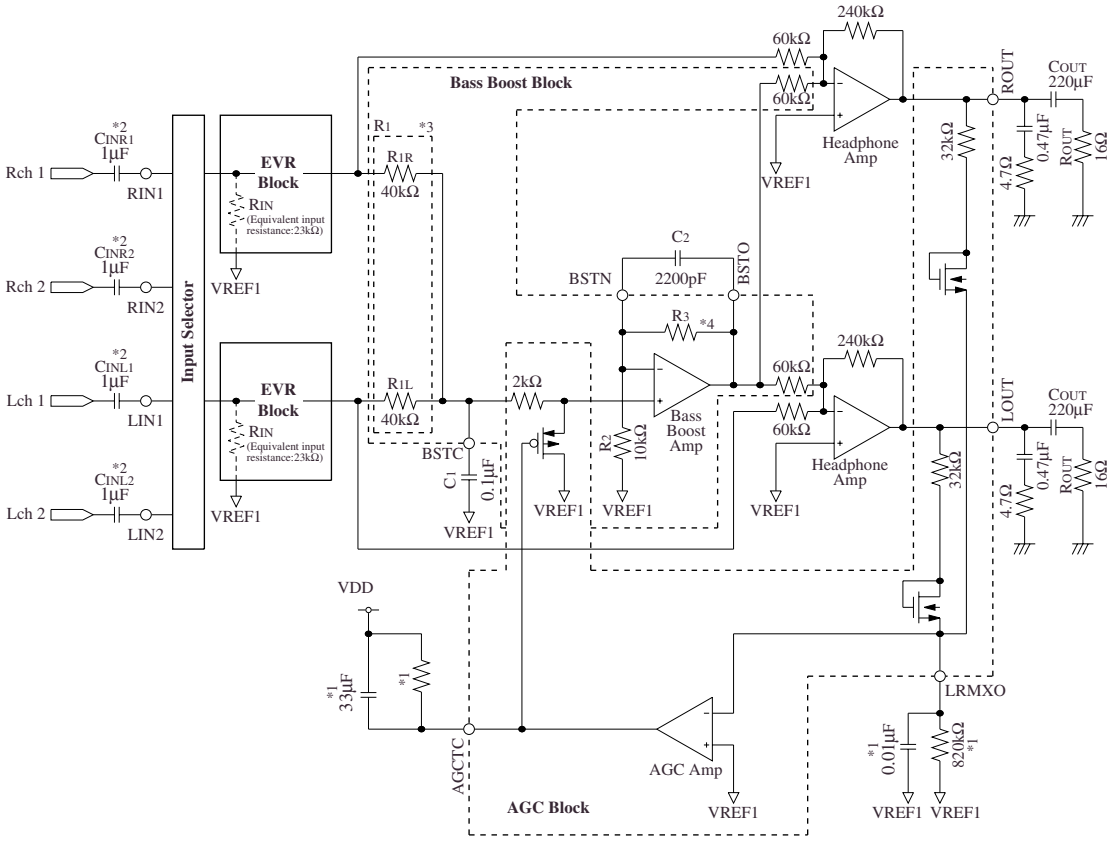
System Reset Function (RSTN)

The system is reset using a LOW-level pulse on RSTN. After the system is reset, AGC is OFF, bass boost mode is BB1, input selector is LIN1/RIN1, and LOUT/ROUT output voltage gain is muted.

AGC	Bass boost mode	Bass boost function	Input Select	EVR gain (G_{EVR})	Output gain (G_O)
OFF	BB1	OFF	LIN1, RIN1	MUTE	MUTE

Bass Boost Function with Automatic Gain Control (AGC)

Equivalent circuit



*1: From “Measurement circuit”. Adjustment AGC detection level and time constant.
*2: $C_{INR1} = C_{INL1}$, $C_{INR2} = C_{INL2} \rightarrow C_{IN}$
*3: RIN1 = LIN1 $\rightarrow R_1 = (R_{1R}/2 + R_{1L}/2) = 20k\Omega$
*4: BB1 $\rightarrow R_3 = 15k\Omega$, BB2 $\rightarrow R_3 = 60k\Omega$

Bass boost function (BSTO, BSTN, BSTC)

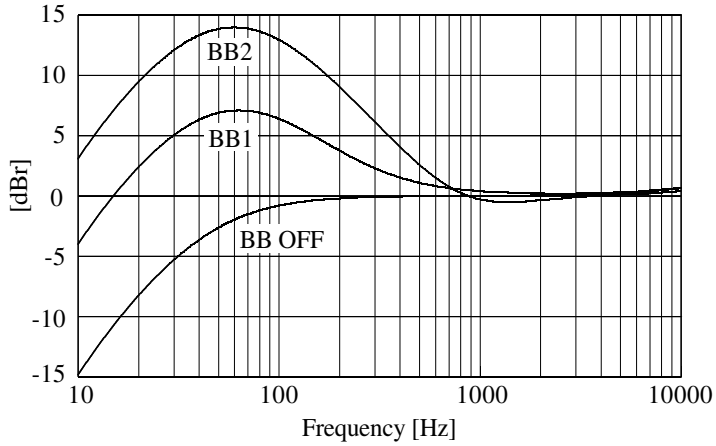
The bass boost characteristic (BB1, BB2) is selected using bit D10. The left-channel and right-channel bass components are mixed and amplified, and then added to the headphone driver amplifier. A capacitor (0.1µF std) connected between BSTC and VREF1 forms a lowpass filter through which the signal from the EVR block passes, boosting the bass component, which is then added to the original signal.

Bass boost examples

IC internal components are R_{IN} = 23kΩ, R1 = 20kΩ, R2 = 10kΩ, R3 = 15kΩ (BB1) or 60kΩ (BB2). The bass boost characteristic also depends on the external resistor and capacitor components connected between BSTO and BSTN, as indicated below.

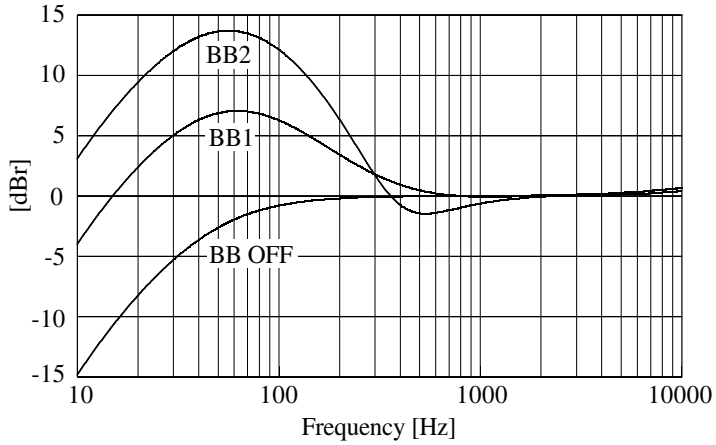
■ Example 1

C_1 = 0.1µF, C_2 = 2200pF, C_{IN} = 1µF, C_{OUT} = 220µF, R_{OUT} = 16Ω (Measurement circuit)



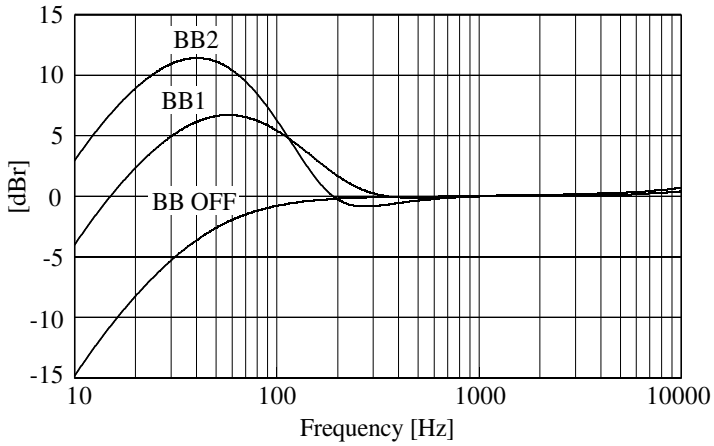
■ Example 2

C_1 = 0.1µF, C_2 = 0.01µF, C_{IN} = 1µF, C_{OUT} = 220µF, R_{OUT} = 16Ω



■ Example 3

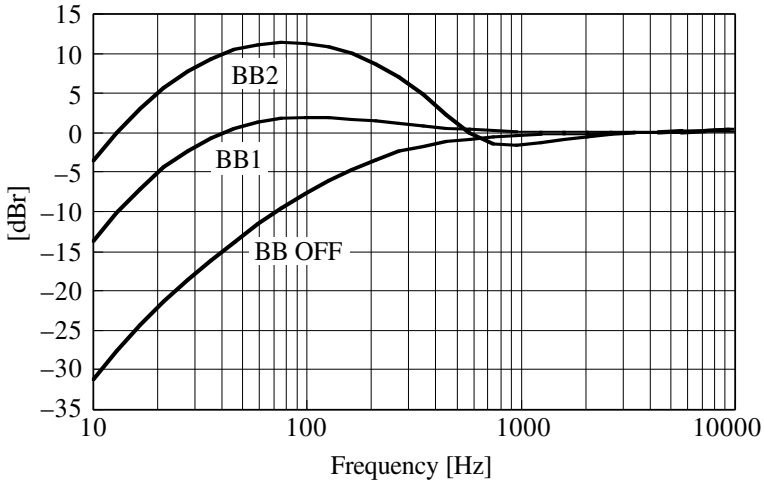
C_1 = 0.1µF, C_2 = 0.047µF, C_{IN} = 1µF, C_{OUT} = 220µF, R_{OUT} = 16Ω



■ Example 4

C_1 = 0.22µF, C_2 = 6800pF, C_{IN} = 0.47µF, C_{OUT} = 47µF, R_{OUT} = 16Ω, 2700Ω resistor connected between BSTN and VREF1

Note that when the output coupling capacitance C_{OUT} is small, the bass signal component margin available before reaching the bass output saturation level is considerably reduced.



Automatic gain control (AGC) function

The AGC function is selected using bit D11. When bass boost is on, whenever the magnitude of either the positive or negative output voltage peak value of LOUT or ROUT exceeds VREF1 + 0.48V (typ), half-wave rectification starts. The resulting detected and smoothed DC potential is compared with the VREF1 potential, and the comparator output signal is used to control the reduction in bass boost gain, thereby increasing the headphone amplifier output bass clip margin.

Power-down Function (PDN)

The power-down function is selected when PDN goes LOW. This reduces the power consumption, while LOUT and ROUT become high impedance. A pull-down resistor connected to PDN is recommended.

Mute Function

Mute function (MUTEN)

The mute function is selected when MUTEN goes LOW. At initial startup, it is recommended that a delay of 2.5 seconds (typ) occur before MUTEN goes HIGH to prevent pop-noise output on LOUT and ROUT that can occur when muting is released and after power-down is released (see mute release timing in figures 4 and 5).

Note that when muting using the MUTEN pin, outputs LOUT and ROUT do not become high impedance. A pull-down resistor connected to MUTEN is recommended.

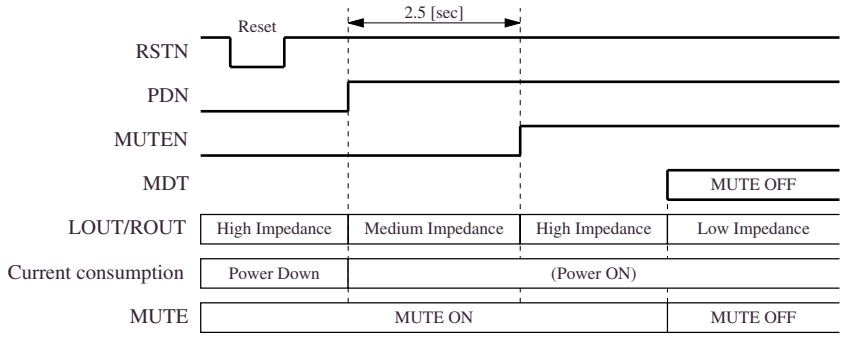


Figure 4. Initial startup recommended mute release timing example 1

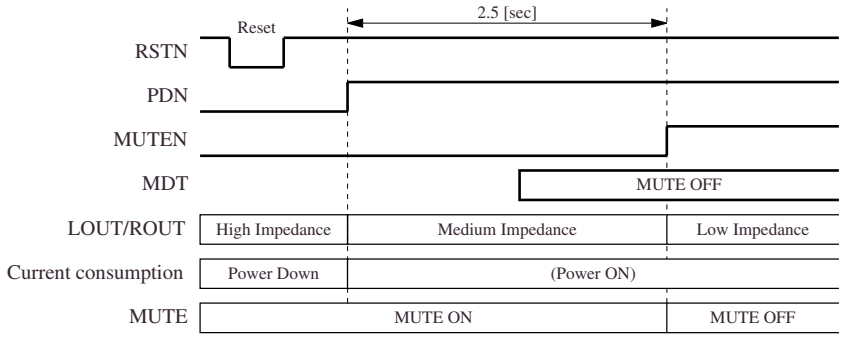


Figure 5. Initial startup recommended mute release timing example 2

Mute function (Microcontroller Data)

Mute is ON when Microcontroller Data D0 to D7 = LOW. Output impedance is HIGH when Microcontroller Data D0 to D7 = LOW, Mute function.

Beep Signal Input/Output (BEEPI, BEEPLO, BEEPRO)

The beep signal is a constant-current output signal on BEEPLO and BEEPRO in response to an input signal on BBEPI. The beep signal input/output circuit should be used when MUTEN is HIGH, when muting using the attenuation data bits D0 to D7, and during power-down.

TYPICAL RESPONSE

V_{DD1} = V_{DD2} = 2.0V, analog input amplitude = 0.025Vrms, input frequency = 1kHz, Ta = 25°C, Measurement circuit, PDN = HIGH, MUTEN = HIGH, MDT D0 to D12 = LOW, unless otherwise noted

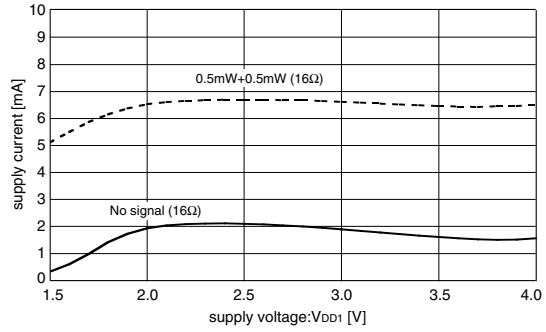


Figure 6. Current consumption vs. Supply voltage

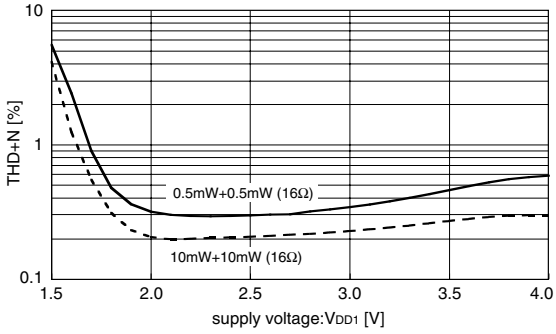


Figure 7. THD+N vs. Supply voltage

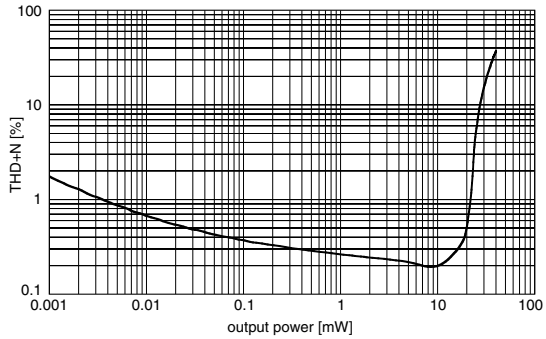


Figure 8. THD+N vs. Output power

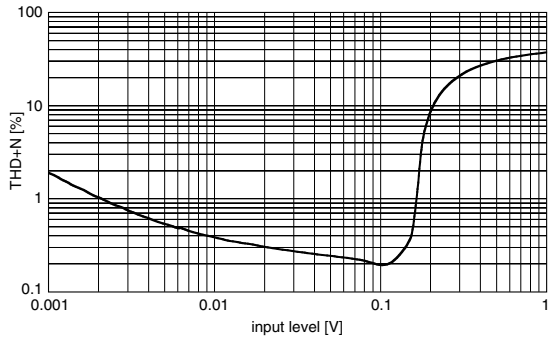


Figure 9. THD+N vs. Input voltage

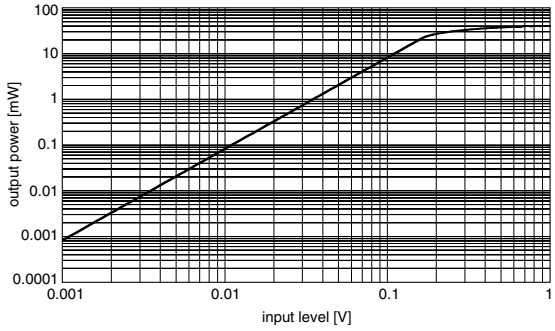


Figure 10. THD+N vs. Input voltage

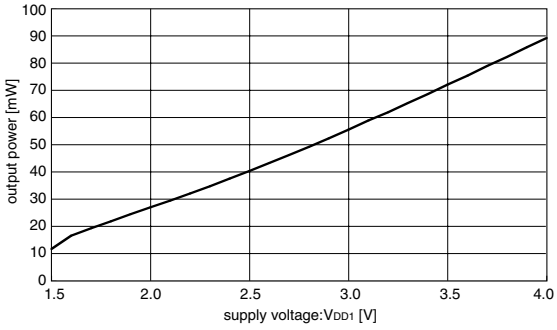


Figure 11. Maximum output power vs. Supply voltage

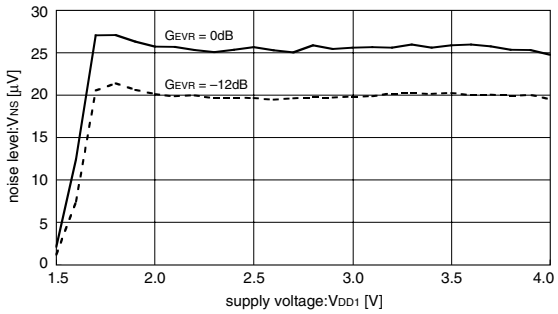


Figure 12. Noise level vs. Supply voltage

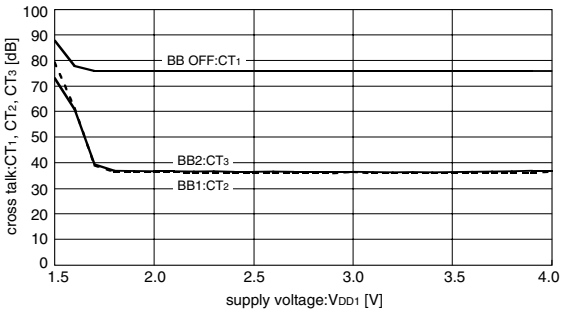


Figure 13. Channel separation vs. Supply voltage

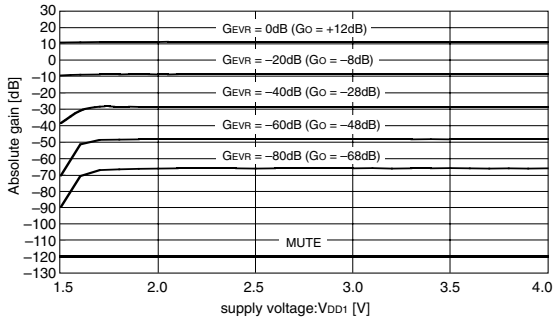


Figure 14. Absolute gain vs. Supply voltage

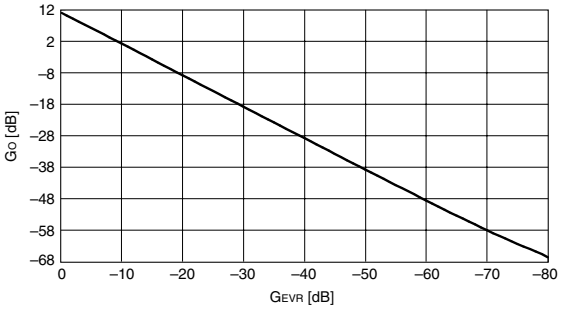


Figure 15. Output voltage gain vs. EVR gain setting

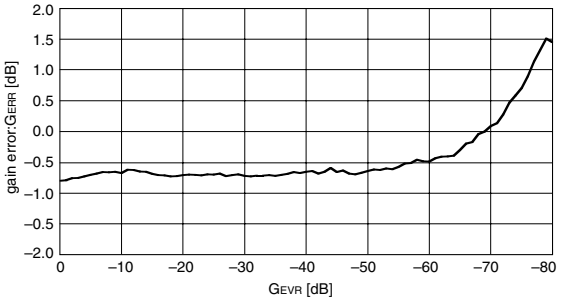


Figure 16. Gain error

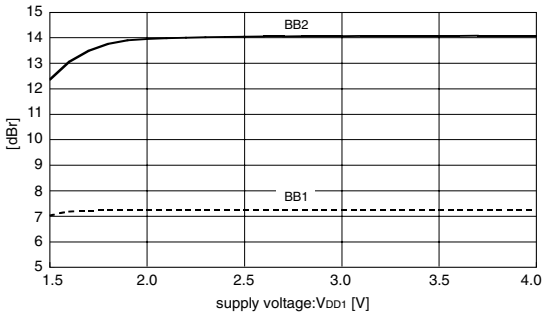


Figure 17. Bass boost gain vs. Supply voltage

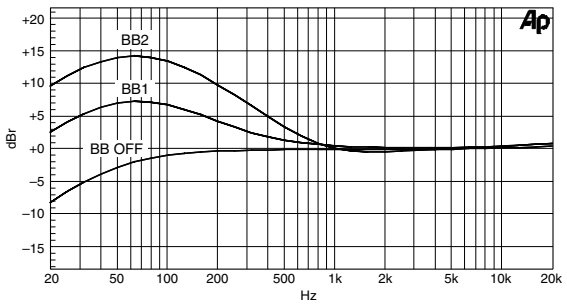


Figure 18. Frequency response vs. Bass boost

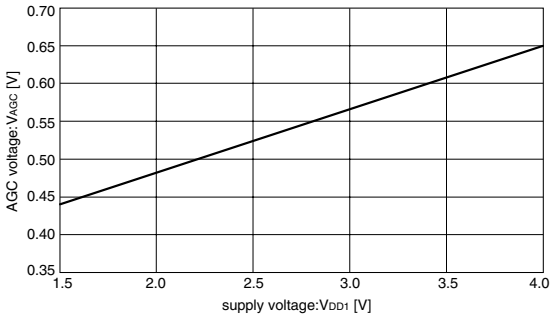


Figure 19. AGC level vs. Supply voltage

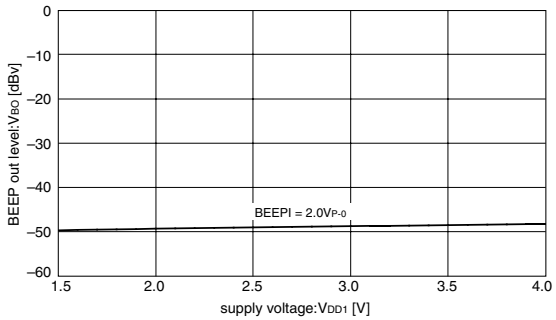


Figure 20. Beep sound output level vs. Supply voltage

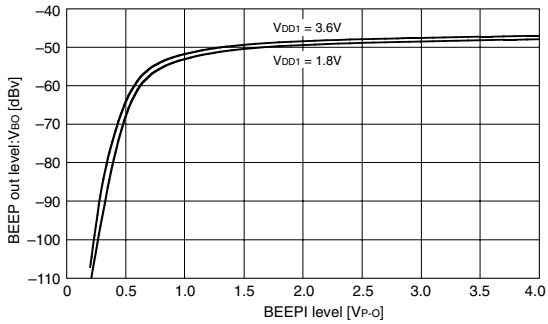


Figure 21. Beep sound output level vs. Beep input level

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