Overview

The SM5906AF is a shock-proof memory controller LSI for video CD players. The operating mode can be set to CD-DA mode, V-CD mode, or Super V-CD mode, and external memory can be selected from 2 options (4M, 16M). It operates from a 2.7 to 3.6 V supply voltage range.

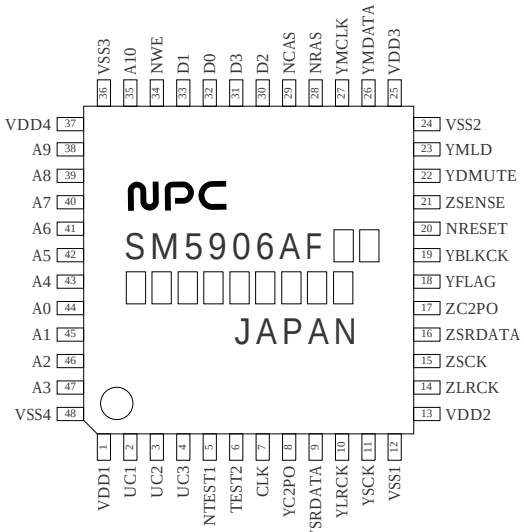
Features

– 2-channel processing
– Serial data input
  • 2s complement, 16-bit/MSB first
  • Right-justified format
  • Wide capture function
    (up to 4 × speed input rate)
  • Selectable 16/24/32-bit clock
– System clock input
  • 384fs (16.9344 MHz)
– Shock-proof memory controller
  • Selectable CD-DA/V-CD/SVC mode
  • 2 external DRAM configurations selectable
    1 × 16M DRAM (4M × 4 bits, refresh cycle = 2048 cycle)
    1 × 4M DRAM (1M × 4 bits)
– Microcontroller interface
  • Serial command write and status read-out
  • Data residual detector:
    11-bit operation, 16-bit output
    (Bits 13 to 15 bit are fixed LOW.)
  • Forced mute
– Extension I/O
    Microcontroller interface for external control using 3 extension I/O pins
– +2.7 to +3.6 V operating voltage range
– Schmitt inputs
    All input pins (including I/O pins) except CLK (system clock)
– Reset signal noise elimination
    Approximately 3.8 µs or longer (65 system clock pulses) continuous LOW-level reset
- 48-pin QFP package (0.5 mm pin pitch)

Ordering Information

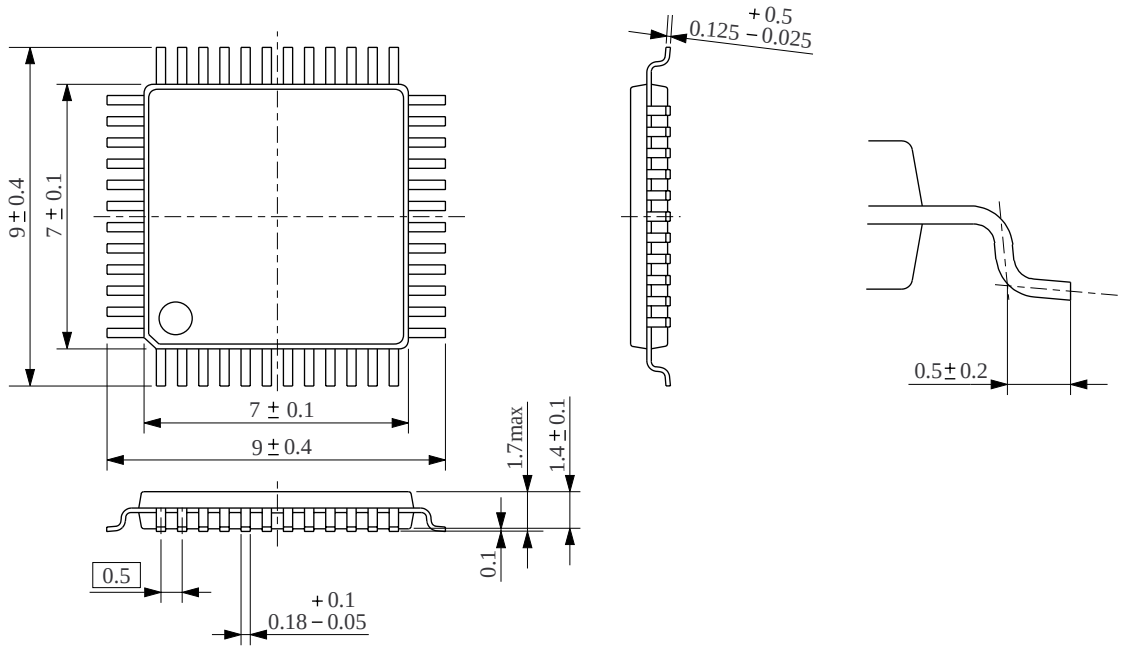
SM5906AF	**48pin QFP**

Pinout (Top View)



Package dimensions (Unit: mm)

48-pin QFP



Pin description

Pin number	Pin name	I/O	Function	Setting	
				H	L
1	VDD1	–	VDD supply pin		
2	UC1	Iu/O	Microcontroller interface extension I/O 1		
3	UC2	Iu/O	Microcontroller interface extension I/O 2		
4	UC3	Iu/O	Microcontroller interface extension I/O 3		
5	NTEST1	Iu	Test pin		Test
6	TEST2	Id	Test pin	Test	
7	CLK	I	16.9344 MHz clock input		
8	YC2PO	I	Serial input C2PO data		
9	YSRDATA	I	Serial input data		
10	YLRCK	I	Serial input LR clock	Left channel	Right channel
11	YSCK	I	Serial input bit clock		
12	VSS1	–	Ground		
13	VDD2	–	VDD supply pin		
14	ZLRCK	O	Serial output LR clock	Left channel	Right channel
15	ZSCK	O	Serial output bit clock		

Iu : Input pin with pull-up resistor, Id : Input pin with pull-down resistor
Iu/O : Input/Output pin (With pull-up resistor when in input mode)

Pin description

Pin number	Pin name	I/O	Function	Setting	
				H	L
16	ZSRDATA	O	Serial output data		
17	ZC2PO	O	Serial output C2PO data		
18	YFLAG	I	Signal processor IC RAM overflow flag		
19	YBLKCK	I	Subcode block clock signal		
20	NRESET	I	System reset pin		Reset
21	ZSENSE	O	Microcontroller interface status output		
22	YDMUTE	I	Forced mute pin	Mute	
23	YMLD	I	Microcontroller interface latch clock		
24	VSS2	–	Ground		
25	VDD3	–	VDD supply pin		
26	YMDATA	I	Microcontroller interface serial data		
27	YMCLK	I	Microcontroller interface shift clock		
28	NRAS	O	DRAM $\overline{\text{RAS}}$ control		
29	NCAS	O	DRAM $\overline{\text{CAS}}$ control		
30	D2	Iu/O	DRAM data input/output 2		
31	D3	Iu/O	DRAM data input/output 3		
32	D0	Iu/O	DRAM data input/output 0		
33	D1	Iu/O	DRAM data input/output 1		
34	NWE	O	DRAM $\overline{\text{WE}}$ control		
35	A10	O	DRAM address 10		
36	VSS3	–	Ground		
37	VDD4	–	VDD supply pin		
38	A9	O	DRAM address 9		
39	A8	O	DRAM address 8		
40	A7	O	DRAM address 7		
41	A6	O	DRAM address 6		
42	A5	O	DRAM address 5		
43	A4	O	DRAM address 4		
44	A0	O	DRAM address 0		
45	A1	O	DRAM address 1		
46	A2	O	DRAM address 2		
47	A3	O	DRAM address 3		
48	VSS4	–	Ground		

Iu : Input pin with pull-up resistor, Id : Input pin with pull-down resistor
Iu/O : Input/Output pin (With pull-up resistor when in input mode)

Absolute maximum ratings

(V_{SS1} = V_{SS2} = V_{SS3} = V_{SS4} = 0V, V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4} pin voltage = V_{DD})

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	– 0.3 to 4.0	V
Input voltage	V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature	T_{STG}	– 55 to 125	˚C
Power dissipation	P_D	340	mW
Soldering temperature	T_{SLD}	255	˚C
Soldering time	t_{SLD}	10	sec

Note. Refer to pin summary on the next page.
Values also apply for supply inrush and switch-off.

Electrical characteristics

Recommended operating conditions

(V_{SS1} = V_{SS2} = V_{SS3} = V_{SS4} = 0V, V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4} pin voltage = V_{DD})

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	2.7 to 3.6	V
Operating temperature	T_{OPR}	– 10 to 70	˚C

DC characteristics

Standard voltage:(V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = 2.7 to 3.6V, V_{SS1} = V_{SS2} = V_{SS3} = V_{SS4} = 0V, Ta = – 10 to 70˚C)

Parameter	Pin	Symbol		Condition	Rating			Unit
					Min	Typ	Max	
Current consumption	VDD	I_{DD}		(*A)SHPRF ON		4.5	9.0	mA
				(*A)Through mode		1.5	3.0	mA
Input voltage	CLK	H level	V_{IH1}		0.8V_{DD}			V
		L level	V_{IL1}				0.2V_{DD}	V
	(*2,3,5)	H level	V_{IH2}		V_{DD} – 0.3			V
		L level	V_{IL2}				0.6	V
	(*4)	H level	V_{IH3}		0.8V_{DD}			V
		L level	V_{IL3}				0.2V_{DD}	V
Output voltage	(*5)	H level	V_{OH1}	I_{OH} = – 1.0 mA	V_{DD} – 0.4			V
		L level	V_{OL1}	I_{OL} = 1.0 mA			0.4	V
	(*6)	H level	V_{OH2}	I_{OH} = – 1.0 mA	V_{DD} – 0.4			V
		L level	V_{OL2}	I_{OL} = 1.0 mA			0.4	V
Input current	(*4)	I_{IH}		V_{IN} = V_{DD}	10	25	80	µA
	(*3,5)	I_{IL}		V_{IN} = 0V	10	25	80	µA
Input leakage current	(*1,2,5)	I_{LH}		V_{IN} = V_{DD}			1.0	µA
	(*1,2,4)	I_{LL}		V_{IN} = 0V			1.0	µA

(*A) V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = 3 V, CLK input frequency f_{XTI}= 384fs = 16.9344 MHz, all outputs unloaded,
SHPRF: Shock-proof,
typical values are for V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = 3 V.

<Pin summary>

(*1)	Pin function	Clock input pin
	Pin name	CLK
(*2)	Pin function	Schmitt input pins
	Pin name	YSRDATA, YLRCK, YSCK, YC2PO, YFLAG, NRESET, YBLKCK, YDMUTE, YMLD, YMDATA, YMCLK
(*3)	Pin function	Schmitt input pin with pull-up
	Pin name	NTEST1
(*4)	Pin function	Schmitt pin with pull-down
	Pin name	TEST2
(*5)	Pin function	I/O pins (Schmitt input with pull-up in input state)
	Pin name	UC1, UC2, UC3, D0, D1, D2, D3
(*6)	Pin function	Outputs
	Pin name	ZSCK, ZLRCK, ZSRDATA, ZC2PO, ZSENSE, NCAS, NWE, NRAS, A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10

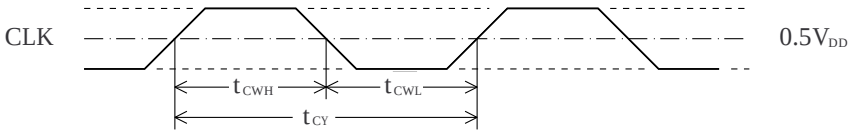
AC characteristics

Standard voltage: V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = 2.7 to 3.6V, V_{SS1} = V_{SS2} =V_{SS3} =V_{SS4} =0V, Ta = –10 to 70 ˚C
(*) Typical values are for fs = 44.1 kHz

System clock (CLK pin)

Parameter	Symbol	Condition	Rating			Unit
		System clock	Min	Typ	Max	
Clock pulsewidth (HIGH level)	t_{CWH}		26	29.5	50	ns
Clock pulsewidth (LOW level)	t_{CWL}		26	29.5	50	ns
Clock pulse cycle	t_{CY}	384fs	58	59	100	ns

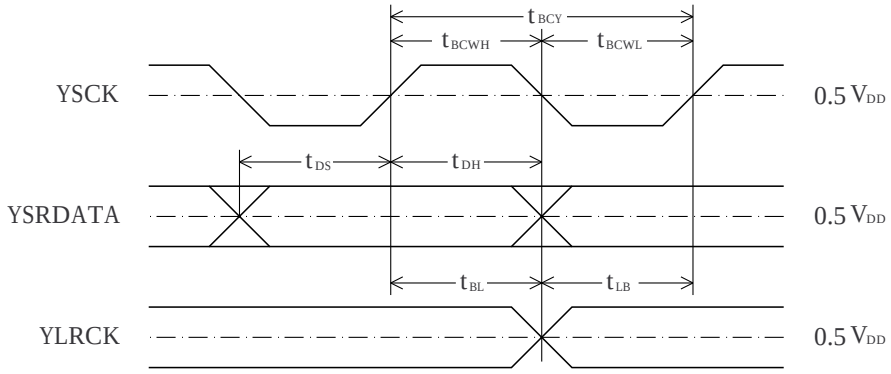
System clock input

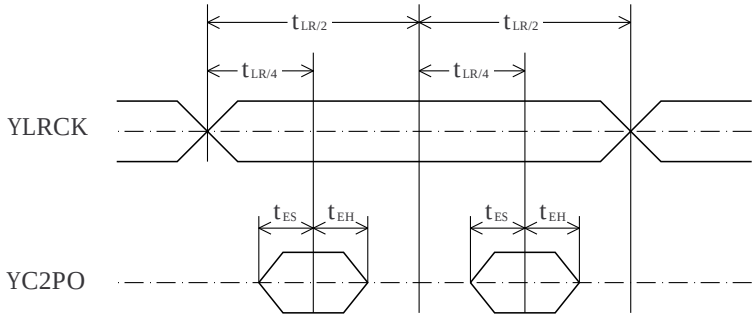


Serial input (YSRDATA, YLRCK, YSCK YC2PO pins)

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
YSCK pulsewidth (HIGH level)	t_{BCWH}	75			ns	
YSCK pulsewidth (LOW level)	t_{BCWL}	75			ns	
YSCK pulse cycle	t_{BCY}	150			ns	
YSRDATA setup time	t_{DS}	50			ns	
YSRDATA hold time	t_{DH}	50			ns	
Last YSCK rising edge to YLRCK edge	t_{BL}	50			ns	
YLRCK edge to first YSCK rising edge	t_{LB}	50			ns	
YLRCK pulse frequency See note below.		0		4fs		Memory system ON (MSON=H)
		fs		fs		Memory system OFF (MSON=L)
YC2PO setup time	t_{ES}	1			µs	
YC2PO hold time	t_{EH}	1			µs	

Note. When the memory system is OFF (through mode), the input data rate is synchronized to the system clock input (384fs), so input data needs to be at 1/384 of this frequency. But, this IC can tolerate a certain amount of jitter. For details, refer to Through-mode operation.



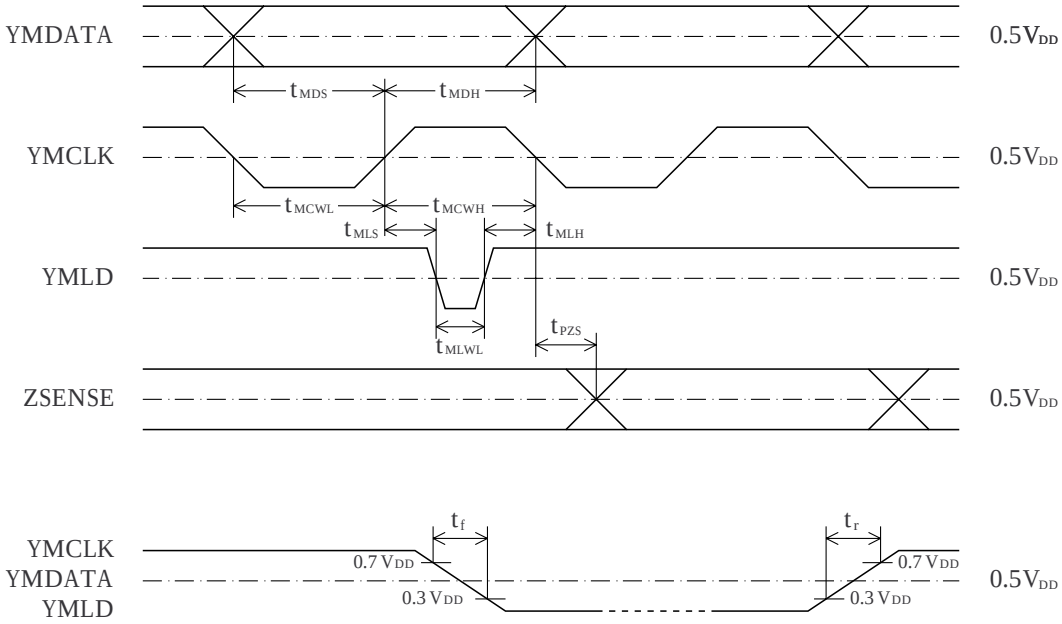


Microcontroller interface (YMCLK, YMDATA, YMLD, ZSENSE pins)

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
YMCLK LOW-level pulsewidth	t_{MCWL}	30 + 2t_{CY}			ns
YMCLK HIGH-level pulsewidth	t_{MCWH}	30 + 2t_{CY}			ns
YMDATA setup time	t_{MDS}	30 + t_{CY}			ns
YMDATA hold time	t_{MDH}	30 + t_{CY}			ns
YMLD LOW-level pulsewidth	t_{MLWL}	30 + 2t_{CY}			ns
YMLD setup time	t_{MLS}	30 + t_{CY}			ns
YMLD hold time	t_{MLH}	30 + t_{CY}			ns
Rise time	t_r			100	ns
Fall time	t_f			100	ns
ZSENSE output delay	t_{PZS}			100 + 3t_{CY}	ns

Note. t_{CY} is the system clock (CLK) input (384fs) cycle time.

t_{CY} = 59 ns, t_{NRST} (min) = 3.8 µs when fs = 44.1 kHz

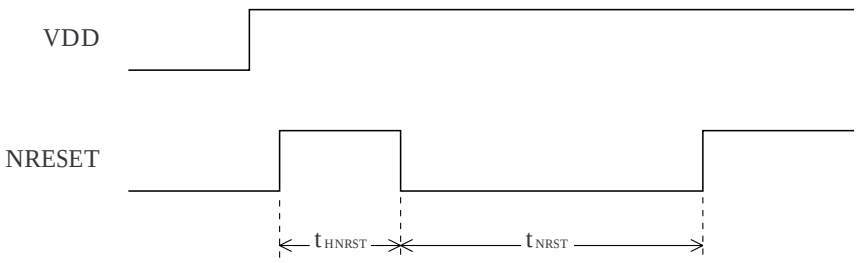


Reset input (NRESET pin)

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
First HIGH-level after supply voltage rising edge	t_{HNRST}	0			t_{CY} (Note)
NRESET pulsewidth	t_{NRST}	64			t_{CY} (Note)

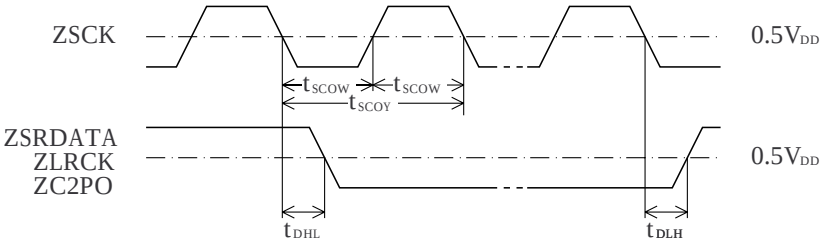
Note. t_{CY} is the system clock (CLK) input (384fs) cycle time.

t_{CY} = 59 ns, t_{NRST} (min) = 3.8 µs when fs = 44.1 kHz



Serial output (ZSRDATA, ZLRCK, ZSCK ZC2PO pins)

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
ZSCK pulsewidth	t_{SCOW}	15 pF load		1/96fs		
ZSCK pulse cycle	t_{SCOY}	15 pF load		1/48fs		
ZSRDATA, ZLRCK, ZC2PO output delay time	t_{DHL}	15 pF load	0		60	ns
	t_{DLH}	15 pF load	0		60	ns

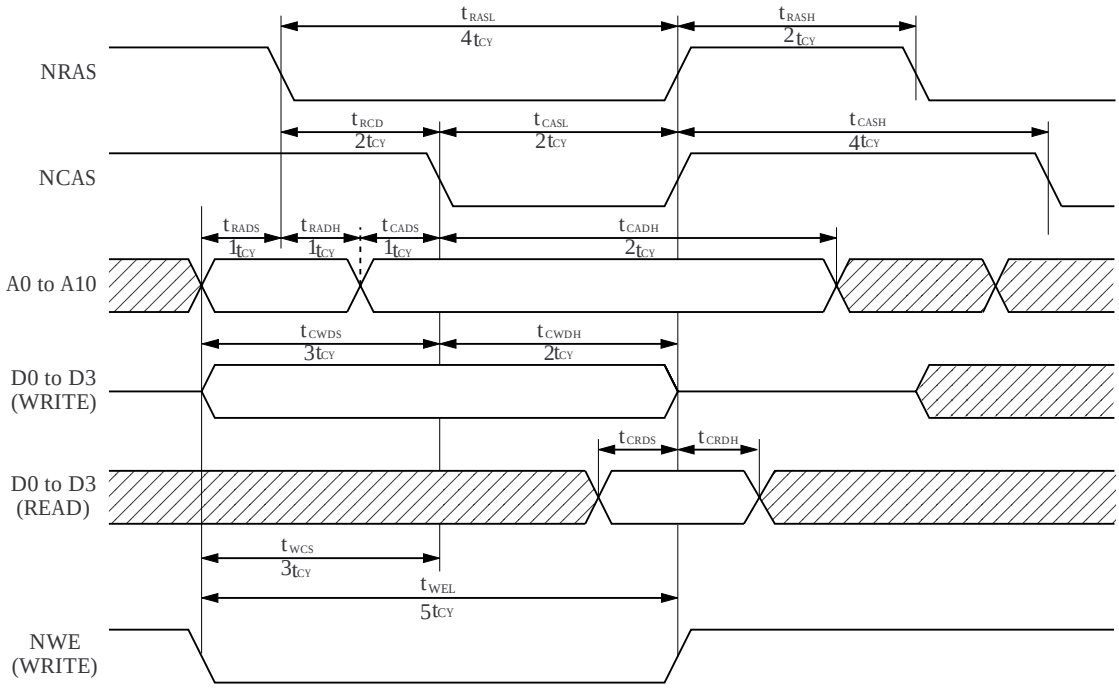


DRAM access timing (NRAS, NCAS, NWE, A0 to A10, D0 to D3)

Parameter		Symbol	Condition		Rating			Unit
					Min	Typ	Max	
NRAS pulsewidth		t_{RASL}	15 pF load			4		t_{CY}(note)
		t_{RASH}	15 pF load		2			t_{CY}
NRAS falling edge to NCAS falling edge		t_{RCD}	15 pF load			2		t_{CY}
NCAS pulsewidth		t_{CASH}	15 pF load		4			t_{CY}
		t_{CASL}	15 pF load			2		t_{CY}
NRAS	Setup time	t_{RADS}	15 pF load			1		t_{CY}
falling edge to address	Hold time	t_{RADH}	15 pF load			1		t_{CY}
NCAS	Setup time	t_{CADS}	15 pF load			1		t_{CY}
falling edge to address	Hold time	t_{CADH}	15 pF load			2		t_{CY}
NCAS	Setup time	t_{CWDS}	15 pF load			3		t_{CY}
falling edge to data write	Hold time	t_{CWDH}	15 pF load			2		t_{CY}
NCAS	Input setup	t_{CRDS}			40			ns
rising edge to data read	Input hold	t_{CRDH}			0			ns
NWE pulsewidth		t_{WEL}	15 pF load			5		t_{CY}
NWE falling edge to NCAS falling edge		t_{WCS}	15 pF load			3		t_{CY}
Refresh cycle		t_{REF}	4M	CD-DA MODE			3.0	ms
(fs = 44.1 kHz playback)			DRAM	VCD MODE			2.6	ms
			× 1	SVC MODE			1.3	ms
Memory system ON			16M	CD-DA MODE			5.9	ms
Read sequence operation			DRAM	VCD MODE			5.2	ms
(RDEN=H)			× 1	SVC MODE			2.6	ms

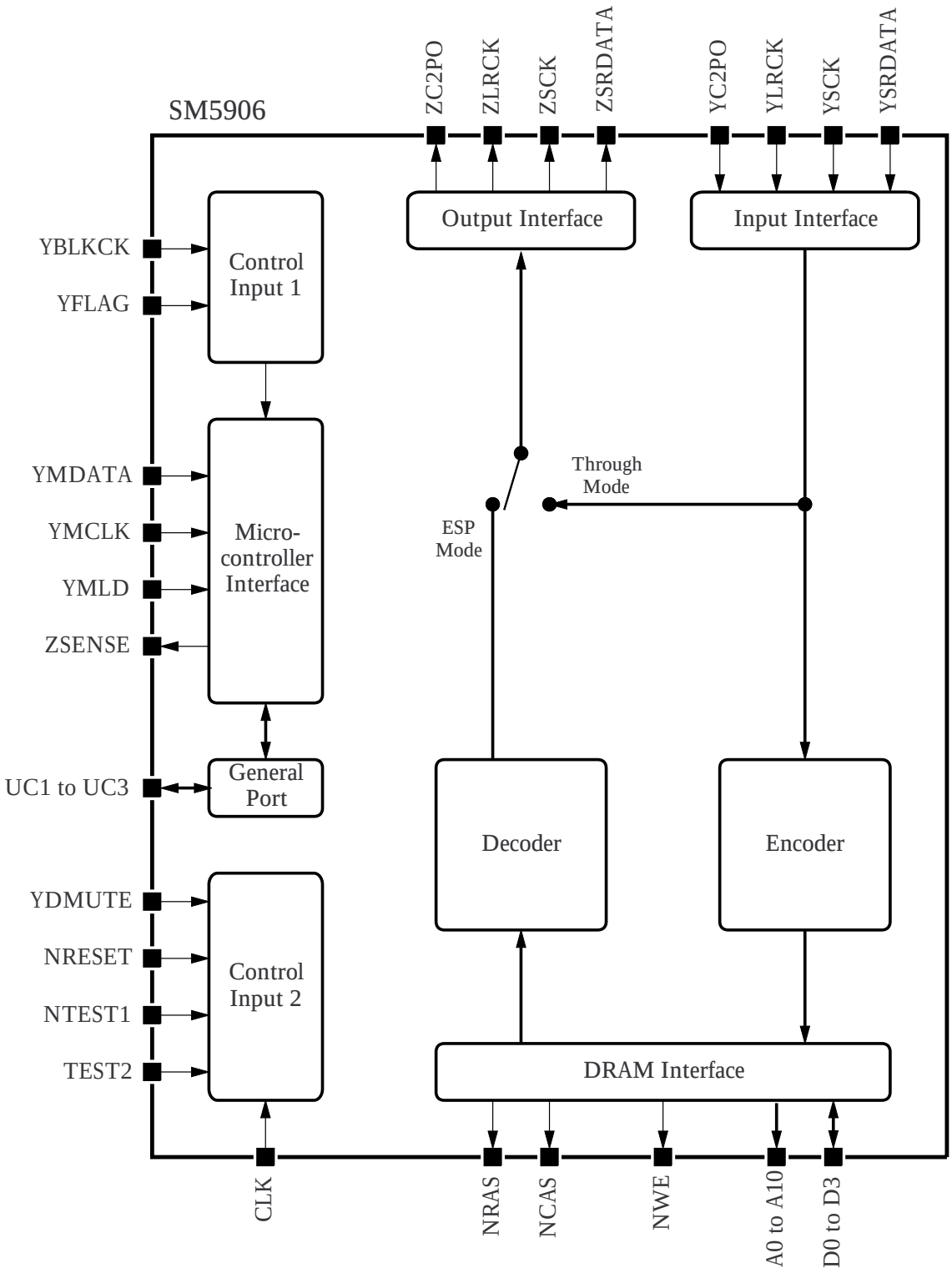
Note. t_{CY} is the system clock (CLK) input (384fs) cycle time. t_{CY} = 59 ns when fs = 44.1 kHz

DRAM access timing



The NWE terminal output is fixed HIGH during read timing.

Block diagram



Functional description

SM5906AF has two modes of operation; shock-proof mode and through mode.

The operating sequences are controlled using commands from a microcontroller.

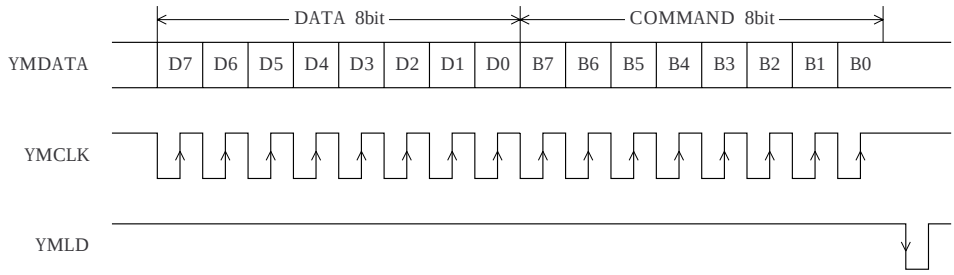
Microcontroller interface

Command format

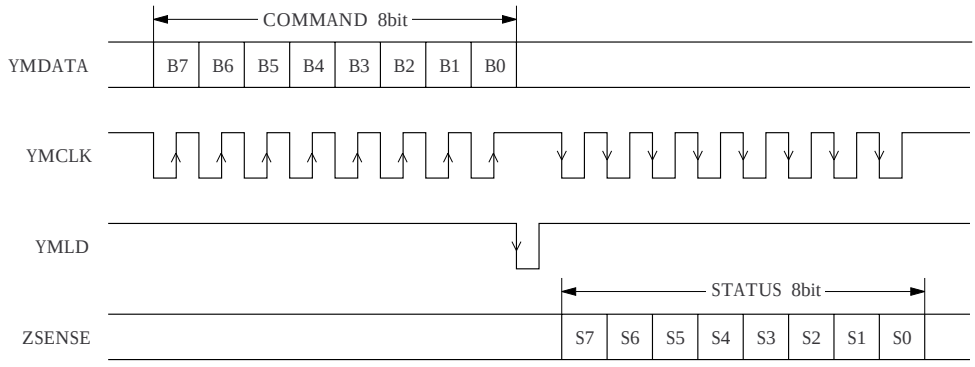
Commands from the microcontroller are input using 3-wire serial interface inputs; data (YMDATA), bit clock (YMCLK) and load signal (YMLD).

In the case of a read command from the microcontroller, bit serial data is output (ZSENSE) synchronized to the bit clock input (YMCLK).

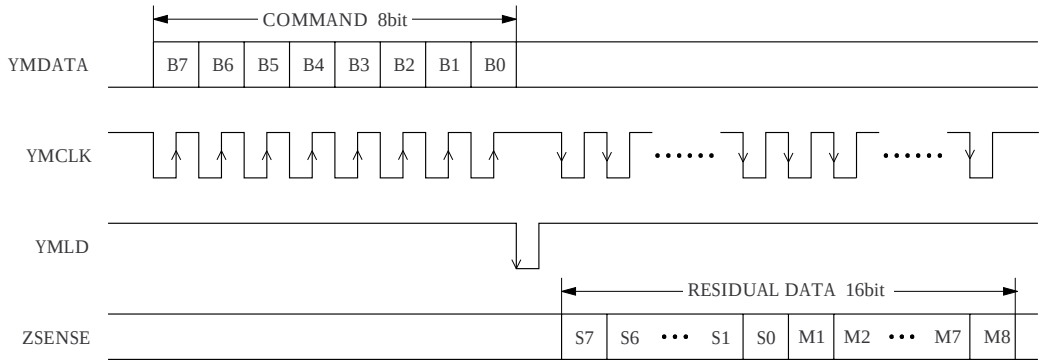
Write command format (Commands 80 to 85)



Read command format (Commands 90, 91, 93)



Read command format (Command 92 (memory residual read))



(M4 to M8 are always 0.)

Command table

Write command summary

MS command 80

Shock-proof memory system settings

80hex = B7 B6 B5 B4 1000 B3 B2 B1 B0 0000

Bit	Name	Function	H operation	Reset level
D7	MSWREN	Write sequence start/stop	Start	L
D6	MSWACL	Write address reset	Reset	L
D5	MSRDEN	Read sequence start/stop	Start	L
D4	MSRACL	Read address reset	Reset	L
D3	MSDCN2	MSDCN2=HIGH, MSDCN1=HIGH: 3-pair comparison start (ASH connect) MSDCN2=HIGH, MSDCN1=LOW: 2-pair comparison start (SH connect)		L
D2	MSDCN1	MSDCN2=LOW, MSDCN1=HIGH: Direct-connect start (S connect) MSDCN2=LOW, MSDCN1=LOW: Connect operation stop		L
D1	WAQV	Q data valid	Valid	L
D0	MSON	Memory system ON	ON	L

( ) : VCD or SVC mode

Extension I/O settings 81

Extension I/O port input/output settings

81hex = B7 B6 B5 B4 1000 B3 B2 B1 B0 0001

Bit	Name	Function	H operation	Reset level
D7				
D6				
D5				
D4				
D3				
D2	UC3OE	Extension I/O port UC3 input/output setting	Output	L
D1	UC2OE	Extension I/O port UC2 input/output setting	Output	L
D0	UC1OE	Extension I/O port UC1 input/output setting	Output	L

Extension I/O output data settings 82

Extension port HIGH/LOW output level

A port setting is invalid if that port has already been defined as an input using the 81H command above.

82hex = B7 B6 B5 B4 1000 B3 B2 B1 B0 0010

Bit	Name	Function	H operation	Reset level
D7				
D6				
D5				
D4				
D3				
D2	UC3WD	Extension I/O port UC3 output data setting	H output	L
D1	UC2WD	Extension I/O port UC2 output data setting	H output	L
D0	UC1WD	Extension I/O port UC1 output data setting	H output	L

Function settings 83

83hex = 1000 0011 (B7 B6 B5 B4 B3 B2 B1 B0)

Bit	Name	Function	H operation	Reset level
D7	NMSOFF	Input signals connected directly to the outputs (changes instantaneously)	New through mode	L
D6	MUTE	Forced muting (changes instantaneously)	Mute ON	L
D5	REFRESH	DRAM refresh cycle performed during momentary pause to restore data	REFRESH ON	L
D4	SCOFF	Ignore sync cycle, and update comparison data when sync data is detected.	SYNCCNT OFF	L
D3				
D2				
D1				
D0				

Refer to "Forced mute", and "SYNC and Header data".

Option settings 85

85hex = 1000 0101 (B7 B6 B5 B4 B3 B2 B1 B0)

Bit	Name	Function	H operation	Reset level
D7	RAMSEL	DRAM select (16M/4M)	16M	L
D6				
D5				
D4	YFLGS	FLAG6 set conditions YFLGS = LOW, YFLAG = LOW : FLAG6 active YFLGS = HIGH, YFLAG = HIGH : FLAG6 active		L
D3	IBSEL2	Bit clock select IBSEL2 = HIGH, IBSEL1 = HIGH : 32-bit mode		L
D2	IBSEL1	IBSEL2 = LOW, IBSEL1 = HIGH : 16-bit mode All other cases: 24-bit mode		L
D1	CDMODE2	Mode select – When MSON = HIGH CDMODE2 = LOW, CDMODE1 = LOW : CDDAMODE CDMODE2 = LOW, CDMODE1 = HIGH : VCDMODE CDMODE2 = HIGH, CDMODE1 = LOW : SVCMODE CDMODE2 = HIGH, CDMODE1 = HIGH : VCDMODE		L
D0	CDMODE1	– When MSON = LOW CDMODE2 = LOW, CDMODE1 = LOW : CDDAMODE CDMODE2 = LOW, CDMODE1 = HIGH : VCDMODE CDMODE2 = HIGH, CDMODE1 = LOW : CDDAMODE CDMODE2 = HIGH, CDMODE1 = HIGH : VCDMODE		L

Read command summary

Shock-proof memory status (1) 90

90hex = B7 B6 B5 B4 B3 B2 B1 B0 = 1001 0000

Bit	Name	Function	HIGH-level state
S7	FLAG6	Signal processor IC jitter margin exceeded	Exceeded
S6	MSOVF	Write overflow (Read once only when RA exceeds WA)	DRAM overflow
S5	BOVF	Input buffer memory overflow because sampling rate of input data is too fast	Input buffer memory overflow
S4	SYNCER	Sync data not verified for ≥ 2 blocks	Sync data not received
S3	DCOMP	Data compare-connect sequence operating	Compare-connect sequence operating
S2	MSWIH	Write sequence stop due to internal factors	Writing stopped
S1	MSRIH	Read sequence stop due to internal factors	Reading stopped
S0	SYNCWAR	Sync data not verified for 1 block	Sync data not received

Refer to "Status flag operation summary".

Shock-proof memory status (2) 91

91hex = B7 B6 B5 B4 B3 B2 B1 B0 = 1001 0001

Bit	Name	Function	HIGH-level state
S7	MSEMP	Valid data empty state (Always HIGH when RA exceeds VWA)	No valid data
S6	OVFL	Write overflow state (Always HIGH when WA exceeds RA)	Memory full
S5	WRSQ	WR sequence operating state	Writing
S4	RDSQ	RD sequence operating state	Reading
S3			
S2			
S1			
S0			

Refer to "Status flag operation summary".

Shock-proof memory valid data residual 92

92hex = B7 B6 B5 B4 B3 B2 B1 B0 = 1001 0010

Bit	Name	Function	
S7	AM21	Valid data accumulated VWA-RA (MSB) 8M bits	
S6	AM20	4M bits	
S5	AM19	2M bits	
S4	AM18	1M bits	
S3	AM17	512k bits	
S2	AM16	256k bits	
S1	AM15	128k bits	
S0	AM14	64k bits	
M1	AM13	32k bits	
M2	AM12	16k bits	
M3	AM11	8k bits	
M4	AM10	4k bits	Output fixed LOW
M5	AM09	2k bits	Output fixed LOW
M6	AM08	1k bits	Output fixed LOW
M7	AM07	512 bits	Output fixed LOW
M8	AM06	256 bits	Output fixed LOW

Note. The time conversion factor varies depending on the compression bit mode.(M = 1,048,576 K= 1,024)
Residual time (sec) = Valid data residual (Mbits) × Time conversion value K
where the Time conversion value K (sec/Mbit) ≈ 0.74 (CD-DA), 0.66 (VCD), 0.33 (SVC).

Extension I/O inputs 93

Input data entering (or output data from) an extension port terminal is echoed to the microcontroller.
(That is, the input data entering an I/O port configured as an input port using the 81H command,
OR the output data from a pin configured as an output port using the 82H command.)

93hex = B7 B6 B5 B4 B3 B2 B1 B0 = 1001 0011

Bit	Name	Function	HIGH-level state
S7			
S6			
S5			
S4			
S3			
S2	UC3RD		
S1	UC2RD		
S0	UC1RD		

Status flag operation summary

Flag name	Read method		
FLAG6	READ 90H bit 7	Meaning	– Indicates to the CD signal processor DSP (used for error correction, de-interleaving) that a disturbance has exceeded the RAM jitter margin.
		Set	– Set according to the YFLAG input and the operating state of YFLGS. – FLAG6 set conditions When YFLGS=0, YFLAG=LOW When YFLGS=1, YFLAG=HIGH
		Reset	– By 90H status read – By 80H command when MSON=ON – After external reset – When MSWACL, MSRACL are issued
MSOVF	READ 90H bit 6	Meaning	– Indicates once only that a write to external DRAM has caused an overflow. (When reset by the 90H status read command, this flag is reset even if the overflow condition continues.)
		Set	– When the write address (WA) exceeds the read address (RA)
		Reset	– By 90H status read – After external reset – When MSWACL, MSRACL are issued
BOVF	READ 90H bit 5	Meaning	– Indicates input data rate was too fast causing buffer overflow and loss of data
		Set	– When data is input while the previous data is still being processed.
		Reset	– By 90H status read – After external reset – When MSWACL, MSRACL are issued
SYNCER	READ 90H bit 4	Meaning	– Indicates residual is not updated because sync data not verified for ≥ 2 blocks
		Set	– When sync data is not verified for ≥ 2 blocks (C2PO error etc.)
		Reset	– When sync data is verified – After external reset – When MSWACL, MSRACL are issued
DCOMP	READ 90H bit 3	Meaning	– Indicates that a compare-connect sequence is operating
		Set	– When a (3-pair or 2-pair) compare-connect start command is received (MSDCN2=1) – When a direct connect command is received (MSDCN2=0, MSDCN1=1)
		Reset	– When a (3-pair or 2-pair) comparison detects conforming data – When the connect has been performed after receiving a direct connect command – When a compare-connect stop command (MSDCN2=0, MSDCN1=0) is received – When a MSWREN=1 command is received (However, if a compare-connect command is received at the same time, WREN has priority.) – After external reset
MSWIH	READ 90H bit 2	Meaning	– Indicates that the write sequence has stopped due to internal factors (not microcontroller commands)
		Set	– When FLAG6 (above) is set – When BOVF (above) is set – When MSOVF (above) is set
		Reset	– When conforming data is detected after receiving a compare-connect start command – When the connect has been performed after receiving a direct connect command – When a read address clear (MSRACL) or write address clear (MSWACL) command is received – After external reset

Flag name	Read method		
MSRIH	READ 90H bit 1	Meaning	– Indicates that the read sequence has stopped due to internal factors (not microcontroller commands)
		Set	– When the valid data residual becomes 0
		Reset	– By 90H status read – When a read address clear (MSRACL) or write address clear (MSWACL) command is recieved – After external reset
SYNCWAR	READ 90H bit 0	Meaning	– Indicates residual is not updated because sync data not verified for 1 block
		Set	– When sync data is not verified for 1 block (C2PO error etc.) – When sync data does not occur within a 2352-byte interval
		Reset	– By 90H status read – After external reset – When MSWACL, MSRACL are issued
MSEMP	READ 91H bit 7	Meaning	– Indicates that the valid data residual has become 0
		Set	– When the VWA (final valid data's next address) = RA (address from which the next read would take place)
		Reset	– Whenever the above does not apply
OVFL	READ 91H bit 6	Meaning	– Indicates a write to external DRAM overflow state
		Set	– When the write address (WA) exceeds the read address (RA). (Note: This flag is not set when WA=RA through an address initialize or reset operation.)
		Reset	– When the read address (RA) is advanced by the read sequence – When a read address clear (MSRACL) or write address clear (MSWACL) command is issued – After external reset
WRSQ	READ 91H bit 5	Meaning	– Indicates that the write sequence (input data entry, DRAM write) is operating
		Set	– By the 80H command when MSWREN=1 – When conforming data is detected during compare-connect operation – When the connect has been performed after receiving a direct connect command
		Reset	– When the FLAG6 flag=1 (above) – When the OVFL flag=1 (above) – When the BOVF flag=1 (above) – By the 80H command when MSWREN=0 – By the 80H command when MSDCN1=1 or MSDCN2=1 (compare-connect start command) – By the 80H command when MSON=0 – After external reset Note. Reset conditions have priority over set conditions. However, simultaneous MSWREN = 1 and compare-connect operation has precedence over WRSQ.
RDSQ	READ 91H bit 4	Meaning	– Indicates that the read sequence (read from DRAM, data output) is operating
		Set	– By a new 80H command when MSRDEN=1 and the MSEMP flag=0 (above)
		Reset	– Whenever the above does not apply

Write command supplementary information

80H (MS command)

– MSWREN

When 1: Write sequence starts

Invalid when MSON is not 1 within the same 80H command

Invalid when FLAG6=1

Invalid when OVFL=1

If MSWREN = 1 command is issued during compare-connect operation, MSDCN1 and MSDCN2 must be set to 0. Write sequence starts from the point the command is issued as direct-connect (CD-DA) sequence.

When 0: Write sequence stops

– MSWACL

When 1: Initializes the write address (WA)

When 0: No operation

– MSRDEN

When 1: Read sequence starts

Does not perform read sequence if MSON=1. If there is no valid data, read sequence temporarily stops. But, because the MSRDEN flag setting is maintained as is, the sequence automatically re-starts when valid data appears.

When 0: Read sequence stops

– MSRACL

When 1: Initializes the read address (RA)

When 0: No operation

– MSDCN2, MSDCN1

Refer to compare-connect sequence

After MSWACL and MSRACL, set MSWREN = 1 to start the write sequence. If the start occurs in direct-connect mode, a noise may be generated.

CDDAMODE

When 1 and 1: 3-pair compare-connect sequence starts

When 1 and 0: 2-pair compare-connect sequence starts

When 0 and 1: Direct connect sequence starts

When 0 and 0: Compare-connect sequence stops. No operation if a compare-connect sequence is not operating.

VCD, SVCMODE

When 1 and 1: Video CD compare-connect sequence, checking C2PO, starts (ASH connect)

When 1 and 0: Video CD compare-connect sequence, ignoring C2PO, starts (SH connect)

When 0 and 1: Connect sequence, checking sync data only, starts (S connect)

When 0 and 0: Compare-connect sequence stops. No operation if a compare-connect sequence is not operating.

– WAQV

When 1: If a write address (WA) is verified as a valid at the preceding YBLKCK falling edge timing, it becomes a valid write address (VWA).

When 0: No operation

– MSON

When 1: Memory system turns ON and shock-proof operation starts

When 0: Memory system turns OFF and through-mode playback starts. Even in through mode, the CDDAMODE and VCDMODE settings may become active. VCDMODE settings should be set if using C2PO. (see 85H command)

81H (Extension I/O port settings)

82H (Extension I/O port output data settings)

83H (NMSOFF, MUTE, REFRESH, SCOFF settings)

– NMSOFF (new through mode)

When 1: Input signals YSCK, YSRDATA, YLRCK, YC2PO are connected directly to outputs ZSCK, ZSRDATA, ZLRCK, ZC2PO as is.

When 0: No operation

– MUTE (forced muting)

When 1: Outputs are instantaneously muted to 0. (note 1)

Same effect as taking the YDMUTE pin HIGH.

When 0: No muting (note 1)

(note1) Effective at the start of left-channel output data.

– MUTE, YDMUTE relationship

When all mute inputs are 0, mute is released.

– REFRESH (refresh mode)

When 1: During momentary pause in shock-proof mode operation, DRAM is accessed in a refresh cycle to maintain data written to DRAM.

When 0: No operation

– SCOFF (SYNC counter off)

A sync counter is used to count 588 data samples per sync cycle. The counter starts when sync data is detected, and valid data is updated after each cycle if sync data is verified. If sync data is not detected, the SYNCWAR and SYNCER flags are set.

When 1: The counter is off (sync cycle is not involved) and valid data is updated when the sync data is detected and verified.

When 0: Counts the sync cycles, and updates valid data.

85H (option settings)

– RAMSEL

When 0 : 4M DRAMs (1M×4 bits)

When 1 : 16M DRAMs (4M×4 bits)

– YFLGS

When 0 : Sets FLAG6 when YFLAG=0

When 1 : Sets FLAG6 when YFLAG=1

– IBSEL2, IBSEL1

When 0 and 1 : Input bit clock(YSCK)=16-bit mode

When 1 and 1 : Input bit clock(YSCK)=32-bit mode

In all other cases: Input bit clock(YSCK)=24-bit mode

Changing mode without initializing during operation is possible.

– CDMODE2, CDMODE1

When 0 and 0 : CDDA mode

YSRDATA only is stored as data in DRAM, with output data on ZSRDATA.

When 1 and 0 : SVC mode

YSRDATA and YC2PO are stored as data in DRAM, with output data at double speed if MSON = 1 only (CD-DA mode if MSON = 0).

In all other cases: VCD mode

YSRDATA and YC2PO are stored as data in DRAM, with output data on ZSRDATA and ZC2PO.

Changing mode without initializing during operation is possible.

Shock-proof operation overview

Shock-proof mode is the mode that realizes shock-proof operation using external DRAM. Shock-proof mode is invoked by setting MSON=H in microcontroller command 80H.

This mode comprises the following 3 sequences.

– Write sequence

1. Input data from a signal processor IC is read in.
2. Data read in is written to external DRAM in the sequence left-channel, (C2PO), and right-channel. (C2PO) is omitted in CDDA mode.

– Read sequence

1. Data written to external DRAM is read out at fs rate (rate 2fs in SVC mode).
2. Data is output in sync with the 24-bit bit clock (ZSCK).

– Compare-connect sequence

1. Encoding immediately stops when either external buffer RAM overflows or when a CD read error occurs due to shock vibrations.
2. Then, using microcontroller command 80H, the compare-connect start command is executed and compare-connect sequence starts.
3. Compares data re-read from the CD with the processed final valid data stored in RAM (confirms its correctness).
4. As soon as the comparison detects conforming data, compare-connect sequence stops and encode sequence re-starts, connecting the data directly behind previous valid data.

RAM addresses

The SM5906AF uses 4M or 16M DRAMs as external buffers.

Three kinds of addresses are used for external RAM control.

WA (write address)

RA (read address)

VWA (valid write address)

Among these, VWA is the write address for conforming data whose validity has been confirmed. Determination of the correctness of data read from the CD is delayed relative to the write processing, so VWA is always delayed relative to WA.

The region available for valid data is the area between VWA-RA.

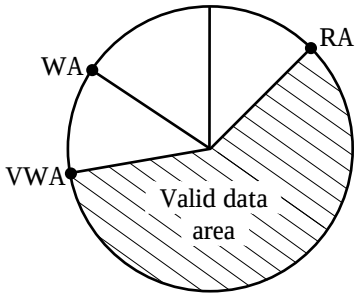


Fig 1. RAM addresses

VWA (valid write address)

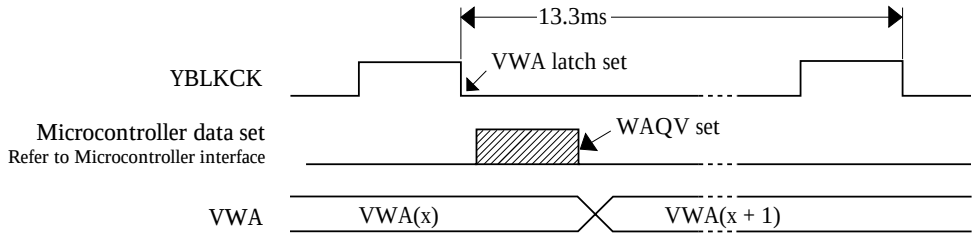
The VWA is determined according to the YBLKCK pin and WAQV command. Refer to the timing chart below.

1.YBLKCK is a 75 Hz clock(HIGH for 136 µs) when used for normal read mode and it is a 150 Hz clock when used for double-speed read mode, synchronized to the CD format block end timing. On the falling edge of this clock, stored compare-connect write address WA1 is promoted to WA2 and stored.(see note 1).

2.The microcontroller checks the subcode and, if confirmed to be correct, generates a WAQV command (80H).

3.When the WAQV command is received, the previously latched WA2 is stored as the VWA.

(Note 1) WA1, in VCD and SVC modes, is the DRAM write address of the last sync data input before the YBLKCK falling edge. In CDDA mode, update occurs in the same manner so that WA1 is updated every 588 data samples.



Values shown are for rate fs. The values are 1/2 those shown at rate 2fs.

Fig 2. YBLKCK and VWA relationship

YFLAG, FLAG6

Correct data demodulation becomes impossible for the CD signal processor IC when a disturbance exceeding the RAM jitter margin occurs. The YFLAG signal input pin is used to indicate when such a condition has occurred.

The IC checks the YFLAG input and stops the write sequence when such a disturbance has occurred, and then makes FLAG6 active.

The YFLAG check method used changes depending on the YFLGS flag (85H command).

(see table1)

85H command		FLAG6 set conditions	FLAG6 reset conditions
	YFLGS		
0	0	When YFLAG = LOW	– By status read (90H command)
1	1	When YFLAG = HIGH	– When MSON = LOW or after system reset

Table 1. YFLAG signal check method

Compare-connect sequence

In compare-connect mode, there are 6 connect modes: CDDA mode 3-pair compare-connect, 2-pair compare-connect and direct connect, plus VCD/SVC mode ASH connect (SYNC, HEADER), SH data connect (no C2PO check), and S connect (SYNC) modes.

– CD-DA mode

In 3-pair compare-connect mode, the final 6 valid data (3 pairs of left- and right-channel) and the most recently input data are compared until three continuous data pairs all conform. At this point, the write sequence is re-started and data is written to VWA.

In 2-pair compare-connect mode, comparison occurs just as for 3-pair comparison except that only 2 pairs from the three compared need to conform with the valid data. At this point, the write sequence is re-started and data is written to VWA.

In direct-connect mode, comparison is not performed at all, and write sequence starts and data is written to the VWA. This mode is for systems that cannot perform compare-connect operation.

– VCD, SVC mode

In ASH connect mode, the final 12 bytes of sync data in the valid data, 4 bytes of header data and the corresponding C2PO value are compared with new input data. If the data matches, the write sequence starts from the next data and connect occurs after the header data.

In SH connect mode, the compare occurs in the same manner as in ASH connect mode except the C2PO is not checked, even if it contains an error. If the data matches, the write sequence starts from the next data and connect occurs after the header data.

In S connect mode, the new data is compared with the sync data. If the data matches, the write sequence starts from the next data and connect occurs after the sync data. S connect mode can be used when other connections are not successful.

– Compare-connect preparation time

1. Comparison data preparation time

   Internally, when the compare-connect start command is issued, a sequence starts to restore the data for comparison. The time required for this preparation after receiving the command is approximately 1 × (1/fs). (approximately 23 μs when fs = 44.1 kHz)

2. After the above preparation is finished, data is input beginning from the left-channel data and comparison starts.
3. The same sequence takes place in direct-connect mode also. However, at the point when 3 words have been input, all data is directly connected as if comparison and conformance had taken place.

– Compare-connect sequence stop

If a compare-connect stop command (80H with MSDCN1= 1, MSDCN2= 0) is input from the microcontroller, compare-connect sequence stops.

If compare-connect sequence was not operating, the compare-connect stop command performs no operation. However, make sure that the other bit settings within the same 80H command are valid.

Write sequence temporary stop

– When RAM becomes full, MSWREN is set LOW using the 80H command and write sequence stops. (For details of the stop conditions, refer to the description of the WASQ flag.)

– Then, if MSWREN is set HIGH without issuing a compare-connect start command, the write sequence re-starts. At this time, new input data is written not to VWA, but to WA. In this way, the data already written to the region between VWA and WA is not lost.

– But if the MSWREN is set HIGH (80H command) after using the compare-connect start command even only once, data is written to VWA. If data is input before comparison and conformance is detected, the same operation as direct-connect mode takes place when the command is issued. After comparison and conformance are detected, no operation is performed because the write sequence has already been started. However, make sure that the other bit settings within the same 80H command are valid.

DRAM refresh

– DRAM initialization refresh

An 8-cycle RAS-only refresh is carried out for DRAM initialization under the following conditions.

When MSON changes from 0 to 1 using command 80H.

When from MSON=1, MSRDEN=0 and MSWREN=0 states only MSWREN changes to 1. In this case, write sequence immediately starts and initial data is written (at 2fs rate input) after a delay of 50µs.

– Refresh during Shock-proof mode operation

In this IC, a data access operation to any address also serves as a data refresh.

A data access to DRAM can occur in an write sequence write operation or in a read sequence read operation. Write sequence write operation stops during a connect operation whereas a read sequence read operation always continues while data is output to the D/A. The refresh rate for each DRAM during read sequence is shown in the table below.

The read sequence, set by MSON=1 and MSRDEN=1, operates when valid data is in DRAM (when MSEMP=0).

– When MSON=0, DRAM is not refreshed because no data is being accessed. Although MSON=1, DRAM is not refreshed if ENCOD=0 and DECOD=0 (both encode and decode sequence are stopped).

	DRAMs used	
Data compression mode	4M (1M×4 bits)	16M(4M×4 bits)
CDDA mode	2.91 ms	5.81 ms
VCD mode	2.58 ms	5.17 ms
SVC mode	1.29 ms	2.59 ms

Table 2. Read sequence refresh rate

– REFRESH flag (85H) refresh

In shock-proof mode, if operation momentarily stops (WRSQ and RDSQ stop), data in DRAM would be lost. In order to be able to use data in DRAM after such a stop, a refresh mode is provided that can refresh data, even during a momentary pause in operation.

1. In shock-proof mode, with WASQ and RASQ in an operating state, only WASQ stops if a stop command is issued (if WASQ is already in the stop state, then the stop command is not required).
2. Set the REFRESH flag HIGH using the 83H command. The outputs are then muted, and read operation also stops. The last read address RAL is stored.
3. At this point, RDSQ is operating and DRAM is being accessed without updating and DRAM data. The operation is similar to momentary stop operation because the outputs are muted. DRAM is repeatedly accessed using read addresses from RAL to VWA.
4. Set the REFRESH flat LOW using the 83H command to release the momentary stop command. At this point, the read address is restored to RAL and data read out starts from this address. Simultaneously, the output muting is also released.
5. When WRSQ starts, send the compare command, and writing starts from after the VWA. If this operation occurs when MSWREN is HIGH, the WA, VWA, and RA address relationship may be lost, resulting in incorrect operation.

Through-mode operation

If MSON is set LOW (80H command), an operating mode that does not perform shock-proof functions becomes active. In this case, input data is passed as-is (except Force mute operation) to the output. External DRAM is not accessed. Also, in through mode, the bit clock and CDDA and VCD mode (85H command) settings become valid. Note that SVC mode cannot be used in through mode, reverting to CDDA mode instead.

– In this case, input data needs to be at a rate fs and the input word clock must be synchronized to the CLK input (384fs). However, short-range jitter can be tolerated (jitter-free system).

– Jitter-free system timing starts from the first YLRCK rising edge after either (A) a reset (NRESET= 0) release by taking the reset input from LOW to HIGH or (B) by taking MSON from HIGH to LOW. Accordingly, to provide for the largest possible jitter margin, it is necessary that the YLRCK clock be at rate fs by the time jitter-free timing starts.

The jitter margin is 0.2/ fs (80 clock cycles).

This jitter margin is the allowable difference between the system clock (CLK) divided by 384 (fs rate clock) and the YLRCK input clock.

If the timing difference exceeds the jitter margin, irregular operation like data being output twice or, conversely, incomplete data output may occur. In the worst case, a click noise may also be generated.

When switching from shock-proof mode to through mode, an output noise may be generated, and it is therefore recommended to use the YDMUTE setting to mute ZSRDATA until just before data output.

– When NMSOFF = 1 (83H command), the YSCK, YSRDATA, YLRCK, YC2PO inputs are connected directly to the ZSCK, ZSRDATA, ZLRCK, ZC2PO outputs, respectively. When the connection is switched, the input clock and data pins are switched instantaneously to the output clock and data pins, so the outputs should be muted just prior to switching.

Force mute

Serial output data is muted by setting the YDMUTE pin input HIGH or by setting the MUTE flag to 1. Mute starts and finishes on the leading left-channel bit.

When MSON is HIGH and valid data is empty (MSEMP=H), the output is automatically forced into the mute state.

SYNC and Header data

Note that video CD sync and header data formats are appended.

Lch		Rch	
MSByte	LSByte	MSByte	LSByte
FF	00	FF	FF
FF	FF	FF	FF
FF	FF	00	FF
Minutes	Seconds	Frames	Mode
Successive data	Successive data	Successive data	Successive data

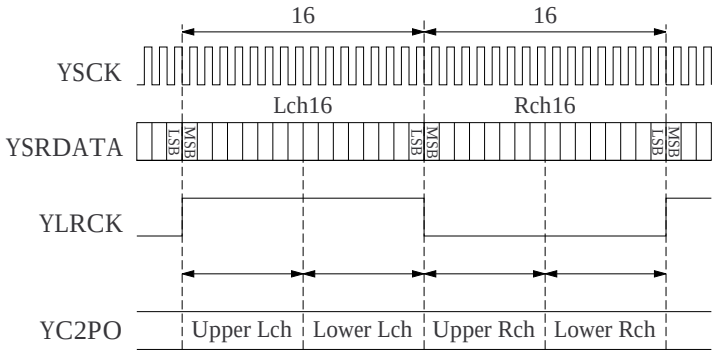
(1 cycle = 2352 bytes)

Table 3.

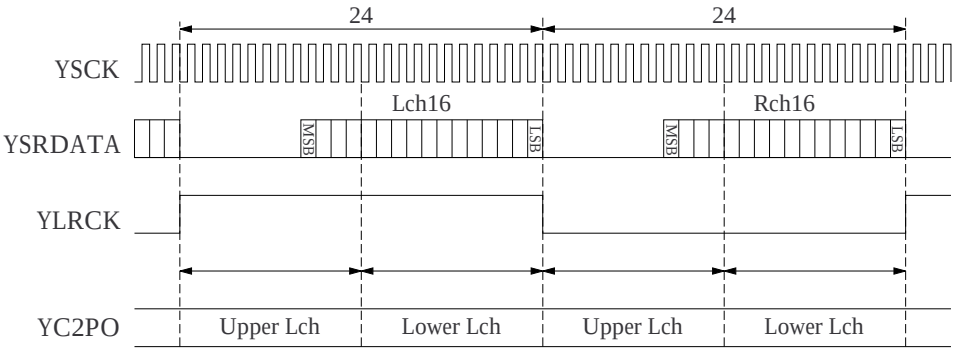
Timing charts

Input timing (YSCK, YSRDATA, YLRCK, YC2PO)

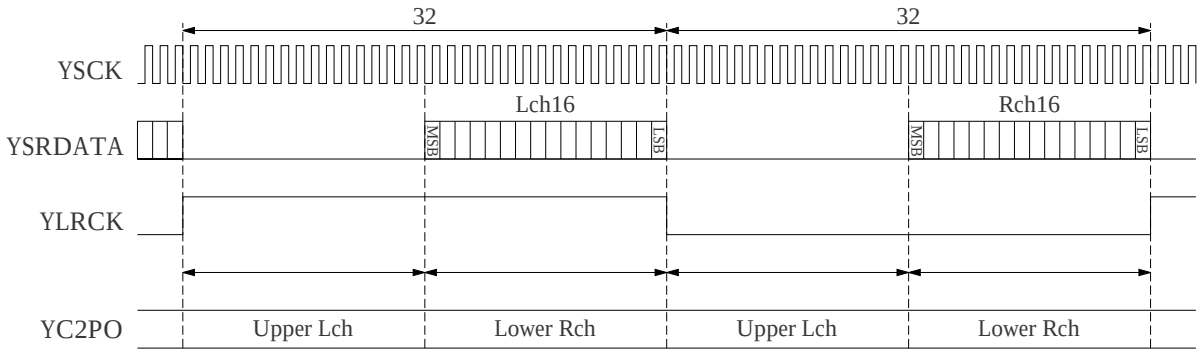
16-bit mode



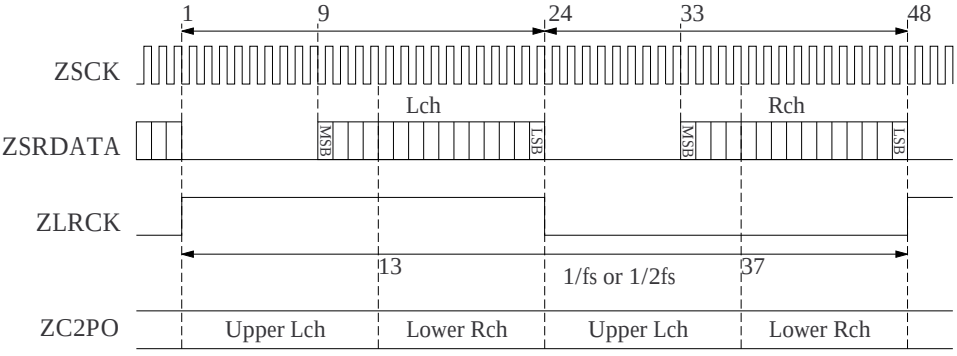
24-bit mode



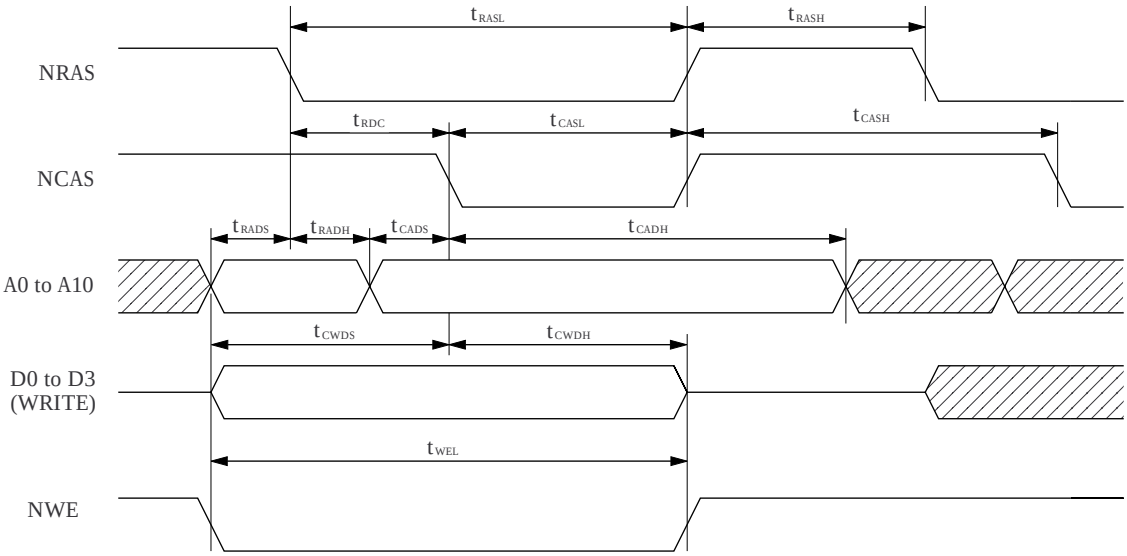
32-bit mode



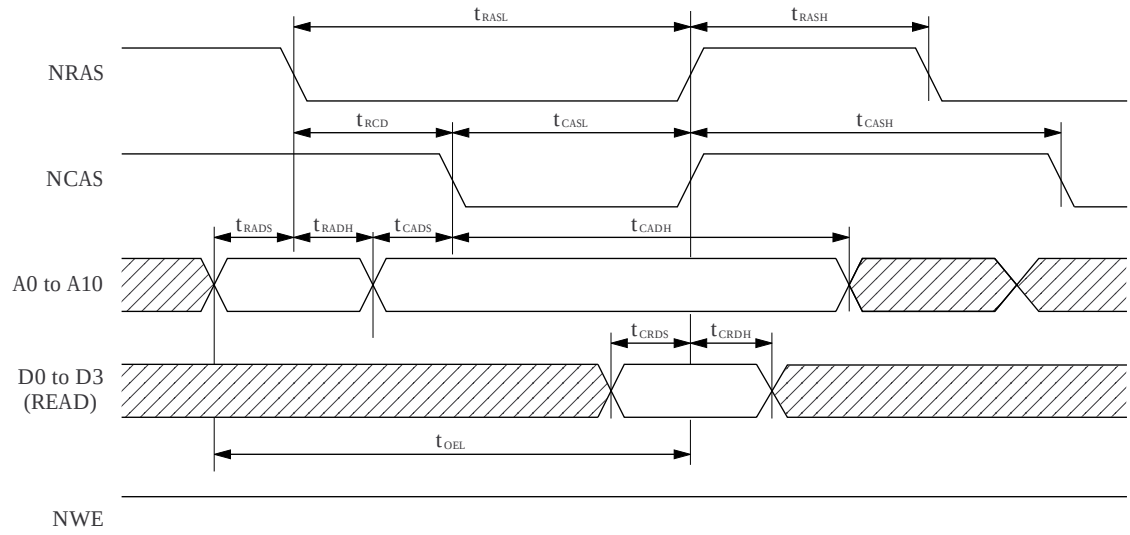
Output timing (ZSCK, ZSRDATA, ZLRCK, ZC2PO)



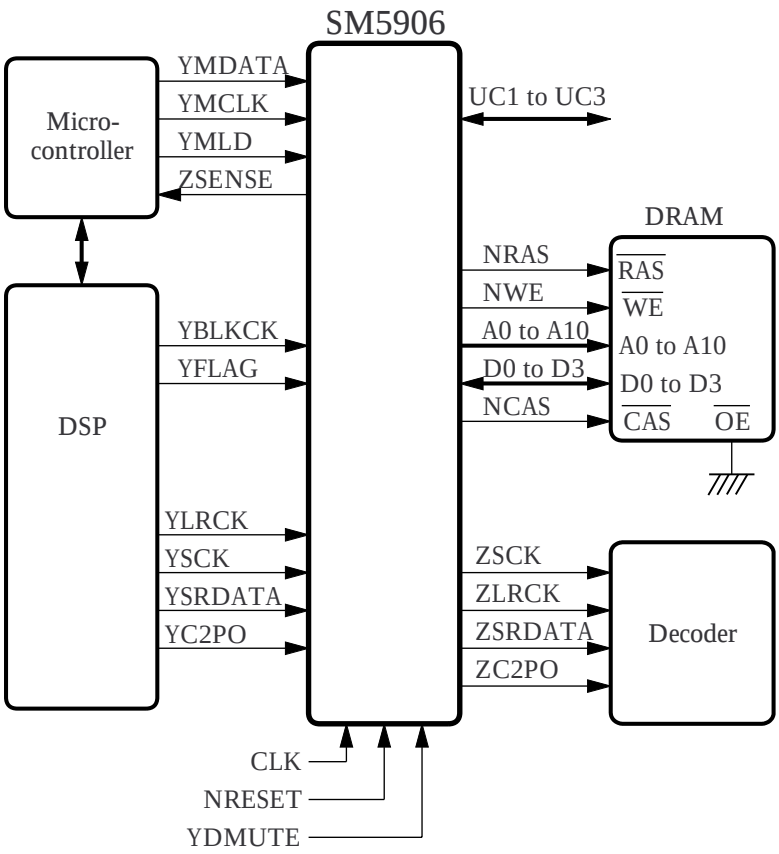
DRAM write timing (NRAS, NCAS, NWE, A0 to A10, D0 to D3)



DRAM read timing (NRAS, NCAS, NWE, A0 to A10, D0 to D3)



Connection example



note1

- When 2 DRAMs are used, the DRAM $\overline{OE}$ pins should be tied LOW.

NPC
NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, FUKUZUMI 2 CHOME, KOTO-KU
TOKYO,135-8430, JAPAN
Telephon: +81-3-3642-6661
Facsimile: +81-3-3642-6698

NC9901AE 1999.7