NIPPON PRECISION CIRCUITS INC.

SM5165AV

PLL Synthesizer IC

OVERVIEW

The SM5165AV is a PLL synthesizer IC developed for application in pagers and fabricated using NPC's Molybdenum-gate CMOS process. It incorporates independently-controlled reference frequency and operating frequency dividers, and operates from a low-voltage supply to realize low power dissipation.

FEATURES

- Up to 90 MHz operating frequency ($V_{DD1} = V_{DD2} = 0.95$ V)
- Up to 100 MHz operating frequency ($V_{DD1} = V_{DD2} = 1.00$ V)
- Supply voltages
  - $V_{DD1} = V_{DD2} = 0.95$ to 1.5 V (prescaler, counters)
  - $V_{DD3} = 2.0$ to 3.3 V (charge pump)
- 40 to 16376 reference frequency divider ratio range (with 1/8 prescaler built-in)
- 1056 to 262143 operating frequency divider ratio range
- Power-save function for reduced power dissipation
- –10 to 60 °C operating temperature range
- 16-pin VSOP
- Molybdenum-gate CMOS process

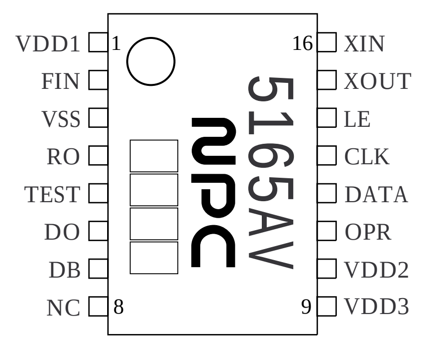
APPLICATIONS

- Pagers

ORDERING INFOMATION

Device	Package
SM5165AV	16pin VSOP

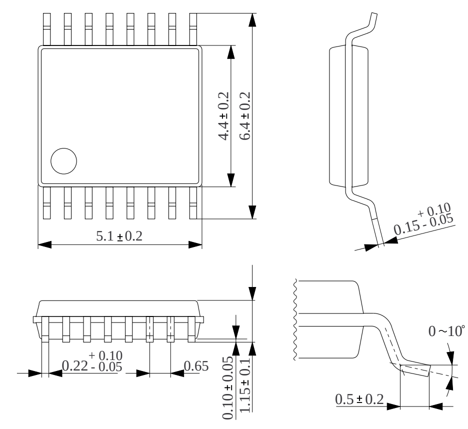
PINOUT(TOP VIEW)



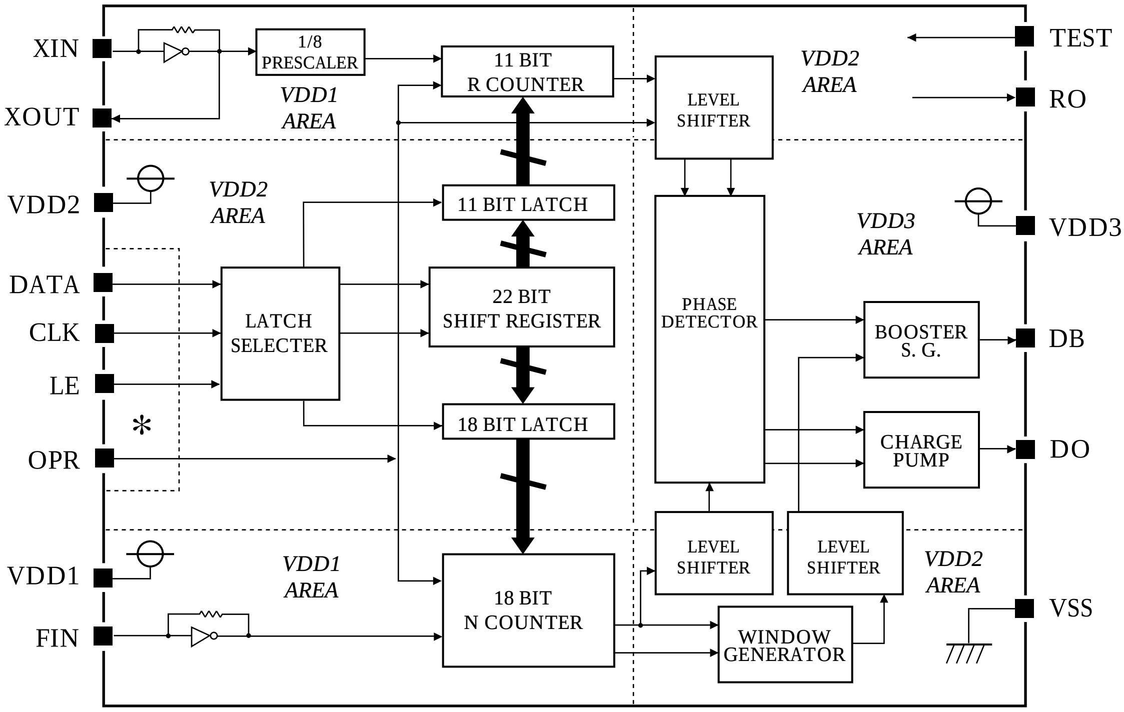
PACKAGE DIMENSIONS

Unit: mm

16-pin VSOP



BLOCK DIAGRAM



*Protection diodes are connected to VDD3. Logic level : VDD2 to VDD3

PIN DESCRIPTION

Number	Name	I/O	Description
1	VDD1	–	Reference frequency and comparator frequency prescaler and counter 1 V supply
2	FIN	I	Operating frequency divider input pin. Feedback resistor built-in for AC-coupled inputs.
3	VSS1	–	Ground pin
4	RO	O	Test output. LOW-level output for (1, 0) test bit patter. Leave open for normal operation.
5	TEST	I	Test pin. Pull-down resistor built-in. Leave open or connect to ground for normal operation.
6	DO	O	Phase detector output pin. Built-in charge pump and tristate output means that this output can be connected to a low-pass filter. The output polarity is preset for connection to a passive filter.
7	DB	O	Booster signal output for faster locking
8	NC	–	No connection
9	VDD3	–	Phase comparator, charge pump and booster signal 3 V supply
10	VDD2	–	Shift register and latch 1 V supply. Should be kept at the same potential as VDD1.
11	OPR	I	Power-save control pin. Operation when HIGH, standby mode when LOW.
12	DATA	I	Control data input pin
13	CLK	I	Control data clock input pin
14	LE	I	Control data latch enable signal input pin
15	XOUT	O	Reference frequency divider crystal oscillator connection pins. Alternatively, an external clock input can be connected to XIN. The clock is also output on XOUT. Feedback resistor built-in for AC-coupled inputs.
16	XIN	I	

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	$V_{DD1,2}$		–0.3 to 2.0	V
	V_{DD3}		–0.3 to 7.0	V
Input voltage range	V_{IN1}	FIN, XIN, TEST	V_{SS} – 0.3 to $V_{DD1,2}$ + 0.3	V
	V_{IN2}	OPR, CLK, DATA, LE	V_{SS} – 0.3 to V_{DD3} + 0.3	V
Storage temperature range	T_{stg}		–40 to 125	°C
Power dissipation	P_D		150	mW
Soldering temperature	T_{sld}		255	°C
Soldering time	t_{sld}		10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	$V_{DD1,2}$		0.95 to 1.5	V
	V_{DD3}		2.0 to 3.3	V
Storage temperature range	T_{stg}		–10 to 60	°C

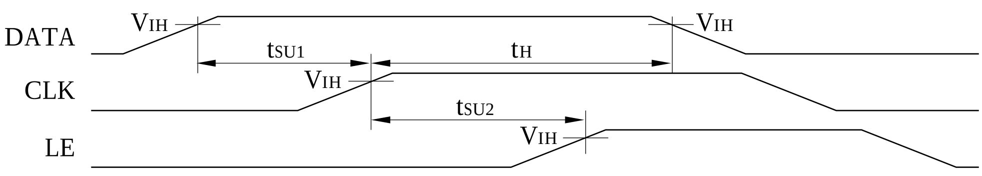
Electrical Characteristics

V_{SS} = 0 V, V_{DD1} = V_{DD2} = 0.95 to 1.5 V, V_{DD3} = 2.0 to 3.3 V, T_a = –10 to 60 °C

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
VDD1, VDD2 operating current consumption	I_{DD1}	Note 1.		–	0.70	1.10	mA
		Note 2.		–	0.75	1.20	
VDD3 operating current consumption	I_{DD2}			–	10	–	µA
VDD2 standby current	I_{DD3}	Note 3.		–	0.1	–	µA
VDD3 standby current	I_{DD4}			–	0.01	10.0	µA
FIN maximum operating input frequency	f_{max1}	300 mVp-p sine wave	$V_{DD1,2}$ = 0.95 to 1.50 V	90	–	–	MHz
			$V_{DD1,2}$ = 1.00 to 1.50 V	100	–	–	
XIN maximum operating input frequency	f_{max2}	300 mVp-p sine wave. Note 4.		16	–	–	MHz
FIN minimum operating input frequency	f_{min1}	300 mVp-p sine wave		–	–	40	MHz
XIN minimum operating input frequency	f_{min2}	300 mVp-p sine wave. Note 4.		–	–	9	MHz
FIN input amplitude	V_{FIN}	$V_{DD1,2}$ = 0.95 to 1.50 V, f_{FIN} = 90 MHz, AC coupling		0.3	–	–	Vp-p
		$V_{DD1,2}$ = 1.00 to 1.50 V, f_{FIN} = 100 MHz, AC coupling		0.3	–	–	
XIN input amplitude	V_{XIN}	f_{XIN} = 16 MHz, AC coupling		0.3	–	–	Vp-p
OPR, CLK, DATA, LE LOW-level input voltage	V_{IL}			–	–	$0.2V_{DD2}$	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
OPR, CLK, DATA, LE HIGH-level input voltage	V_{IH}		$0.8V_{DD2}$	–	V_{DD3}	V
FIN LOW-level input current	I_{IL1}	$V_{IL} = 0$ V	–	–	60	µA
XIN LOW-level input current	I_{IL2}		–	–	10	µA
FIN HIGH-level input current	I_{IH1}	$V_{IH} = V_{DD1}$	–	–	60	µA
XIN HIGH-level input current	I_{IH2}		–	–	10	µA
DO, DB LOW-level output current	I_{OL}	Note 5.	1.0	–	–	mA
DO, DB HIGH-level output current	I_{OH}	Note 6.	1.0	–	–	mA
Tristate output high-impedance leakage current	I_{OZL}	$V_{OL} = 0$ V	–	–	100	nA
	I_{OZH}	$V_{OH} = V_{DD3}$	–	–	100	nA
DATA → CLK setup time	t_{SU1}	Note 7.	2	–	–	µs
CLK → LE setup time	t_{SU2}		2	–	–	µs
Hold time	t_H		2	–	–	µs

1. $V_{DD1} = V_{DD2} = 0.95$ to 1.05 V, $V_{DD3} = 2.7$ to 3.3 V, $f_{FIN} = 90$ MHz (300 mVp-p sine wave), $f_{XIN} = 14.4$ MHz (300 mVp-p sine wave), OPR = HIGH, no output load
2. $V_{DD1} = V_{DD2} = 1.00$ to 1.05 V, $V_{DD3} = 2.7$ to 3.3 V, $f_{FIN} = 100$ MHz (300 mVp-p sine wave), $f_{XIN} = 14.4$ MHz (300 mVp-p sine wave), OPR = HIGH, no output load
3. $V_{DD1} = 0$ V, $V_{DD2} = 0.95$ to 1.05 V, $V_{DD3} = 2.7$ to 3.3 V, OPR = LOW, no input/output load (i.e. CLK = DATA = LE = 0 V)
4. Externally-input sine wave
5. DO and DB outputs are derived from the V_{DD3} supply. $V_{DD3} = 2.7$ to 3.3 V, $V_{OL} = 0.4$ V
6. DO and DB outputs are derived from the V_{DD3} supply. $V_{DD3} = 2.7$ to 3.3 V, $V_{OH} = V_{DD3} - 0.4$ V
7. Setup and hold times.



FUNCTIONAL DESCRIPTION

Operating Frequency Divider (N-counter) Structure

The operating frequency divider generates a comparator frequency signal (FV), which is input to the phase comparator, by dividing the VCO signal input on pin FIN.

The operating frequency divider is comprised by dual modulus prescalers, a 5-bit swallow counter and a 13-bit main counter.

The settings for the dual modulus prescaler (P and P + 1), swallow counter (S) and main counter (M) are related to the comparator frequency divider ratio by:

$$N = (P + 1) \times S + P(M - S)$$
$$= PM + S$$

The counter value ranges are P = 32, P + 1 = 33, S = 0 to 31, and M = 32 to 8191. Therefore, the comparator frequency divider ratio range N is 1056 to 262143.

Reference Frequency Divider (R-counter) Structure

The reference frequency divider generates a comparator frequency signal (FR), which is input to the phase comparator, by dividing the reference oscillator frequency input either from an external signal on XIN or from a crystal oscillator connected between XIN and XOUT.

The reference frequency divider is comprised by a fixed divide-by-8 prescaler and an 11-bit reference counter.

The settings for the prescaler (A = 8) and reference counter (R) are related to the reference frequency divider ratio by:

$$R = AB = 8B$$

The counter value ranges are A = 8 and B = 5 to 2047. Therefore, the reference frequency divider ratio range is R = 40 to 16376.

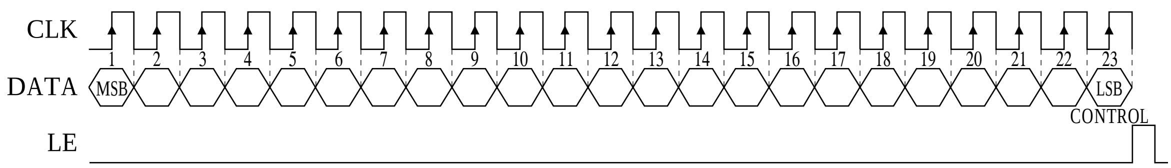
Input Data

The input data should be specified keeping in mind both the V_{DD2} and V_{DD3} supplies. The data is input using CLK, DATA and LE pins into the shift register and latch which operate from the V_{DD2} supply. However, the input voltages can be specified using either the V_{DD2} or V_{DD3} supply levels.

The control data input uses a 3-line 23-bit serial interface comprising the clock (CLK), data input (DATA) and latch enable (LE). The data is input with the MSB first. The last (23rd) bit is used as the latch select control bit. Data is written to the shift register on the rising edge of the clock signal. Accordingly, the data should change state on the falling edge of the clock signal. Data is transferred from the shift register to the latch when the latch enable (LE) signal goes HIGH. Accordingly, the latch enable signal should be held LOW while data is being written to the shift register.

The clock and data input signals are both ignored when the latch enable signal goes HIGH.

Input data format

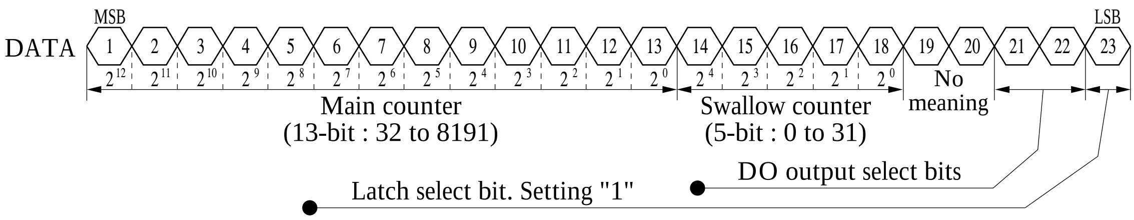


Latch select

The last (23rd) data bit determines the shift register data latch.

Bit 23	Latch
0	Reference frequency counter divider ratio data latch select
1	Swallow counter and main counter frequency divider ratio and DO output latch select

Swallow counter, main counter frequency divider data and DO output



Bits 19 and 20 have no meaning. These bits should be set to 0.

Bits 20 and 21 control the state of the DO output pin.

Bit 21	Bit 22	DO output
0	0	High impedance
1	0	
0	1	Normal operation
1	1	

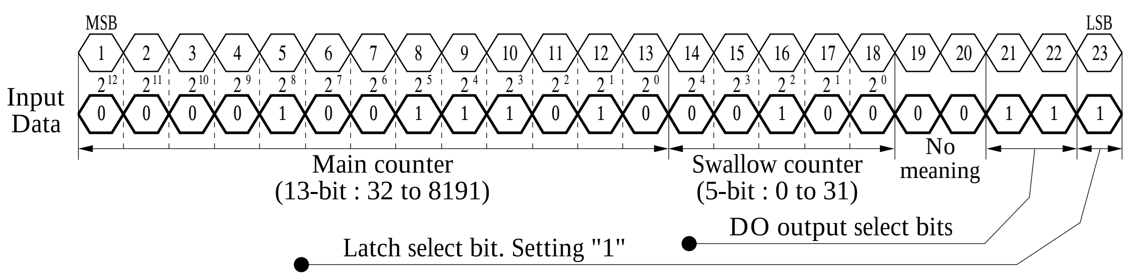
The DO output polarity can be set by master-slice for either a passive or active filter.

Input data example

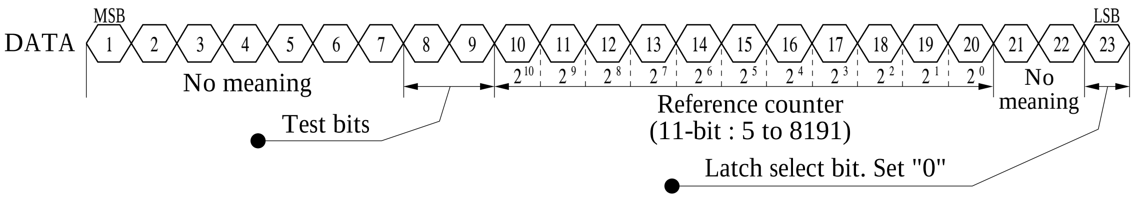
If the VCO output is (f_{VCO}) trebled, the output frequency (f_{LO}) is 251.3 MHz, and the channel bandwidth (f_{CH}: comparator frequency (f_R) × 3) is 25 kHz, then the comparator frequency divider ratio N is given by:

$$N = \frac{f_{LO}}{f_{CH}} = \frac{f_{VCO} \times 3}{f_R \times 3} = \frac{251.3/3}{0.025/3} = 10052 = 32 \times 314 + 4$$

Therefore, the swallow counter count is 4 $(00100)_2$ and the main counter count is 314 $(0000100111010)_2$.



Reference counter frequency divider setting



Bits 1 to 7 and bits 21 and 22 have no meaning. These bits should be set to 0.

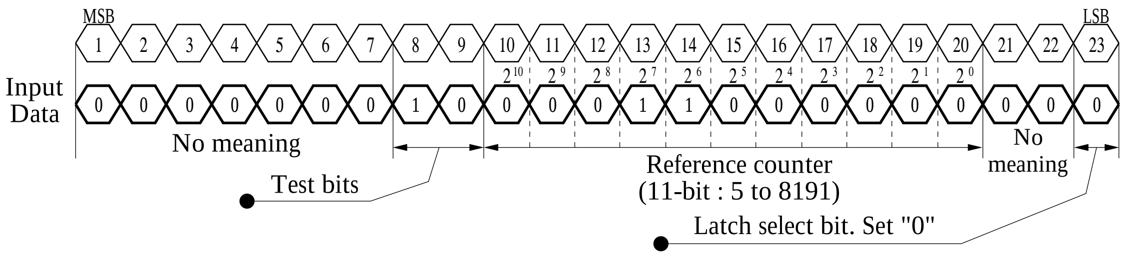
Bits 8 and 9 are used for testing at the manufacturers and should be set to 1 and 0, respectively, for normal operation.

Input data example

If the VCO output is (f_{VCO}) trebled, the crystal oscillator frequency is 12.8 MHz and the channel bandwidth (f_{CH}: comparator frequency (f_R) × 3) is 25 kHz, then the reference frequency divider ratio R is given by:

$$NR = \frac{Xtal}{f_{CH}} = \frac{Xtal}{f_R \times 3} = \frac{12.8}{0.025/3} = 1536 = 8 \times 192$$

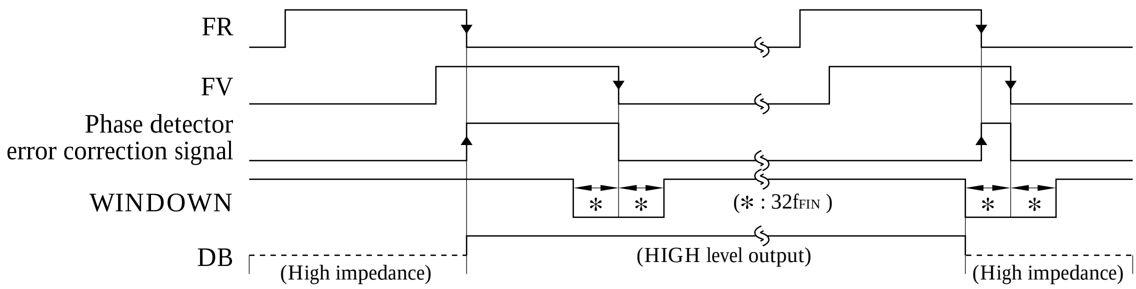
Therefore, the reference counter count is 192 $(00011000000)_2$.



Boost-up Signal

When the PLL starts up with some phase tolerance, a level signal is output on pin DB. When the PLL phase error comes within the tolerance before in lock, output DB goes high impedance.

When the PLL starts up, the signal on DB charges the low-pass filter capacitor in anticipation of high-speed locking. After the boost-up signal is output and the PLL phase error comes within tolerance, the boost-up circuit stops and operation continues when the 3 supplies (V_{DD1}, V_{DD2}) are applied and OPR goes HIGH once only. After the boost-up circuit stops, new data is written and the boost-up signal is not output even if the VCO is not in lock.



Operating principles

When the PLL is operating with a phase error within fixed tolerance, an internal WINDOWN signal is generated. This signal is in sync with the N counter output signal (FV) and is 62 cycles of the FIN input period in length centered about the falling edge of FV.

If the phase detector error correction signal occurs before the WINDOWN LOW-level pulse, the HIGH-level output from DB continues. However, if the error correction signal occurs wholly within the WINDOWN LOW-level pulsewidth, DB goes high impedance and the boost-up circuit operation stops.

The above description applies when the error correction signal is revising up. When the error correction signal is revising down, DB goes LOW.

Standby Mode

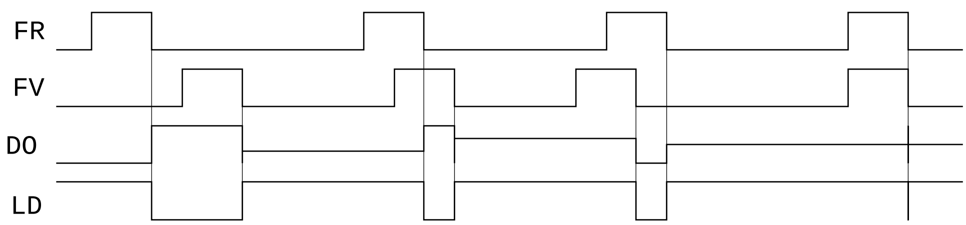
The SM5165AV enters standby mode when OPR goes LOW. In this mode, the following pin states and functions occur.

Function	State
Outputs DO and DB	Floating (high impedance)
Phase detector	Reset
Input FIN	Feedback resistor is cutoff (internal HIGH level)
Input XIN	Feedback resistor is cutoff (internal HIGH level)
N counter	Reset
R counter	Reset
Latch data	Stored

Note that even in standby mode, some current flows into VDD1 (FIN and XIN prescaler current). It is recommended that VDD1 be grounded in standby mode to reduce current consumption if necessary.

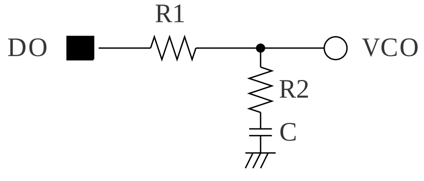
Note also that the above pin states and functions are only valid if V_{DD2} and V_{DD3} are maintained within normal operating conditions. If V_{DD2} and/or V_{DD3} are not within normal operating conditions, the latch data is not retained.

Phase Comparator Timing Diagram



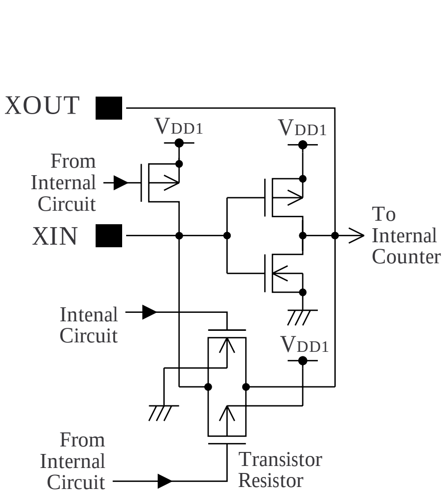
FV and FR are the internal comparator frequency divider output signal and reference frequency divider output signal, respectively.

Passive Low-pass Filter

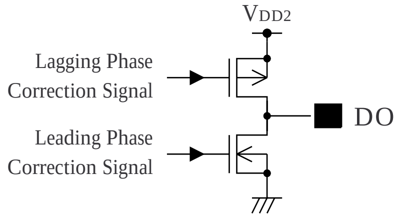


Input/Output Equivalent Circuits

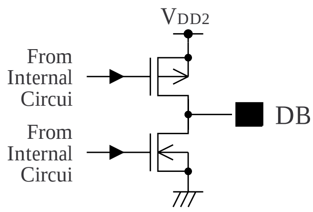
XIN, XOUT



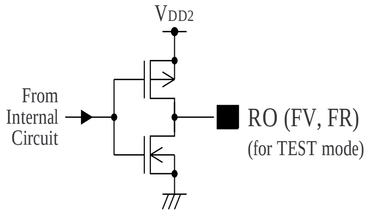
DO (for passive filter)



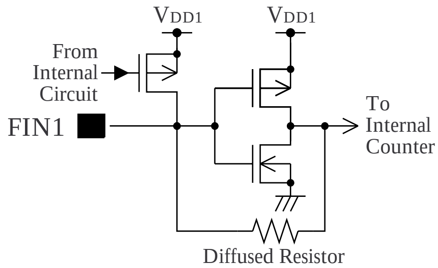
DB



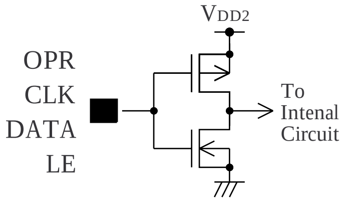
RO



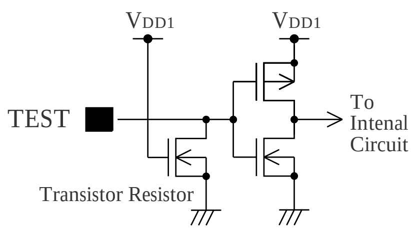
FIN



OPR, CLK, DATA, LE



TEST



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