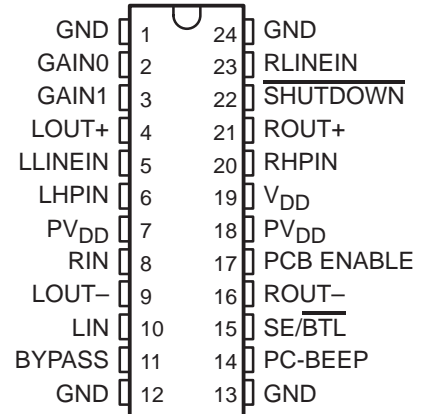


TPA0112 STEREO 2-W AUDIO POWER AMPLIFIER WITH FOUR SELECTABLE GAIN SETTINGS

SLOS204A – MAY 1999 – REVISED MAY 1999

- Compatible With PC 99 Desktop Line-Out Into 10-k Ω Load
- Internal Gain Control, Which Eliminates External Gain-Setting Resistors
- 2-W/Ch Output Power Into 3- Ω Load
- PC-Beep Input
- Depop Circuitry
- Stereo Input MUX
- Fully Differential Input
- Low Supply Current and Shutdown Current
- Surface-Mount Power Packaging
24-Pin TSSOP PowerPAD™

PWP PACKAGE
(TOP VIEW)



description

The TPA0112 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3- Ω loads. This device minimizes the number of external components needed, simplifying the design, and freeing up board space for other features. When driving 1 W into 8- Ω speakers, the TPA0112 has less than 0.8% THD+N across its specified frequency range.

Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is internally configured and controlled by way of two terminals (GAIN0 and GAIN1). BTL gain settings of 2, 6, 12, and 24 V/V are provided, while SE gain is always configured as 1 V/V for headphone drive. An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0112 automatically switches into SE mode when the SE/BTL input is activated, and this reduces the gain to 1 V/V.

The TPA0112 consumes only 6 mA of supply current during normal operation. A miserly shutdown mode is included that reduces the supply current to less than 150 μ A.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0112 to operate at full power into 8- Ω loads at an ambient temperature of 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

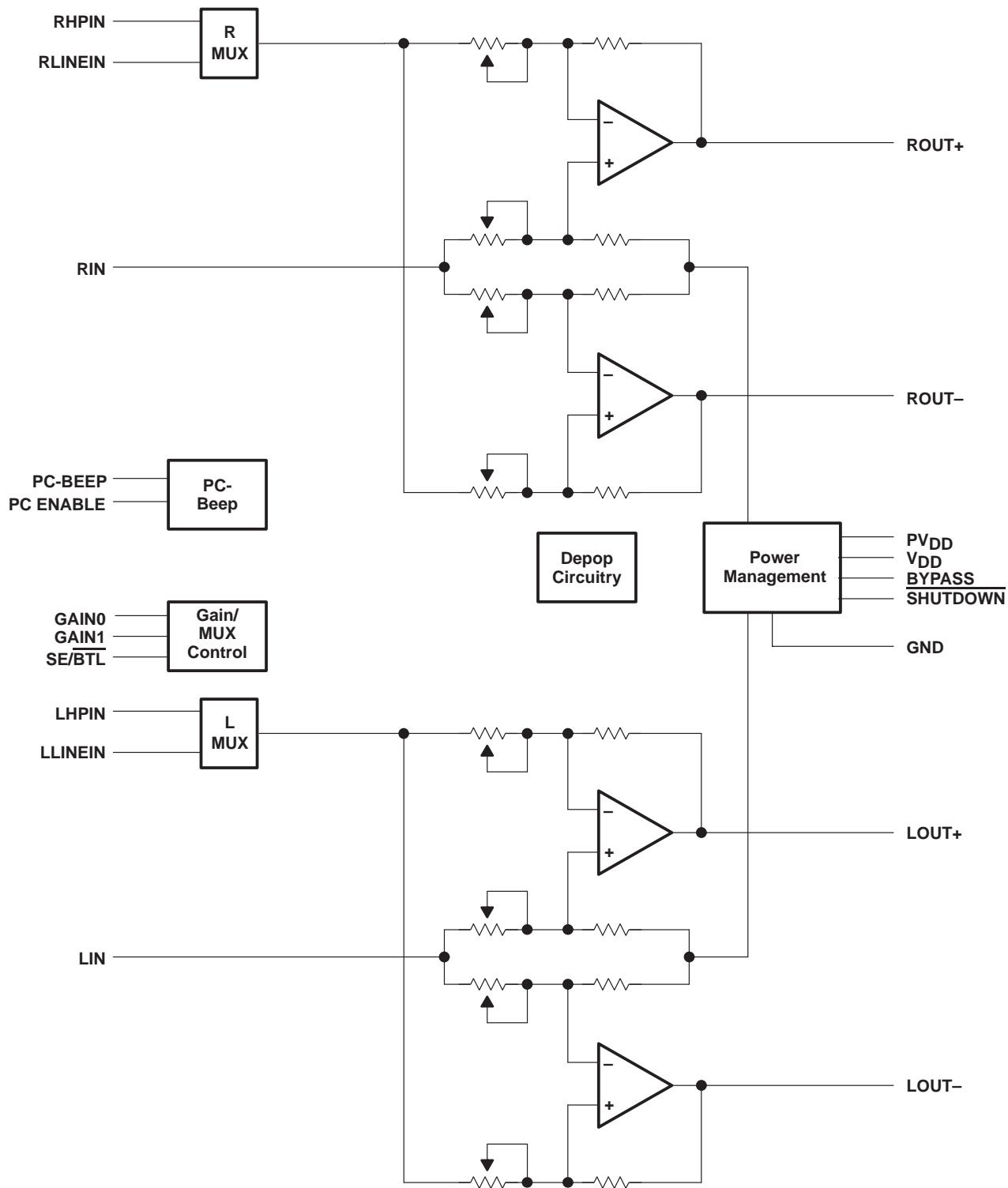
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functional block diagram



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AVAILABLE OPTIONS

T _A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0112PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0112PWPR).

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
GAIN0	2	I	Bit 0 of gain control
GAIN1	3	I	Bit 1 of gain control
GND	1, 12, 13, 24		Ground connection for circuitry. Connected to the thermal pad.
LHPIN	6	I	Left channel headphone input, selected when SE/BTL is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs.
LLINEIN	5	I	Left channel line input, selected when SE/BTL is held low
LOUT+	4	O	Left channel positive output in BTL mode and positive output in SE mode
LOUT–	9	O	Left channel negative output in BTL mode and high-impedance in SE mode
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
PCB ENABLE	17	I	If this terminal is high, the detection circuitry for PC-BEEP is overridden and passes PC-BEEP through the amplifier, regardless of its amplitude. If PCB ENABLE is floating or low, the amplifier continues to operate normally.
PVDD	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/BTL is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs.
RLINEIN	23	I	Right channel line input, selected when SE/BTL is held low
ROUT+	21	O	Right channel positive output in BTL mode and positive output in SE mode
ROUT–	16	O	Right channel negative output in BTL mode and high-impedance in SE mode
SHUTDOWN	22	I	Places entire IC in shutdown mode when held low, except PC-BEEP remains active
SE/BTL	15	I	Input MUX control input. When this terminal is held high, the LHPIN or RHPIN and SE output is selected. When this terminal is held low, the LLINEIN or RLINEIN and BTL output are selected.
VDD	19	I	Analog VDD input supply. This terminal needs to be isolated from PVDD to achieve highest performance.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD}	6 V
Input voltage, V_I	-0.3 V to $V_{DD} + 0.3$ V
Continuous total power dissipation	internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A	-40°C to 85°C
Operating junction temperature range, T_J	-40°C to 150°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$
PWP	2.7 W§	21.8 mW/°C	1.7 W	1.4 W

§ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/BTL	4		V
	SHUTDOWN	2		
Low-level input voltage, V_{IL}	SE/BTL	3		V
	SHUTDOWN	0.8		
Operating free-air temperature, T_A		-40	85	°C



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OD} $	Differential output voltage				25	mV
PSRR	Power supply rejection ratio	$V_{DD} = 4\text{ V to }5\text{ V}$		77		dB
$ I_{IH} $	High-level input current	$V_{DD} = 5.5\text{ V}$, $V_I = V_{DD}$			900	nA
$ I_{IL} $	Low-level input current	$V_{DD} = 5.5\text{ V}$, $V_I = 0\text{ V}$			900	nA
I_{DD}	Supply current	BTL mode		6	8	mA
		SE mode		3	4	
$I_{DD(sd)}$	Supply current, shutdown mode			150	300	μA

operating characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 8\ \Omega$, Gain = -2 V/V , BTL mode

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%, $R_L = 4\ \Omega$	$f = 1\text{ kHz}$,		1.9		W
THD + N	Total harmonic distortion plus noise	$P_O = 1\text{ W}$,	$f = 20\text{ Hz to }15\text{ kHz}$		0.75%		
BOM	Maximum output power bandwidth	THD = 5%			>15		kHz
k_{SVR}	Supply ripple rejection ratio	$f = 1\text{ kHz}$, $C_B = 0.47\ \mu\text{F}$	BTL mode		68		dB
SNR	Signal-to-noise ratio				105		dB
V_n	Noise output voltage	$C_B = 0.47\ \mu\text{F}$, $f = 20\text{ Hz to }20\text{ kHz}$	BTL mode		16		$\mu\text{V RMS}$
			SE mode		30		

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APPLICATION INFORMATION

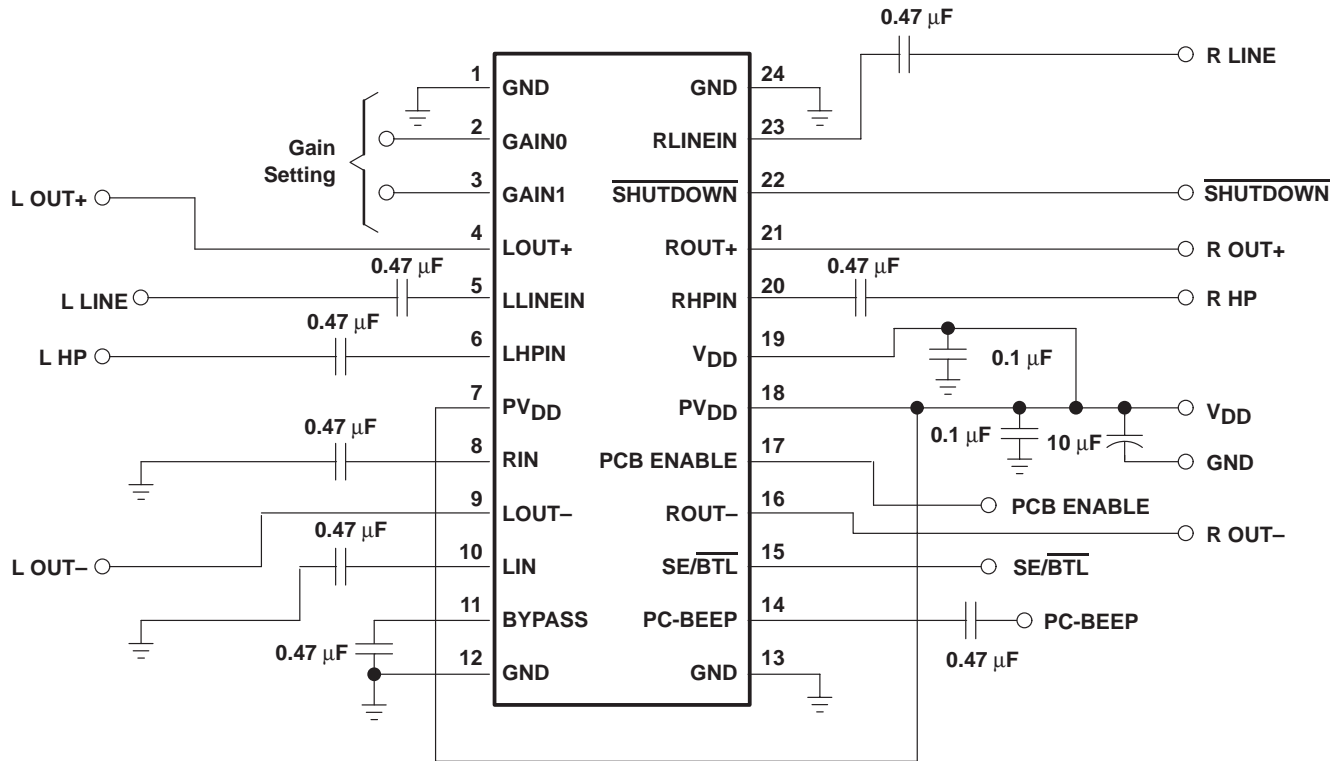


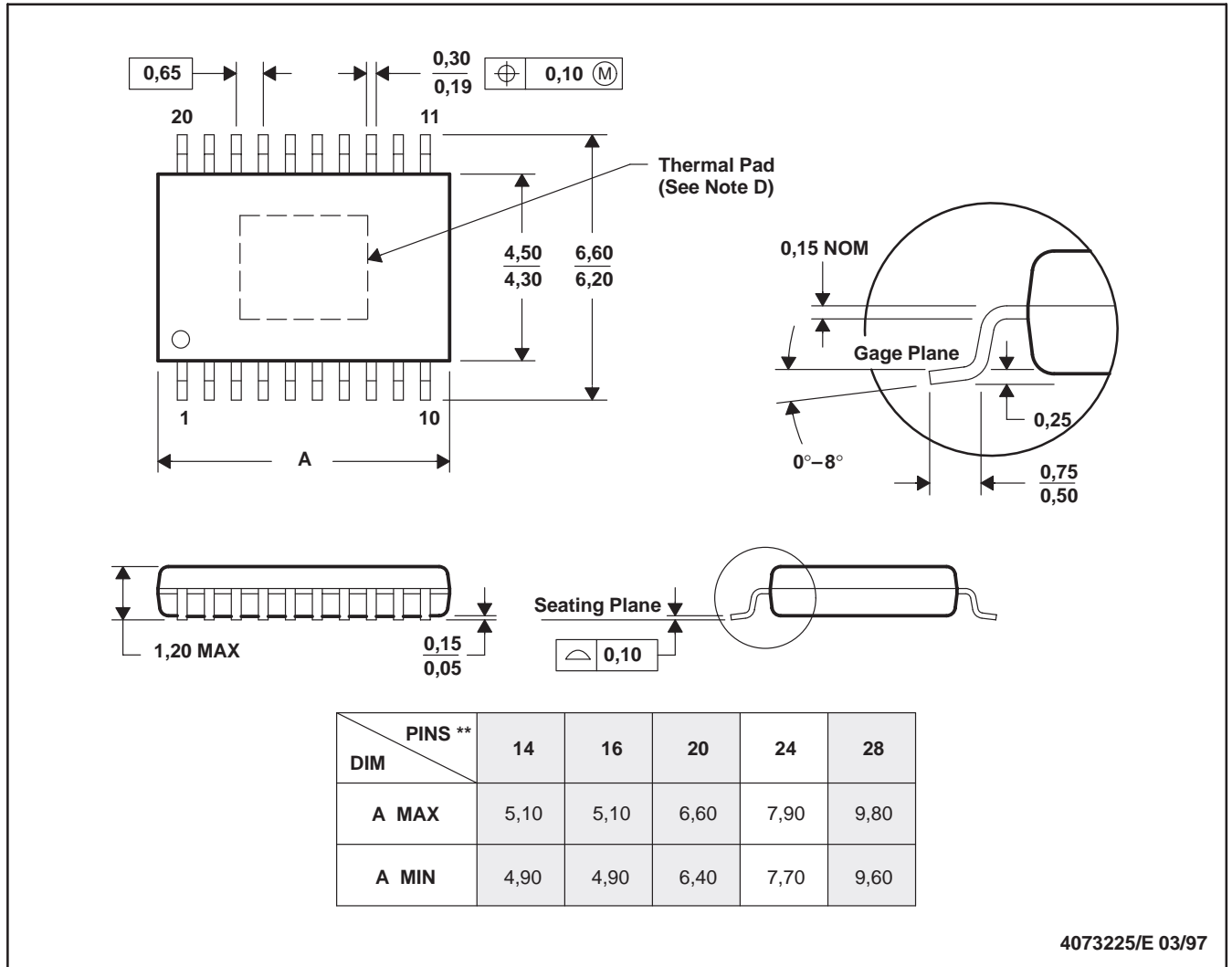
Figure 1. Typical TPA0112 Application Circuit

MECHANICAL DATA

PWP (R-PDSO-G)**

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20-PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusions.
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 E. Falls within JEDEC MO-153

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