TOPAZ SEMICONDUCTOR

SD5400, SD5401, SD5402

QUAD D-MOS FET ANALOG SWITCH ARRAYS

ORDERING INFORMATION

14 Pin Plastic, Small-Outline Package	SD5400CY	SD5401CY	SD5402CY
Description	20V, 30Ω	10V, 30Ω	15V, 30Ω
Temperature Range	Commercial	Commercial	Commercial

FEATURES

- Low Interelectrode Capacitances
  Analog Input—3.5pF typ.
  Input (Gate) —2.4pF typ.
  Output —1.3pF typ.
  Feedback —0.3pF typ.
- Low Insertion Loss, r_{DS} <30 ohms
- Low Crosstalk——107dB @ 3KHz
- Bidirectional Switches
- Small-Outline Surface Mount Package

APPLICATIONS

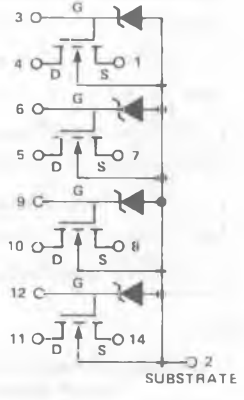
- High Speed Analog Switches
  Analog Range ± 10V—SD5400
  Analog Range ±7.5V—SD5402
  Analog Range ±5.0V—SD5401
- High-Speed Switch Drivers
  20V—SD5400
  15V—SD5402
  10V—SD5401
- Sample & Hold

ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

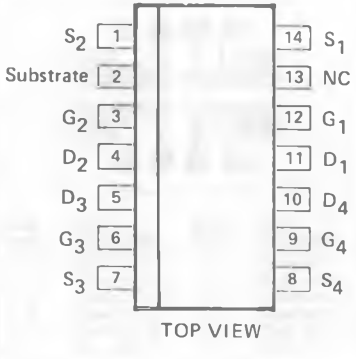
PARAMETER	SD5400	SD5401	SD5402	UNITS
V_{DS}	+20	+10	+15	V
V_{SD}	+20	+10	+15	V
V_{DB}	+25	+15	+22.5	V
V_{SB}	+25	+15	+22.5	V
V_{GS}	−25	−15	−22.5	V
	+30	+25	+30	V
V_{GB}	−0.3	−0.3	−0.3	V
	+30	+25	+30	V
V_{GD}	−25	−15	−22.5	V
	+30	+25	+30	V

I_D Continuous Drain Current 50mA
P_D Total Package Power Dissipation
(at or below T_A = +25°C) 640mW
Linear Derating Factor ..... 5.33mW/°C
P_D Single Device Power Dissipation
(at or below T_A = +25°C) 300mW
T_J Operating Junction
Temperature Range ..... 0 to +70°C
T_S Storage Temperature Range ..... −55 to +125°C

SCHEMATIC DIAGRAM



PIN CONFIGURATION



PACKAGE DIMENSIONS

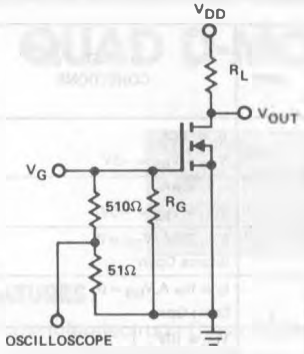
SO-14

(See Package 20)

ELECTRICAL CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise noted)

#		PARAMETER		SD5400			SD5401			SD5402			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	20	25		10	25		15	25		V	I_D = 10nA $V_{GS} = V_{BS} = -5V$	
2		BV_{SD}	Source-Drain Breakdown Voltage	20			10			15			V	I_S = 10nA $V_{GD} = V_{BD} = -5V$	
3		BV_{DB}	Drain-Substrate Breakdown Voltage	25			15			22.5			V	I_D = 10nA, V_{GB} = 0 Source Open	
4		BV_{SB}	Source-Substrate Breakdown Voltage	25			15			22.5			V	I_S = 10μ A, V_{GB} = 0 Drain Open	
5		$I_{D(off)}$	Drain-Source Off Current						10				nA	V_{DS} = 10V	$V_{GS} = V_{BS} = -5V$
6												10	nA	V_{DS} = 15V	
7						10							nA	V_{DS} = 20V	
8		$I_{S(off)}$	Source-Drain OFF Current						10				nA	V_{SD} = 10V	$V_{GD} = V_{BD} = -5V$
9												10	nA	V_{SD} = 15V	
10						10							nA	V_{SD} = 20V	
11		I_{GBS}	Gate-Body Leakage Current						1.0				μ A	V_{GB} = 25V	$V_{DB} = V_{SB} = 0$
12						1.0						1.0		V_{GB} = 30V	
13		$V_{GS(th)}$	Gate Threshold Voltage	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V	$V_{DS} = V_{GS}$, I_D = 1μ A V_{SB} = 0	
14		$r_{DS(on)}$	Drain-Source ON Resistance		50	70		50	70		50	70	ohms	V_{GS} = 5V	I_D = 1mA V_{SB} = 0
15					30			30			30			V_{GS} = 10V	
16					23			23			23			V_{GS} = 15V	
17					19			19			19			V_{GS} = 20V	
18		r_{DSM}	ON Resistance Match		1.0	5.0		1.0	5.0		1.0	5.0		V_{GS} = 5V	
19	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	V_{DS} = 10V, I_D = 20mA f = 1KHz, VSB = 0	
20		$C_{(gs + gd + gb)}$	Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5	pF	V_{DS} = 10V $V_{GS} = V_{BS} = -15V$ f = 1MHz	
21		$C_{(gs + db)}$	Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5			
22		$C_{(gs + sb)}$	Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0			
23		$C_{(dg)}$	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		0.3	0.5			
24		C_T	Cross Talk		−107			−107			−107		dB	f = 3KHz, R_G = 600Ω	
25		$t_{d(on)}$	Turn ON Delay Time		0.7	1.0		0.7	1.0		0.7	1.0	nSec	V_{DD} = 5V, $V_{G(on)}$ = 10V R_L = 680Ω, R_G = 51Ω	
26		t_r	Rise Time		0.8	1.0		0.8	1.0		0.8	1.0			
27		t_{off}	Turn OFF Time		10			10			10				

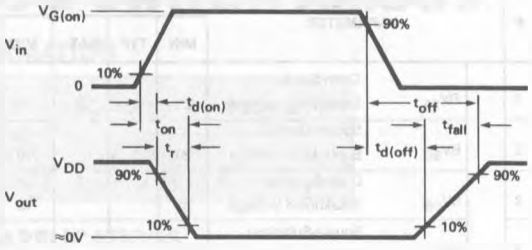
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
$t_r \leq 0.5$ nSEC
PULSE WIDTH – 100 nSEC

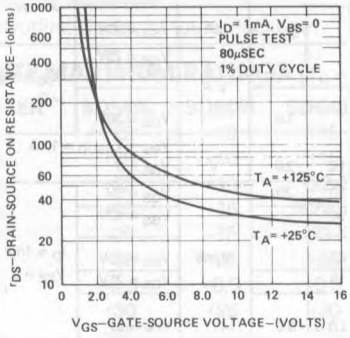
SAMPLING OSCILLOSCOPE
$t_r < 0.38$ nSEC
$R_{in} > 1M\Omega$
$C_{in} < 2.0$ pF

TEST WAVEFORMS

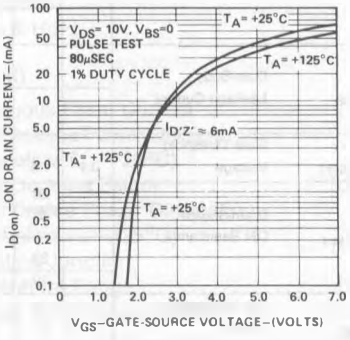


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise specified)

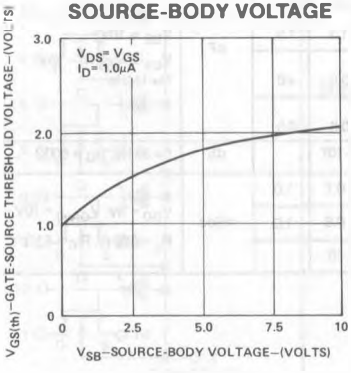
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



GATE-SOURCE THRESHOLD VOLTAGE —vs— SOURCE-BODY VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT