DATA SHEET

SAB9080
NTSC Picture-In-Picture (PIP) controller

Preliminary specification
File under Integrated Circuits, IC02

1999 Jan 05

Philips
Semiconductors

PHILIPS

NTSC Picture-In-Picture (PIP) controller SAB9080

FEATURES

- Double window PIP in interlaced mode at 8-bit resolution
- Internal DRAM of 1 Mbit
- Three 8-bit Analog-to-Digital Converters (ADCs) (7-bit performance) with clamp circuit for each acquisition channel
- One PLL which generates the line-locked clocks for the subchannel
- One PLL which generates the line-locked clocks for the main and display channel
- Three 8-bit Digital-to-Analog Converters (DACs)
- Linear zoom in both horizontal and vertical direction for the subchannel
- Linear zoom in horizontal direction for the main channel.

GENERAL DESCRIPTION

The SAB9080 is an NTSC Picture-in-Picture controller which can be used in double window applications.

It inserts one or two live video signals with reduced size into another live video signal. The incoming video signals are expected to be analog baseband signals.
The conversion into the digital environment is done on chip with ADCs. Processing and storage of the video data is done entirely in the digital domain. The conversion back to the analog domain is done by means of DACs. Internal clocks are generated by PLLs which lock on to the applied horizontal and vertical syncs.

The main input channel is compressed horizontally with a factor of 2 and directly fed to the output. After compressing a horizontal expansion of 2 is possible for the main channel.

The subchannel is also compressed horizontally with a factor of 2 but stored in memory before it is fed to the outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current		tbf	65	tbf	mA
I_{DDA}	analog supply current		tbf	185	tbf	mA
PLL						
f_{sys}	system frequency	1792 × HSYNC	–	28	–	MHz
B_{loop}	loop bandwidth		–	4	–	kHz
t_{jitter}	short term stability	jitter during 64 μs	–	–	4	ns
ζ	damping factor		–	0.7	–	

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAB9080	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

BLOCK DIAGRAM

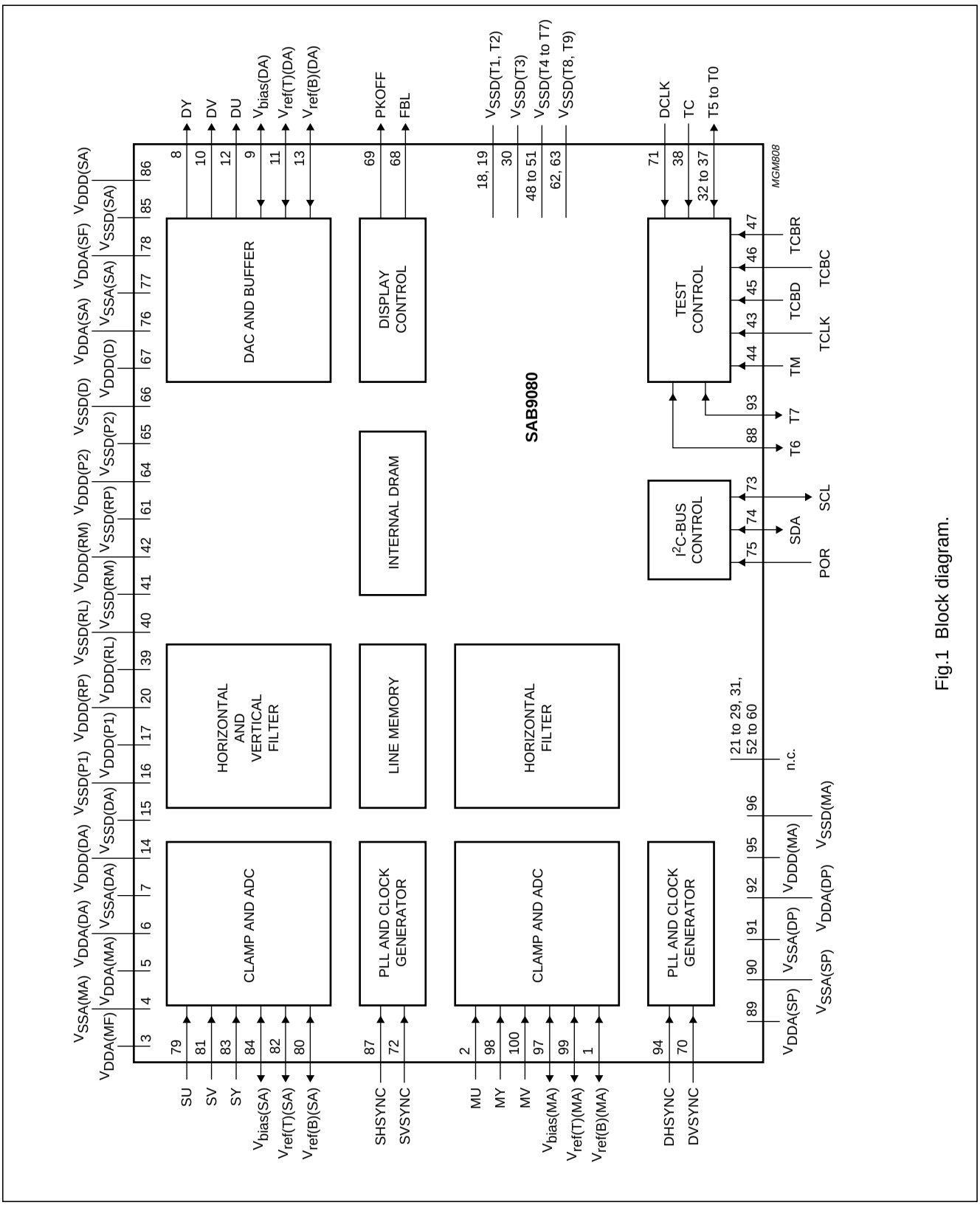


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
$V_{ref(B)(MA)}$	1	I/O	analog bottom reference voltage for main channel ADCs
MU	2	I	analog U input for main channel
$V_{DDA(MF)}$	3	S	analog supply voltage for main channel front-end buffers
$V_{SSA(MA)}$	4	S	analog ground for main channel ADCs
$V_{DDA(MA)}$	5	S	analog supply voltage for main channel ADCs
$V_{DDA(DA)}$	6	S	analog supply voltage for DACs
$V_{SSA(DA)}$	7	S	analog ground for DACs
DY	8	O	analog Y output of DAC
$V_{bias(DA)}$	9	I/O	input/output analog bias voltage reference for DACs
DV	10	O	analog V output of DAC
$V_{ref(T)(DA)}$	11	I/O	input/output analog top reference voltage for DACs
DU	12	O	analog U output of DAC
$V_{ref(B)(DA)}$	13	I/O	analog bottom reference voltage for DACs
$V_{DDD(DA)}$	14	S	digital supply voltage for DACs
$V_{SSD(DA)}$	15	S	digital ground for DACs
$V_{SSD(P1)}$	16	S	digital ground for periphery
$V_{DDD(P1)}$	17	S	digital supply voltage for periphery
$V_{SSD(T1)}$	18	–	digital ground for test
$V_{SSD(T2)}$	19	–	digital ground for test
$V_{DDD(RP)}$	20	S	digital supply voltage for memory periphery
n.c.	21 to 29	–	not connected
$V_{SSD(T3)}$	30	–	digital ground for test
n.c.	31	–	not connected
T5	32	I/O	test data input/output bit 5 (CMOS levels)
T4	33	I/O	test data input/output bit 4 (CMOS levels)
T3	34	I/O	test data input/output bit 3 (CMOS levels)
T2	35	I/O	test data input/output bit 2 (CMOS levels)
T1	36	I/O	test data input/output bit 1 (CMOS levels)
T0	37	I/O	test data input/output bit 0 (CMOS levels)
TC	38	I	test control input (CMOS levels)
$V_{DDD(RL)}$	39	S	digital supply voltage for memory logic
$V_{SSD(RL)}$	40	S	digital ground for memory logic
$V_{SSD(RM)}$	41	S	digital ground for memory core
$V_{DDD(RM)}$	42	S	digital supply voltage for memory core
TCLK	43	I	test clock input (CMOS levels)
TM	44	I	test mode input (CMOS levels)
TCBD	45	I	test control block data input (CMOS levels)
TCBC	46	I	test control block clock input (CMOS levels)
TCBR	47	I	test control block reset input (CMOS levels)
$V_{SSD(T4-T7)}$	48 to 51	–	digital ground for test

SYMBOL	PIN	I/O	DESCRIPTION
n.c.	52 to 60	–	not connected
$V_{SSD(RP)}$	61	S	digital ground for memory periphery
$V_{SSD(T8,T9)}$	62 and 63	–	digital ground for test
$V_{DDD(P2)}$	64	S	digital supply voltage for periphery
$V_{SSD(P2)}$	65	S	digital ground for periphery
$V_{SSD(D)}$	66	S	digital ground for digital core
$V_{DDD(D)}$	67	S	digital supply voltage for digital core
FBL	68	O	fast blanking control signal output (CMOS levels; +5 V tolerant)
PKOFF	69	O	peak off control signal output (CMOS levels; +5 V tolerant)
DVSYNC	70	I	vertical sync display channel input (CMOS levels; +5 V tolerant)
DCLK	71	I	test clock input (28 MHz) (CMOS levels)
SVSYNC	72	I	vertical sync for subchannel input (CMOS levels; +5 V tolerant)
SCL	73	I/O	input/output serial clock (I^2C-bus) (CMOS levels; +5 V tolerant)
SDA	74	I/O	input/output serial data/acknowledge output (I^2C-bus) (+5 V tolerant)
POR	75	I	power-on reset input (CMOS levels; pull-up resistor connected to V_{DD})
$V_{DDA(SA)}$	76	S	analog supply voltage for subchannel ADCs
$V_{SSA(SA)}$	77	S	analog ground for subchannel ADCs
$V_{DDA(SF)}$	78	S	analog supply voltage for subchannel front-end buffers and clamps
SU	79	I	analog U input for subchannel
$V_{ref(B)(SA)}$	80	I/O	input/output analog bottom reference voltage for subchannel ADCs
SV	81	I	analog V input for subchannel
$V_{ref(T)(SA)}$	82	I/O	input/output analog top reference voltage for subchannel ADCs
SY	83	I	analog Y input for subchannel
$V_{bias(SA)}$	84	I/O	analog bias reference voltage for subchannel ADCs
$V_{SSD(SA)}$	85	S	digital ground for subchannel ADCs
$V_{DDD(SA)}$	86	S	digital supply voltage for subchannel ADCs
SHSYNC	87	I	horizontal sync input for subchannel ($V_i < V_{SHSYNC}$)
T6	88	I/O	test data input/output bit 7 (CMOS levels)
$V_{DDA(SP)}$	89	S	analog supply voltage for subchannel PLL
$V_{SSA(SP)}$	90	S	analog ground for subchannel PLL
$V_{SSA(DP)}$	91	S	analog ground for display channel PLL
$V_{DDA(DP)}$	92	S	analog supply voltage for display channel PLL
T7	93	I/O	test data input/output bit 6 (CMOS levels)
DHSYNC	94	I	horizontal sync display input for channel ($V_i < V_{DHSYNC}$)
$V_{DDD(MA)}$	95	S	digital supply voltage for main channel ADCs
$V_{SSD(MA)}$	96	S	digital ground for main channel ADCs
$V_{bias(MA)}$	97	I/O	analog bias reference voltage for main channel ADCs
MY	98	I	analog Y input for main channel
$V_{ref(T)(MA)}$	99	I/O	analog top reference voltage for main channel ADCs
MV	100	I	analog V input for main channel

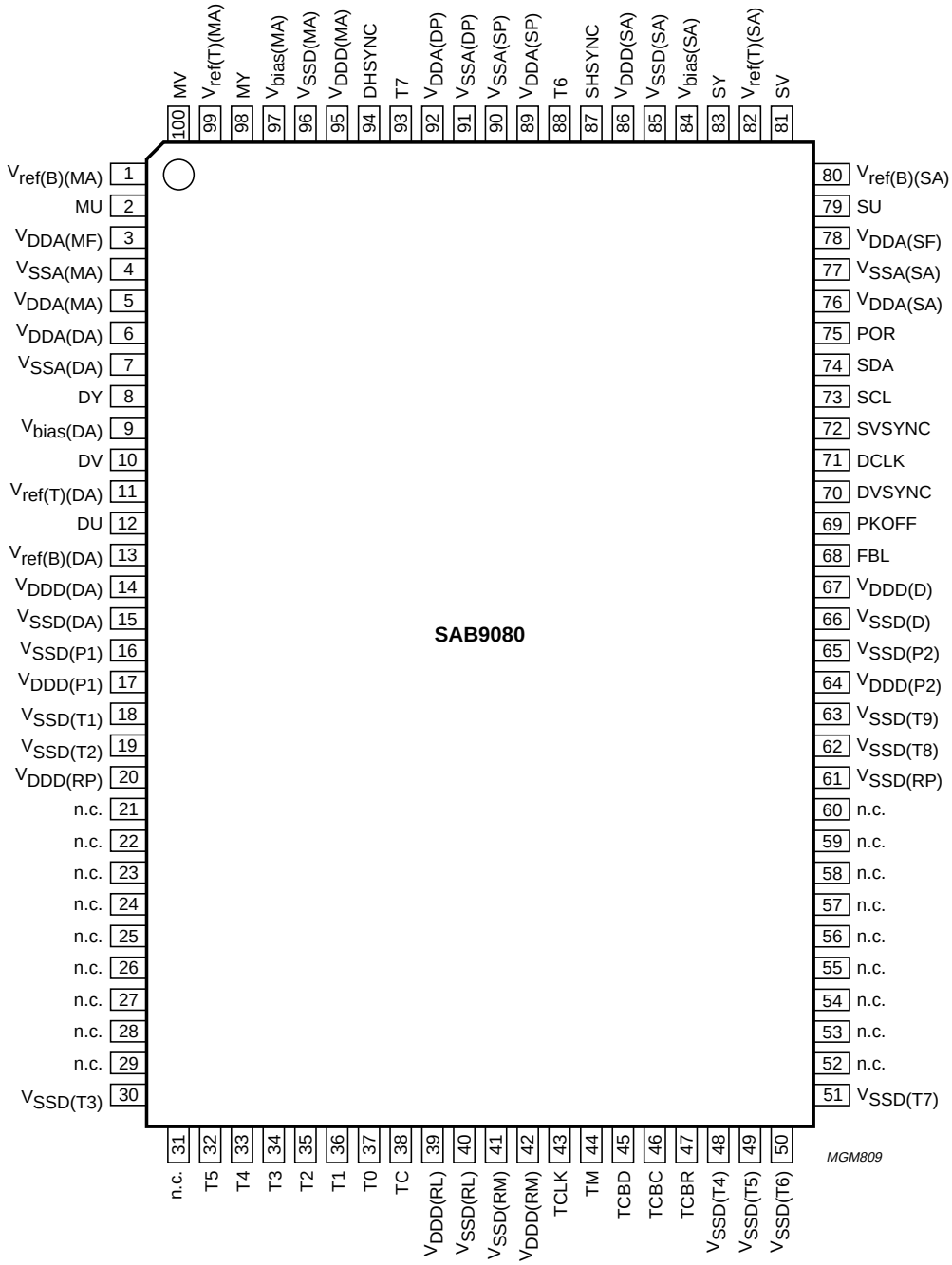


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Acquisition

The internal pixel rate is 28 MHz for the Y, U and V channels. It is expected that the bandwidth of the input signals is limited to 4.5 MHz for the Y input and 1.125 MHz for the U and V input. Inset synchronization is achieved via the acquisition SHSYNC and SVSYNC pins. With the acquisition fine positioning added to a system constant the starting point of the acquisition can be controlled. With a nominal input SHSYNC frequency of 1792 × HSYNC (approximately 28 MHz) clock and standard NTSC signals 1408 samples are acquired and processed by the SAB9080.

PIP modes

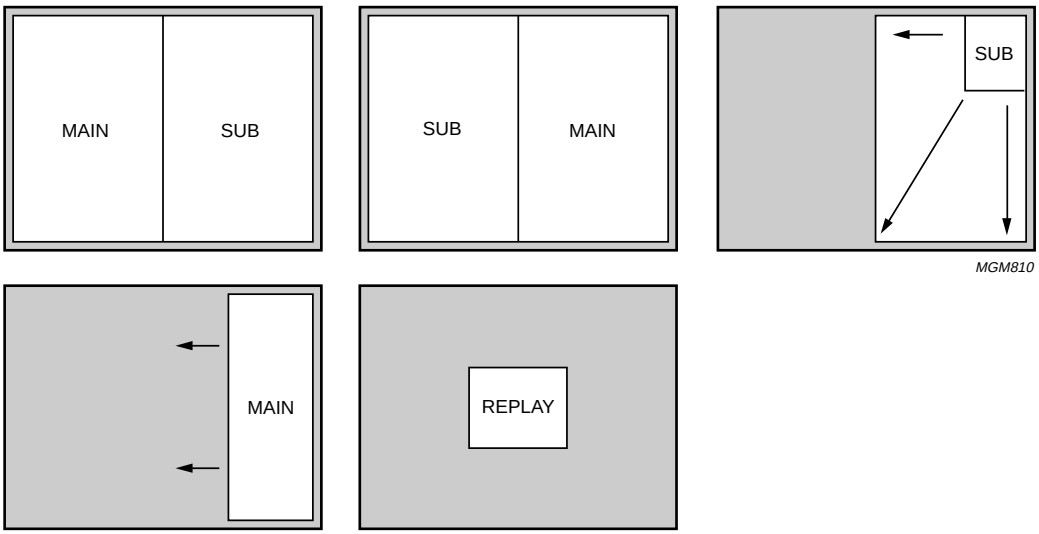


Fig.3 PIP modes.

I²C-bus description

The I²C-bus provides bidirectional 2-line communication between different ICs. The SDA line is the serial data line and the SCL serves as serial clock line. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy. The SAB9080 has the I²C-bus addresses 2C. Valid subaddresses are 00H to 18H, registers 15H to 18H are reserved for future extensions. I²C-bus control is according to the I²C-bus protocol: First a START sequence must be put on the I²C-bus, then the I²C-bus address of the circuit must be sent, then a subaddress. After this sequence the data of the subaddresses must be sent. An auto increment function gives the option to send data of the incremented subaddresses until a STOP sequence is sent. Table 1 gives an overview of the I²C-bus addresses. The data bits which are not used should be set to zero.

Table 1 Overview of I²C-bus addresses

SUB ADD	DATA BYTES							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00H	MPIPON	SPIPON	S1FLD	SFreeze	DNonint	PipMode2	PipMode1	PipMode0
01H	SHBlow1	SHBlow0	SHRed5	SHRed4	SHRed3	SHRed2	SHRed1	SHRed0
02H	SVBlow	SVRed6	SVRed5	SVRed4	SVRed3	SVRed2	SVRed1	SVRed0
03H	BGVfp3	BGVfp2	BGVfp1	BGVfp0	BGHfp3	BGHfp2	BGHfp1	BGHfp0
04H	SDHfp7	SDHfp6	SDHfp5	SDHfp4	SDHfp3	SDHfp2	SDHfp1	SDHfp0
05H	SDVfp7	SDVfp6	SDVfp5	SDVfp4	SDVfp3	SDVfp2	SDVfp1	SDVfp0
06H	–	–	–	–	–	–	–	–
07H	–	–	–	–	–	–	–	–
08H	MAHfp3	MAHfp2	MAHfp1	MAHfp0	SAHfp3	SAHfp2	SAHfp1	SAHfp0
09H	SAVfp7	SAVfp6	SAVfp5	SAVfp4	SAVfp3	SAVfp2	SAVfp1	SAVfp0
0AH	DUVPol	DVSPol	DFPol	DHsync	SUVPol	SVSPol	SFPol	SHsync
0BH	MainFidPos7	MainFidPos6	MainFidPos5	MainFidPos4	MainFidPos3	MainFidPos2	MainFidPos1	MainFidPos0
0CH	SubFidPos7	SubFidPos6	SubFidPos5	SubFidPos4	SubFidPos3	SubFidPos2	SubFidPos1	SubFidPos0
0DH	BGon	Bon	MFidPOn	SFidPOn	Prio	AlgOff	SFblkPkff1	SFblkPkff0
0EH	BSel1	BSel0	SBBrt1	SBBrt0	–	SBCol2	SBCol1	SBCol0
0FH	–	–	SLSel5	SLSel4	SLSel3	SLSel2	SLSel1	SLSel0
10H	I2CHold	SV	SDSel5	SDSel4	SDSel3	SDSel2	SDSel1	SDSel0
11H	MDHfp7	MDHfp6	MDHfp5	MDHfp4	MDHfp3	MDHfp2	MDHfp1	MDHfp0
12H	MDVfp7	MDVfp6	MDVfp5	MDVfp4	MDVfp3	MDVfp2	MDVfp1	MDVfp0
13H	MHBlow	–	MHRED5	MHRED4	MHRED3	MHRED2	MHRED1	MHRED0
14H	–	VBwidth2	VBwidth1	VBwidth0	–	HBwidth2	HBwidth1	HBwidth0
15H to 18H	all bits are reserved							

MPIPON (DOUBLE WINDOW)

With MPIPON the main channel PIP is switched on (logic 1) or off (logic 0).

SPIPON

With SPIPON the sub PIPs are switched on (logic 1) or off (logic 0).

S1FLD

If S1FLD is set to logic 0 two fields are used for the live PIP. When a 50/60 Hz or a 60/50 Hz mode is detected the SAB908x automatically switches to the 1 Field mode (1 Field resolution vertically).

If S1FLD is set to logic 1 only one field is used. This causes joint line errors but saves memory. In normal modes this bit should not be set.

SFREEZE

With SFreeze set to logic 1 the current live sub PIP will be frozen. If set to logic 0 it is unfrozen.

ALGOFF

In double window mode precautions are taken to prevent a joint line error. Under some conditions this feature should be switched off. This can be realized by setting this bit to logic 1. AlgOff should be set to logic 0.

DNONINT

In normal mode (this bit is logic 0) the SAB9080 calculates whether a signal is non-interlaced or not and reacts accordingly. With the DNonint bit set to logic 1 the display channel is forced into the non-interlaced mode. In the non-interlaced mode only one field is used during processing of the PIPs.

PIP MODE AND REPLAY

The PIP modes for the SAB9080 are shown in Table 2.

Table 2 PIP modes

BITS	MODE
000	double window mode
001	replay mode

SHRED AND SVRED (DOUBLE WINDOW)

SHRed and SVRed determine the reduction factor in the double window mode.

The horizontal reduction is equal to SHRed/96 and the vertical reduction is equal to SVRed/96. SHRed should lie in the range from 0 to 48, if set to logic 0 the PIP is off. SVRed should lie in the range from 0 to 96, if set to logic 0 the PIP is off.

For the horizontal reduction factor, when the reduction factor is 48/96, 704 samples are processed. The HRed is linear so when HRed is e.g 24/96 352 samples are processed. For the vertical reduction factor the same holds but then with the number of lines. For NTSC the number of processed lines can be calculated from VRed/96 $\times$ 228 lines.

BGHFP AND BGVFP

These bits control the horizontal and vertical positioning of the PIP configuration on the screen. The horizontal range is adjustable in 16 steps of four 28 MHz clocks.
The vertical range is 16 steps of 1 line/field.
The background colour can be adjusted with bits Bsel, SBBrt and SBCol.

SDHFP AND SDVFP

These bytes control the horizontal and vertical positioning of the sub PIPs on the screen. The horizontal range is 256 steps of eight 28 MHz clocks. The vertical range is 256 steps of 1 line/field.

MAHFP, SAHFP AND SAVFP

These bytes control the horizontal and vertical inset starting point of the acquired data. The horizontal range is 16 steps of eight 28 MHz clocks. The vertical range is 256 steps of 1 line/field.

DUVPOL, DVSPOL, DFPOL AND DHSYNC

These bits control the PLL/deflection settings. With DUVPol the polarity of the border UV signals can be inverted in case the deflection circuit behind the SAB9080 expects inverted signals. With DVSPol set to logic 0 the SAB9080 triggers on positive edges of the DVSYNC. If it is set to logic 1 it triggers on negative edges. DHSYNC determines the timing of the DHSYNC pulse. If it is set to logic 0 a burstkey is expected and if it is set to logic 1 a H-sync is expected. DFPol can invert the field ID of the incoming fields.

SUVPOL, SVSPOL, SFPOL AND SHSYNC

These bits control the PLL/Decoder settings. With SUVPol the polarity of the video UV signals can be inverted in case the decoder circuit before the SAB9080 gives inverted signals out.

With SVSPol set to logic 0 the SAB9080 triggers on positive edges of the SVSYNC. If it is set to logic 1 it triggers on the negative edges. SHSYNC determines the timing of the SHSYNC pulse. If it is set to logic 0 a burstkey is expected and if it is set to logic 1 a H-sync is expected. SFPol can invert the field ID of the incoming fields.

MAIN, SUB FID POS ON (MFIDPON AND SFIDPON)

MFidPon (main) and SFidPon (sub) enable the field identification position fine tuning. The default value is off (logic 0), no fine positioning; when on (logic 1) the field identification position is determined by the value of M/S FIDPos.

BGON

BGOn determines whether a the background is visible. The background has a size of 720 pixels and 240 lines for NTSC. The background colour can be adjusted with bits Bsel, SBBrt and SBCol.

BON, SBBRT, SBCOL AND BSEL

Bon can switch the sub-borders on (logic 1) or off (logic 0). SBBrt and SBCol set the brightness and colour type of the selected border. The brightness is set in 4 levels of 30%, 50%, 70% and 100% IRE. The colour type is one of black (grey), blue, red, magenta, green, cyan, yellow or white (gray). Bsel selects which colour is set, background or border.

Table 3 Bsel modes

BSEL	BORDER COLOUR SET
00	main
01	sub
10	background
11	sub-border select

MDHFP AND MDVFP

These bytes control the horizontal and vertical positioning of the main PIP on the screen. The horizontal range is 256 steps size of eight 28 MHz clocks. The vertical range is 256 steps of 1 line/field.

MHRED

MHRed can set the horizontal reduction factor, equal to MHRed/96, in a range from 0 to 48. If it is set to logic 0 the PIP is off, if it is set to 48 (the maximum value of MHRed) the horizontal reduction factor is 0.5.

SHBLOW AND SVBLOW (REPLAY MODE)

SHBlow and SVBlow are used in the replay mode. These bits can expand a pixel on the display side by a factor two (01) or four (11) in the horizontal direction (SHBlow) and a factor of two (1) in the vertical direction (SVBlow). Zero values indicate no expansion.

MHBLOW

MHBlow can expand the main picture by a factor of two in the horizontal direction.

SLSEL (REPLAY MODE)

In the replay PIP mode SLSel determines at which memory location the PIP data is written, the range depends on the memory usage for each PIP.
The maximum number of PIPs that can be stored in NTSC mode is 42.

SDSEL (REPLAY MODE)

SDSel selects which PIP is read from memory. Valid numbers are dependent on the maximum value of SLSel.

SFBLKPKOFF 1 : 0

SFBlkPkoff shifts the signals Fblk and Pkoff with respect to the YUV output, by half pixels.

Table 4 Shifts of FBLK and PKOff

SFBLKPKOFF	SHIFT OF FBLK AND PKOff
00	+0.5 pixel
01	no shift
10	–0.5 pixel
11	–1 pixel

I2CHOLD

I2CHOLD controls the updating of the I²C-bus controlled function towards the PIP. If set to logic 1 some register updates are on hold until the bit is set to logic 0. At the next main Vsync all settings are passed to the PIP functions.

The registers which are on hold when the I2CHold bit is set to logic 1 are:

1. MPIPON and SPIPON.
2. SHBlow and SVBlow.
3. SHRed and SVRed.
4. BGHfp and BGVfp.
5. BGOn and Bon.
6. SBBrt and SBCol.
7. MDHfp and MDVfp.
8. HBWidth and VBWidth.
9. DNonint.
10. BSel.

SV

SV controls the internal horizontal offset of the background. When set to logic 0 the offset is 0.86 μs, when set to logic 1 the offset is 4.56 μs.

HBWIDTH AND VBWIDTH

These bits control the horizontal and vertical border size in steps of 2 pixels and 1 line. The default horizontal border size is 4 pixels and the vertical border size is 2 lines. Default means after power-up and no I²C-bus data sent to the Picture-in-Picture controller.

NOTES

1. When the SAB9080 is set in the 1 field mode, joint line errors can occur. The SAB9080 is set in the 1 field mode by setting the 1Fld bit to logic 1.
2. When the SAB9080 is set in the non-interlace mode, joint line errors can occur. The SAB9080 is set in the non-interlace mode by setting the NonInt bit to logic 1.
3. When the input signals for the main and/or subchannel are non-interlaced signals, joint line errors can occur. When non-interlaced signals are input the SAB9080 switches automatically to the non-interlaced mode.
4. When the prevent joint line error algorithm is switched off (AlgOff is set to logic 1) joint line errors can still occur in the 2 field mode.

Acquisition channel ADCs and clamping

The analog input signals are converted to digital signals by means of three ADCs. The resolution of the ADCs is 8-bit (DNL is 7-bit and INL is 6-bit) and the sampling is performed at the system frequency of 28 MHz for the Y input. A bias voltage (V_{bias}) is used for decoupling the AC components on internal references.

The inputs should be AC-coupled and an internal clamp circuit, using external clamp capacitors, will clamp the input to $V_{ref(B)(DA)}$ for the luminance channels and to $(V_{ref(T)(DA)} - V_{ref(B)(DA)})/2 + LSB/2$ for the chrominance channels. The clamping starts at the active edge of the burst key. Internal video buffers amplify the standard input signals Y, U and V to the correct ADC levels.

PLL

The PLL generates an internal system clock of $1792 \times$ HSYNC, from the HSYNC, which is approximately 28 MHz.

DACs and video buffers

The 28 MHz digital video signals are fed to the 8-bit DACs which produce the required analog video signals.
The video buffers amplify these signals prior to being fed to the output to drive another device.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	–0.5	tbf	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	0	70	°C
V_{esd}	electrostatic discharge handling	–	3	kV
R_{thj-a}	thermal resistance	–	45	K/W
P_{max}	maximum power dissipation	–	1.0	W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611, Part E”*, dated 14 december 1992.

ESD LEVELS

Table 5 ESD performance

PIN	SYMBOL	HUMAN BODY MODEL (V)	MACHINE MODEL (V)
20	$V_{DD(RP)}$	> 500	> 150
32	T5	400	> 150
33	T4	400	< 150 (estimated 50)
34	T3	400	< 150 (estimated 50)
35	T2	400	> 150
36	T1	400	> 150
37	T0	400	> 150
38	TC	> 500	> 150
39	$V_{DDD(RL)}$	> 500	> 150
40	$V_{SSD(RL)}$	> 500	> 150
41	$V_{SSD(RM)}$	> 500	> 150
42	$V_{DDD(RM)}$	> 500	> 150
43	TCLK	> 500	< 150 (estimated 50)
44	TM	> 500	> 150
45	TCBD	> 500	> 150
46	TCBC	> 500	> 150
47	TCBR	> 500	< 150 (estimated 50)
61	$V_{SSD(RP)}$	> 500	> 150
68	FBL	1000	standard specification
69	PKOFF	1000	standard specification
70	DVSYNC	1000	standard specification
72	SVSYNC	1000	standard specification
73	SCL	1000	standard specification
81	SV	> 3000	150
93	T7	> 3000	> 325
rest in range 1 to 17	all other pins	> 3000	> 325
rest in range 64 to 100	all other pins	> 3000	> 325

ANALOG CHARACTERISTICS

V_{DDA} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	positive supply voltage		3.0	3.3	3.6	V
V_{SS}	ground voltage		–	0	–	V
$\Delta V_{DD(max)}$	maximum DC difference between supply voltages		–	0	100	mV
$\Delta V_{SS(max)}$	maximum DC difference between ground voltages		–	0	100	mV
$I_{DDD(q)}$	quiescent current of digital supply voltages	note 1	–	0	50	µA
$I_{DDA(DP)}$	display PLL supply current		–	1	–	mA
$I_{DDA(SP}$	sub PLL supply current		–	1	–	mA
$I_{DDA(MA)}$	main ADCs supply current	note 2	–	65	–	mA
$I_{DDA(SA)}$	sub ADCs supply current	note 2	–	65	–	mA
$I_{DDA(DA)}$	DACs supply current		–	tbf	–	mA
$I_{DDA(tot)}$	total analog supply current	note 2	–	tbf	–	mA
$I_{DDD(tot)}$	total digital supply current		–	tbf	–	mA
Analog-to-digital converter and clamping						
$V_{ref(T)}$	top reference voltage	note 3	tbf	2.90	tbf	V
$V_{ref(B)}$	bottom reference voltage	note 3	tbf	1.10	tbf	V
$V_{iY(p-p)}$	Y input signal amplitude (peak-to-peak value)	note 4	tbf	1.00	tbf	V
$V_{i(V)(p-p)}$	V input signal amplitude (peak-to-peak value)	note 4	tbf	1.05	tbf	V
$V_{i(U)(p-p)}$	U input signal amplitude (peak-to-peak value)	note 4	tbf	1.33	tbf	V
I_i	input current	clamping off	–	0.1	–	µA
		clamping on	–	tbf	–	µA
C_i	input capacitance		–	5	–	pF
f_s	sample frequency	note 5	–	1792 × HSYNC	–	kHz
RES	resolution		8	8	8	bit
DNL	differential non-linearity		–1.1	–	+1.1	LSB
INL	integral non-linearity		–2.0	–	+2.0	LSB
α_{cs}	channel separation		–	48	–	dB
PSRR	power supply rejection ratio		–	48	–	dB
$V_{clamp(Y)}$	Y clamping voltage level	note 6	–	1.28	–	V
$V_{clamp(U,V)}$	U/V clamping voltage level	note 6	–	2.00	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital-to-analog converter and output stage						
$V_{ref(T)}$	top reference voltage	note 2	tbf	1.19	tbf	V
$V_{ref(B)}$	bottom reference voltage		tbf	0.19	tbf	V
R_L	load resistance		1	–	1000	kΩ
C_L	load capacitance		0	–	5	pF
f_s	sample frequency	1FH, note 5	–	1792 × HSYNC	–	kHz
RES	resolution		8	8	8	bit
DNL	differential non-linearity		–1.0	–	+1.0	LSB
INL	integral non-linearity		–1.0	–	+1.0	LSB
α_{cs}	channel separation		–	48	–	dB
PSRR	power supply rejection ratio		–	48	–	dB
Display PLL and clock generation						
$f_{i(PLL)}$	input frequency	note 1	14	15.75 (NTSC)	17	kHz
Sub PLL and clock generation						
$f_{i(subPLL)}$	input frequency	note 1	14	15.75 (NTSC)	17	kHz

Notes

1. Digital clocks are silent, POR and TM are connected to V_{DDA}.
2. This value is measured with an external bias resistor of 39 kΩ resulting in a bias current of 50 μA.
3. The $V_{ref(T)}$ and $V_{ref(B)}$ are made by a resistor division of the V_{DD}. They can be calculated with the formulas:

   $$V_{ref(T)} = V_{DDA} \times \frac{2.90}{V_{DDA(nom)}} V \text{ and } V_{ref(B)} = V_{DDA} \times \frac{1.10}{V_{DDA(nom)}} V$$

4. The input signal are amplified to meet an internal peak-to-peak voltage level of $0.8 \times [V_{ref(T)} - V_{ref(B)}]$.
5. The internal system frequency is 1792 times the HSYNC input frequency for the subchannel.
6. The clamp level is not necessarily equal to the $V_{ref(B)}$ of the ADCs.
7. The UV-channels are clamped to: $\frac{(V_{ref(B)} + V_{ref(T)} + V_{LSB})}{2}$

DIGITAL CHARACTERISTICS

V_{DDD} = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC characteristics						
V_{IH}	HIGH-level input voltage	default	$0.8V_{DDD}$	–	V_{DDD} + 0.5	V
		pin 74	$0.8V_{DDD}$	–	tbf	V
		5 V tolerant pins 68, 69, 70, 72, 73	$0.8V_{DDD}$	–	tbf	V
V_{IL}	LOW-level input voltage	default	–0.5	–	$0.2V_{DDD}$	V
		pins tbf	–0.5	–	$0.2V_{DDD}$	V
V_{hys}	hysteresis voltage		0.8	–	–	V
V_{OH}	HIGH-level output voltage	I_{OL} = –X mA; V_{DDD} = 3.0 V; note 1	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} =X mA; V_{DDD} = 3.0 V; note 1	–	–	0.4	V
		I_{OL} = 2 mA; V_{DDD} = 3.0 V	–	–	0.4	V
$\|I_{LI}\|$	input leakage current	V_I = 0	–	–	1	µA
		$V_I = V_{DDD}$	–	–	1	µA
$\|I_{OZ}\|$	3-state output leakage current	V_O = 0 V or $V_O = V_{DDD}$	–	–	1	µA
$I_{lu(I/O)}$	I/O latch-up current	V < 0V; V > V_{DDD}	200	–	–	mA
R_{pu}	internal pull-up resistor		16	33	78	kΩ
AC characteristics						
f_{sys}	system frequency	note 2	–	1792 × HSYNC	–	kHz
t_r	rise time		–	6	25	ns
t_f	fall time		–	6	25	ns

Note

1. X is the source/sink current under worst case conditions. X is reflected in the name of the I/O cell according to the drive capability. Minimum value of X is 1 mA.
2. The internal system frequency is 1792 times the HSYNC input frequency for the subchannel.

TEST AND APPLICATION INFORMATION

The application diagram in a standard configuration is shown in Figure 4. The input signals main CVBS and sub CVBS of different video sources are processed by the SAB9080 and inserted by the YUV/RGB switch.

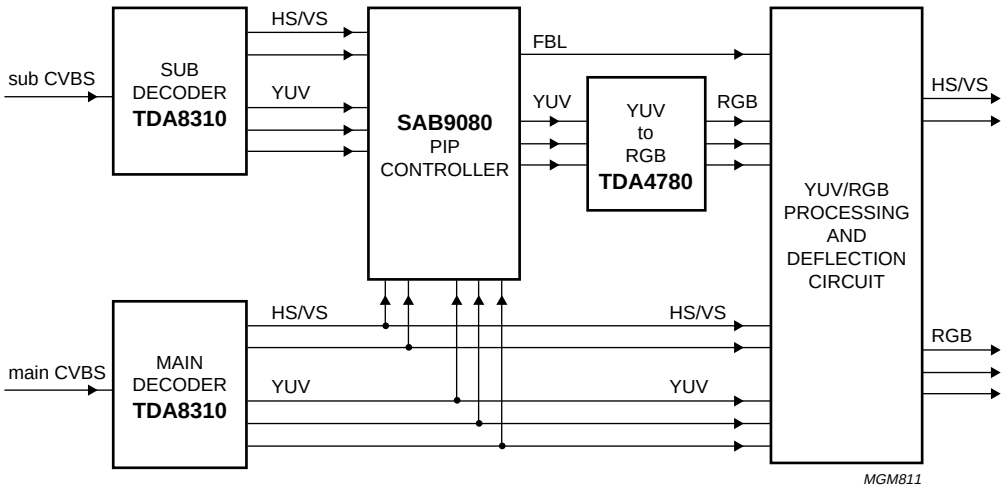
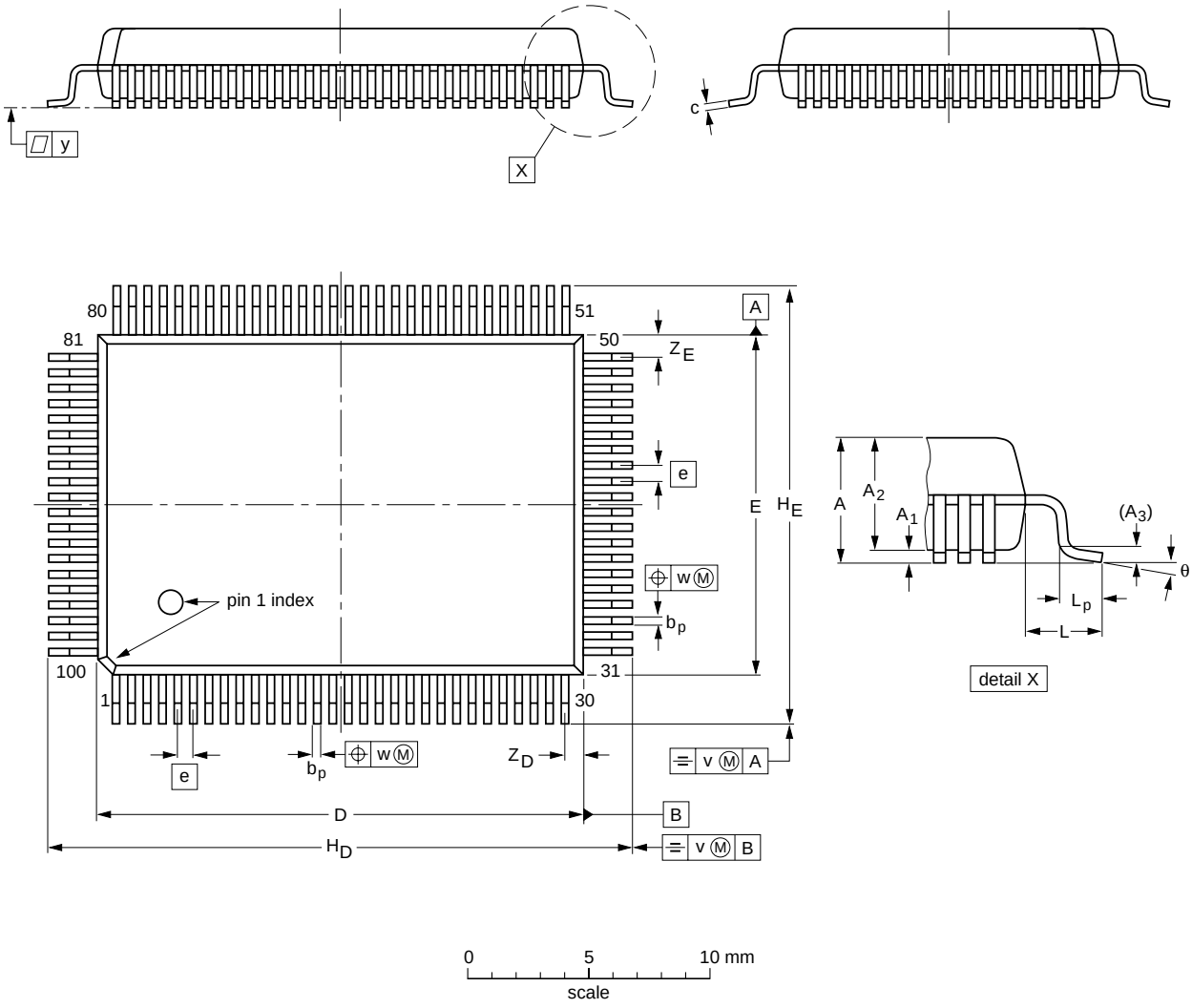


Fig.4 Application diagram.

PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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Printed in The Netherlands 545104/750/01/pp24 Date of release: 1999 Jan 05 Document order number: 9397 750 03293

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