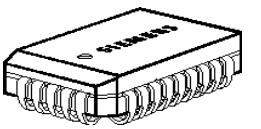
SIEMENS

High-Level Serial Communications Controller (HSCC)

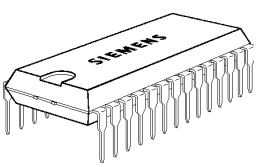
SAB 82520
SAF 82520

1 Features

- Two independent HDLC channels
- Implementation of X.25 LAPB/LAPD protocol
- Programmable timeout and retry conditions
- FIFO buffers for efficient transfer of data packets
- Digital phase-locked loop for each channel
- Baudrate generator and oscillator
- Different modes for clock recovery and data encoding
- High-speed data rate (up to 4 MHz)
- Supports bus configuration by collision resolution
- Telecom-specific features programmable
- 8-bit parallel µP interface
- Advanced CMOS technology
- Low power consumption; active: 25 mW at 4 MHz
  standby: 3 mW
- SAB 82520: operating temperature 0 to 70 °C
- SAF 82520: operating temperature – 40 to 85 °C



P-LCC-28-R



P-DIP-28

SAB 82520, a High-level Serial Communications Controller (HSCC), has been designed to free the user from tasks occurring in communication via networks and trunk lines.

SAB 82520 is an X.25 LAPB/LAPD controller which, to a large degree performs communications procedures independently of CPU support.

A parallel processor bus constitutes the µC system. The communications interface is implemented by two full-duplex HDLC channels, which can be operated independently from one another. The HSCC is connected to the transmission line via additional line drivers or modems. External logic is cost-effective because clock recovery can be performed by an on-chip oscillator, DPLL circuits and a programmable baudrate generator.

Type	Ordering Code	Package
SAB 82520-N	Q67100-H8400	P-LCC-28 (SMD)
SAB 82520-P	Q67100-H8014	P-DIP-28
SAF 82520-N	Q67100-H8610	P-LCC-28 (SMD)
SAF 82520-P	Q67100-H8512	P-DIP-28

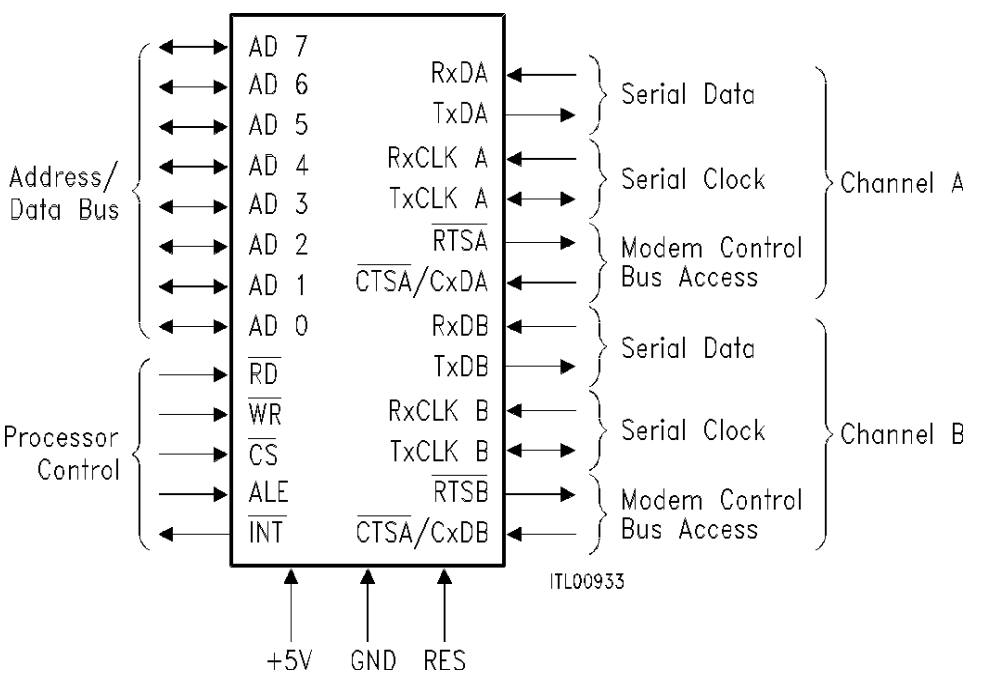
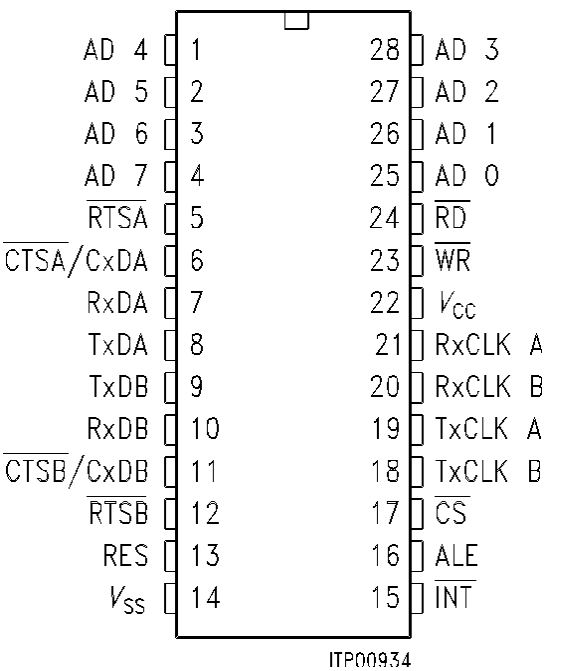


Figure 1
Logic Symbol

Pin Configurations
(top view)

P-DIP



P-LCC

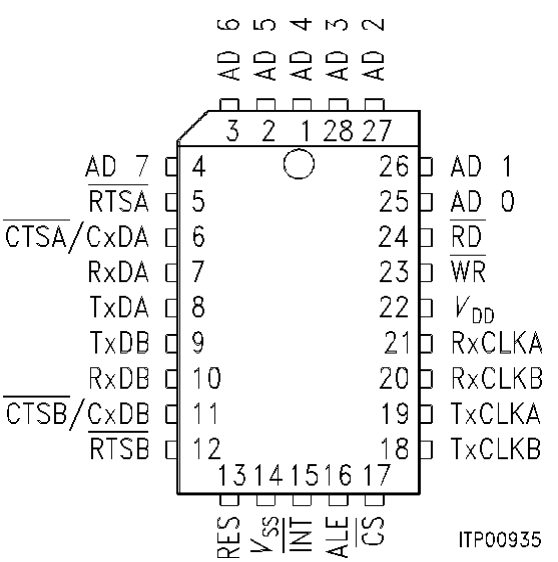


Figure 2

1.1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Functions
25 26 27 28 1 2 3 4	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address Data Bus** The multiplexed address data bus transfers data and commands between the µP system and the HSCC.
5 12	$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	O O	**$\overline{\text{Request to Send}}$** When the RTS bit in MODE is set, the RTS signal goes low. When the RTS bit is reset, the signal goes high of the transmitter has finished and there is no further request for a transmission. In a bus configuration, RTS goes low during the actual transmission of a frame shifted by a clock period, excluding collision bits.
6 11	$\overline{\text{CTSA}}$/C × DA $\overline{\text{CTSA}}$/C × DA	I I	**$\overline{\text{Clear to Send}}$/Collision Data** A low on the inputs enables the respective transmitter. If the transmitters are always enabled, CTS should be connected to VSS. In a bus configuration the external serial bus must be connected to the respective C ¥ D pin.
7 10	R × DA R × DB	I I	**Receive Data** These lines receive serial data at standard TTL or CMOS levels.
8 9	T × DA T × DB	O O	**Transmit Data** These lines transmit serial data at standard TTL or CMOS levels. They can be programmed as push-pull or open-drain outputs.
13	RES	I	**RESET** A high on this input forces the HSCC into reset state. The HSCC is in power-up mode during reset and in power-down mode after reset. The minimum pulse length is 1.8 µs.
14	V_{SS}		Ground (0 V)
15	$\overline{\text{INT}}$	O	**$\overline{\text{Interrupt Request}}$** The signal is activated when the HSCC requests an interrupt. It is an open-drain output.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Functions
16	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address data bus, selecting one of the HSCC internal sources or destinations.
17	$\overline{CS}$	I	**$\overline{\text{Chip Select}}$** A low on this signal selects the HSCC for a read/write operation.
18 19	T × CLK B T × CLK A	I/O I/O	**Transmit Clock** These pins can be programmed in several different modes of operation. T × CLK may supply the transmit clock for the respective channel, a receive strobe signal (T × CLK A) and a transmit strobe signal (T × CLK B) or a frame synchronization signal (T × CLK A, clock mode 5). Programmed as outputs, T × CLK supply the transmit clock of the respective channel or a tristate control signal, indicating the programmed transmit time slot (T × CLK B, clock mode 5).
20 21	R × CLK B R × CLK A	I I	**Receive Clock** These pins can be programmed in several different modes of operation. In each channel R × CLK may supply the receive clock, the receive and transmit clock, the clock for the baud rate generator or the clock for the DPLL. They also can be programmed for use as a crystal oscillator.
22	V_{DD}		Power + 5 V power supply.
23	$\overline{WR}$	I	**$\overline{\text{Write}}$** This signal indicates a write operation.
24	$\overline{RD}$	I	**$\overline{\text{Read}}$** This signal indicates a read operation.

1.2 Functional Description

In a point-to-multipoint or in a multimaster configuration the HSCC can be used as a central station (master) or a peripheral station. As a peripheral station the HSCC can initiate the transmission of data. An internal function block provides for collision avoidance, which may occur if several stations start the transmitting simultaneously.

Furthermore, in a special operating mode the HSCC can transmit or receive data packets in programmable time slots; this makes SAB 82520 especially suitable for applications in systems designed for packet switching. In this application in particular, the integrated collision-resolution mechanism provides optimal utilization of system-internal PCM paths.

A number of characteristics which distinguish the SAB 82520 from conventional low-level HDLC devices are described below.

Support of Layer-2 Functions by HSCC

"Low-level" HDLC devices usually support various of protocols. When applying the HDLC protocol mainly bit-oriented functions such as bit stuffing, CRC check, flag and address recognition are performed. SAB 82520 has been especially designed to support the ISO HDLC protocol. In addition to the bit-oriented functions, the device provides a high degree of procedural support and evaluates the layer-2 control field. The communications procedures are processed between the communications controllers and not between the processors. As a result procedure handshaking is no longer necessary. The processor is informed of the status of the procedure, however. The dynamic load of the processor is thus largely reduced. To maintain cost effectiveness and flexibility, not all layer-2 functions have been implemented as hardware. Instead, functions such as connection set-up/connection clear-down and error recovery in case of protocol errors are performed by the processor software.

Operating Modes

The distribution of functions between HSCC and CPU applies to the auto mode. As a prerequisite for this operating mode, the window size between transmitted and acknowledged frames has to be limited to 1 frame. Alternatively, transparent modes can be applied, the data field as well as the layer-2 headers are forwarded directly to the CPU. The reception and transmission of messages is fully controlled by the CPU. This operating mode is selected when the component is used as a central station (master) or if the accepted distance between transmitted and received frames (window size) is larger than 1 frame.

Furthermore, there is a possibility to bypass the receiver and to get access to the received data directly.

FIFO Buffers for Efficient Transfer of Data Packets

Another feature of the SAB 82520 can be seen in the buffers that are used for temporary storage of data packets which are transferred between the serial communication interface and the parallel system bus. Due to the overlapping input/output operation (dual-port behavior), the maximum length of the data packets is not limited by the buffer size. The dynamic load of the processor is reduced by transferring the data packets block by block.

One FIFO buffer with a total capacity of 64 bytes per direction and channel is divided into two memory pools of 32 bytes each. When a pool is filled (receive mode) or emptied (transmit mode) via the serial interface, the processor is prompted by interrupt to read or write this pool. Subsequently the second pool is filled or emptied. During this time the CPU can transfer the first block thereby ensuring availability of the pool. With a serial transfer rate of 1 Mbit/s the reaction time between the first prompting and data overflow with loss of data is 256 µs. In addition, the transmit FIFO provides the flexibility for temporarily storing blocks of various lengths, which can be received in rapid succession. The FIFO will also store a data packet when a preceding short data packet stored in the memory has not yet been read by the processor.

The HSCC is especially suitable for cost-critical applications with single chip processors due to its memory organization and on-chip memory control.

Move string commands are available for high-performance applications where fast data rates at the communication interface and a high level of processor performance are required. The FIFO can then be addressed by the automatically incremented address.

Serial Interface

The serial interface provides two independent, high-performance communication interfaces. As already mentioned, the ISO HDLC layer-2 protocol is supported by the HSCC. In addition, layer-1 functions are provided by means of on-chip circuits. Eight different operating modes can be selected to clock the serial data stream.

- During the self-clocked operating mode, the transfer clock is recovered from the received data stream by means of an external crystal only. On-chip oscillator and DPLL circuits sample the received bit stream and adjust the clock edge to the center of the data bit.
- The bit stream is synchronized in the externally clocked operation mode by external clock signals. On the whole, 4 different clock signals separated by direction and channel, can be forwarded.
  In addition to the data clock, an externally supplied strobe signal can be applied to determine the time period during which data is to be received or transmitted. Using another operating mode, a time slot (up to 64 bit) can be programmed for transmitting data and another time slot for receiving data. One time slot consists of eight clock cycles.
- With the point-to-multipoint configuration, comprising a central station (master) and several peripheral stations (slaves), data transmission can be initiated by a slave. If several stations (slaves) transmit data simultaneously, the bus is assigned to one station by a collision-resolution procedure implemented by the HSCC.
- The maximum data rate of the externally clocked operating mode is 4 Mbits per second. In the self-clocked operating mode with an external reference clock or the crystal oscillator, the maximum clock rate is 11.52 MHz, the maximum data rate will be 1220 kbit/s.

Applications

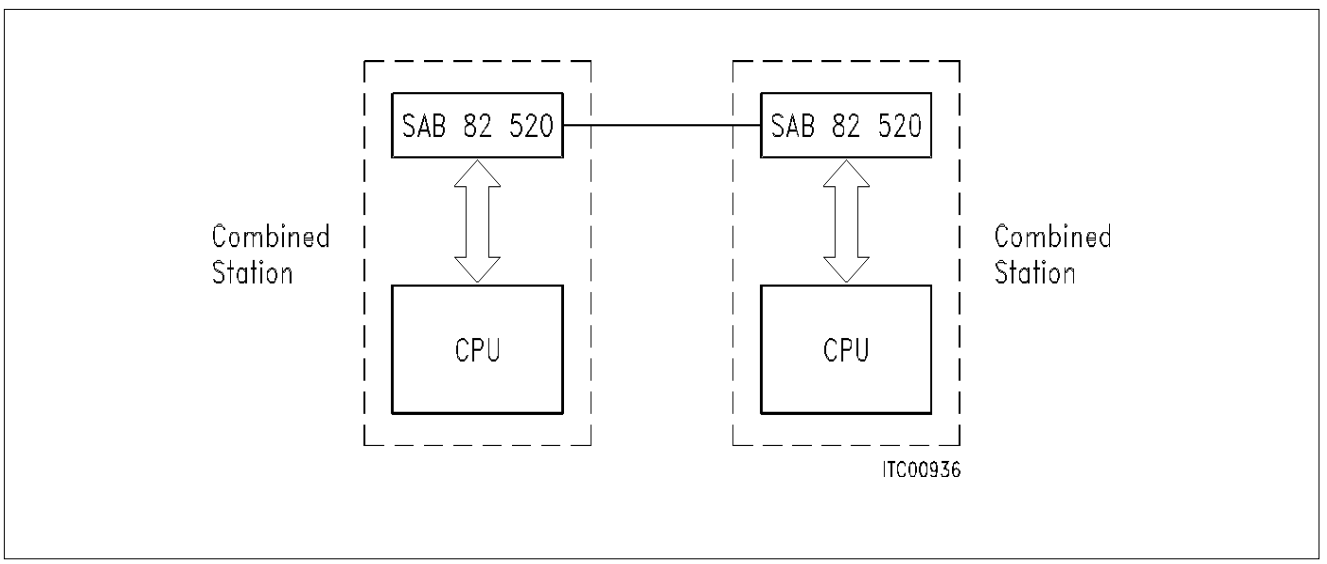


Figure 3a
Point-to- Point Configuration

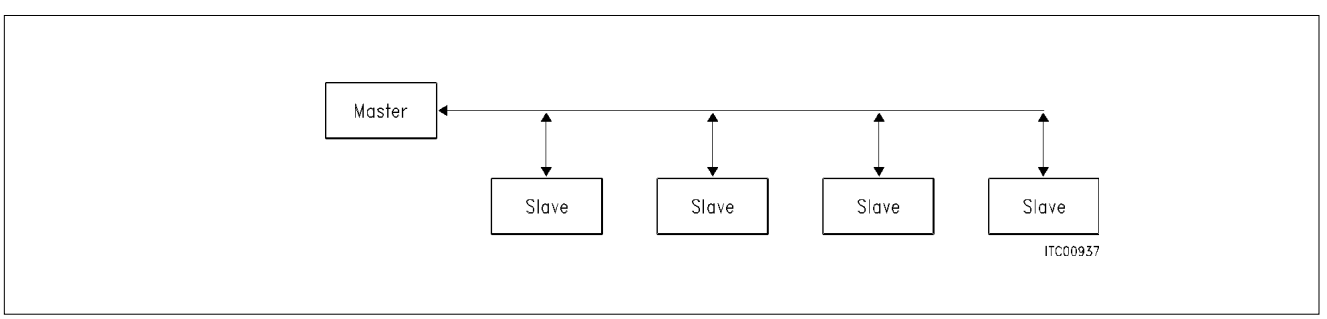


Figure 3b
Point-to- Multipoint Configuration

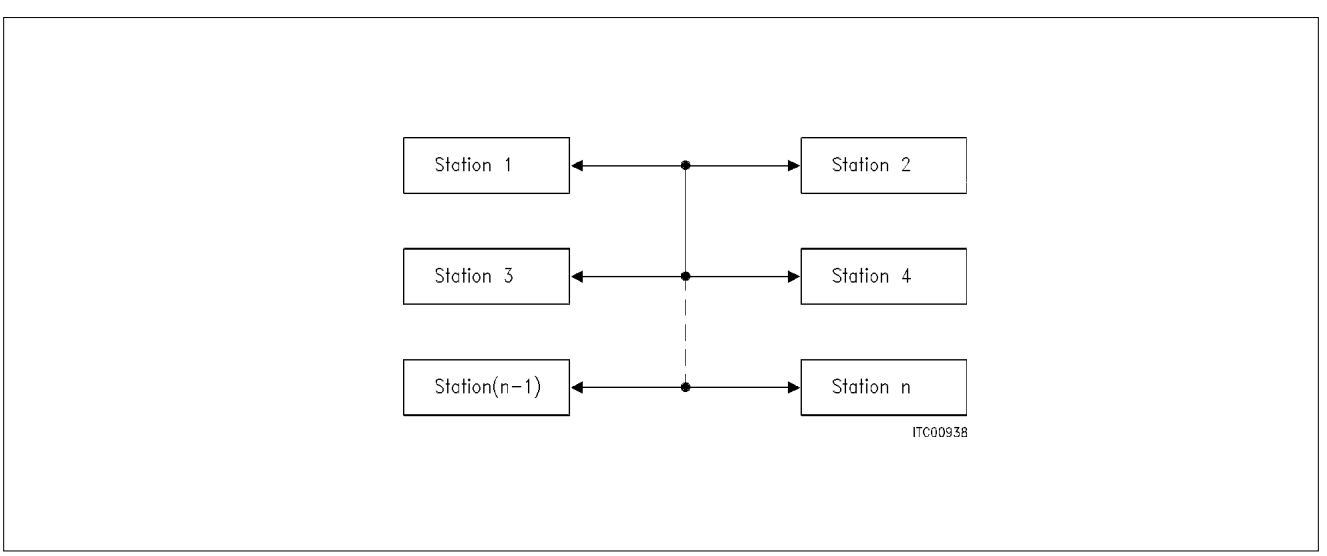


Figure 3c
Multimaster Configuration

Description of Block Diagram

The chip contains a serial interface for two channels, including a DPLL and collision-detection block, a data-link controller and the FIFO buffers. The µP interface, including the status and command registers, is used for both channels. These functions are implemented in 2 µm CMOS technology.

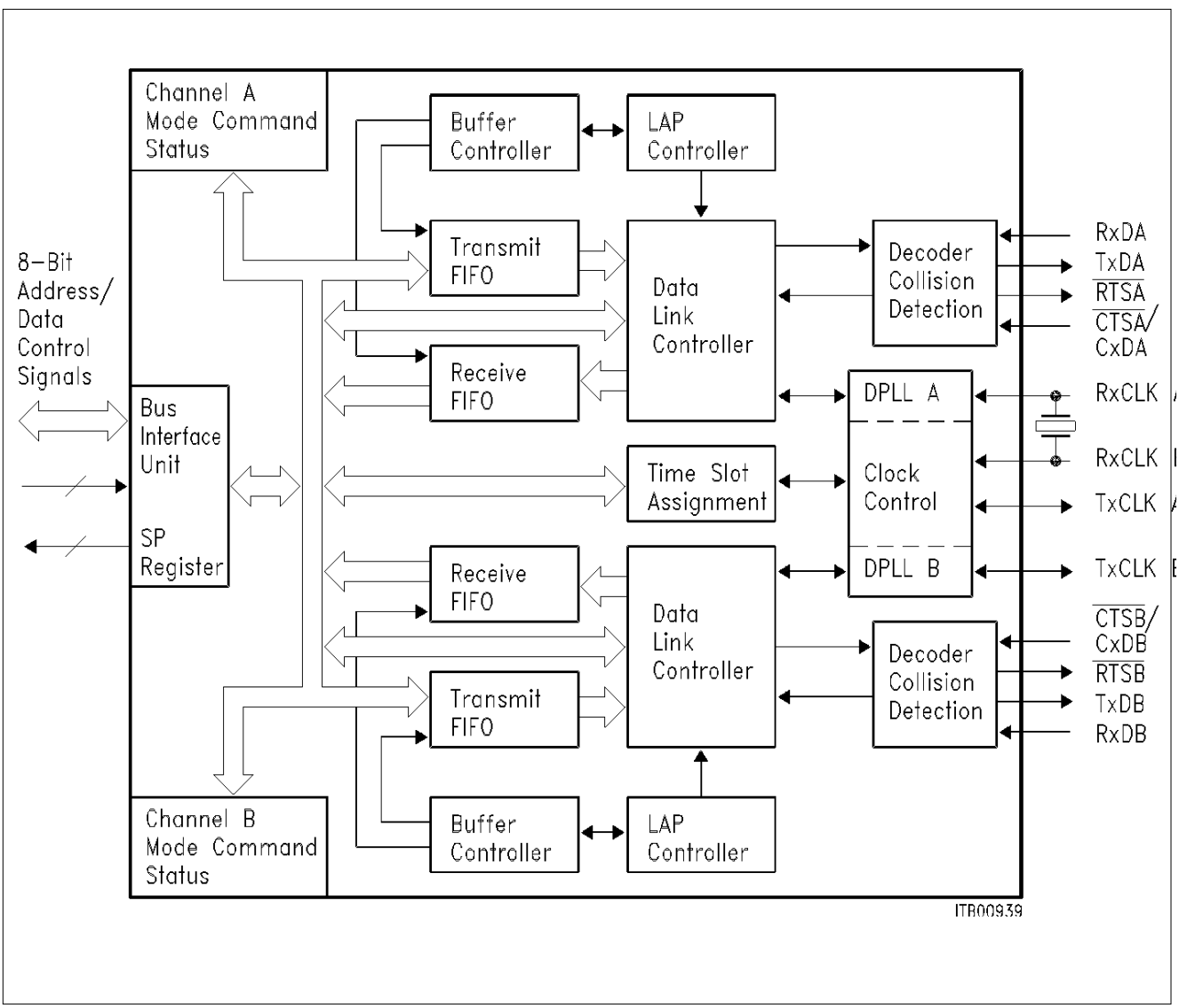


Figure 4
Block Diagram

2 Operating Modes

The µC sets the operating modes as well as controlling the functional sequences by reading or writing special registers in the HSCC. A detailed description of these registers has been provided under item 5.

The following functions are performed in accordance with the above:

- Setting of operating modes
- Transfer of data packets
- Layer-2 functions
- Test loops
- Bus mode
- DPLL mode
- Baud rate generator

The processor is informed by interrupt of special events in the HSCC. The $\overline{\text{INT}}$ output has been designed as an open-drain output, providing the possibility of connecting several HSCC's to an interrupt input of the µC. Subsequent to an interrupt, the interrupt status register/channel B (ISTA) must be read. Five interrupt events can be read out directly. Bit 0 indicates the extended interrupt register/channel B (EXIR), bit 1 the EXIR/channel A and bit 2 the ISTA/channel A.

Indications, which do not trigger an interrupt, can be read for each channel from the respective status register (STAR). Command and acknowledgements from the µC are forwarded to the HSCC by writing to the command register (CMDR).

The clock multiplexer's operating mode as well as the configuration of the serial interface can set in the common configuration register (CCR), while the operating mode of the HDLC controller for each channel can be individually set in the mode register.

2.1 The HDLC Controller's Operating Modes

The different operating modes differ in the treatment of the HDLC frames. There are 5 operating modes which can be set with software.

- Auto mode
- Non-auto mode
- Transparent mode
- Extended transparent mode 0
- Extended transparent mode 1

The type of processing of the layer-2 header of HDLC frames differs according to the operating mode.

Auto Mode

Characteristics: Window size 1, random message length, address recognition.

The component autonomously processes all numbered frames (S + I frames) of an LAP. All unnumbered frames on this LAP as well as all frames on logical connections operating in parallel are forwarded directly to the µC.

Data in the I field of the frames are temporarily stored in the RFIFO. The HDLC control field as well as additional information can be read from special registers.

According to the selected programming mode, the HSCC can perform a two byte or one byte address recognition. The higher ranking address byte of a two byte address will be compared with the fixed value FE_H and/or FC_H as well as two Bit 1 will thereby be excluded from the address comparison and is instead interpreted as a command/response bit, depending on the programming of the RAH1 register (CRI bit). Similarly, two comparison values can be entered into special registers (RAL1, RAL2) for the lower ranking address byte. A valid address will be recognized in the case where the higher ranking and lower ranking address bytes correspond to one of the comparison values. Thus, the HSCC can be called with a maximum of six address combinations, however, only the LAP identified through the address combination RAH1, RAL1 will be processed in the auto mode.

In case of a one byte address, RAL1 and RAL2 will be used as comparison registers. According to LAP B, the value in RAL1 will be interpreted as command and the value in RAL2 as response.

Note: In case of a one-byte address the value of RAH1 must be set to 00_H.

Non-Auto Mode

Characteristics: Address recognition, random window size.

All frames with a valid address comparison are forwarded directly to the µC. Up to 64 data bytes or two complete frames can be temporarily stored in the HSCC. Data in the I field is temporarily stored in the RFIFO. The HDLC control field and additional information can be read from special registers.

Transparent Mode

Characteristics: Address recognition high byte.

Only the higher address byte in a two byte address will be compared. Data in the I field is stored temporarily in the RFIFO. The second address byte can be read from the receive address byte low register 1 (RAL1), while the HDLC control field can be read from the receive HDLC control register (RHCR) and additional information from the receive status register (RSTA). Since the address compare procedure is omitted for one byte address, each frame will be stored.

Extended Transparent Mode 0

Characteristics: No address recognition.

The entire frame between the start flag and the first CRC byte is stored in the RFIFIO. In addition, the first byte after the start flag can be read from the RAL1, the second byte from the RHCR, and additional information from the RSTA.

Extended Transparent Mode 1

Characteristics: Full transparency, HDLC receiver deactivated.

With the receiver deactivated (MODE register), received data bytes can be read from RAL1. The HDLC receiver is in this case by-passed. Data will be updated in RAL1 after eight clock periods.

Characteristics: Address recognition high byte, HDLC receiver active.

The first byte after the opening flag is compared with FE_H, FC_H as well as with the values programmed in RAH1 and RAH2. In the case of a match, the remaining bytes of the frame (up to but excluding the CRC dependence) are stored in the RFIFO.

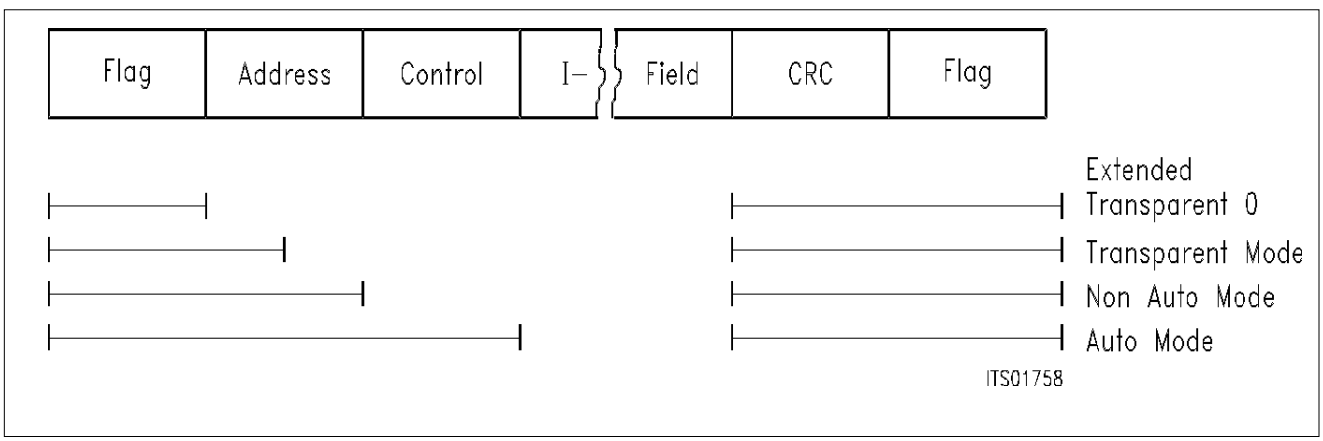


Figure 5
Internal Processing of an HDLC Frame

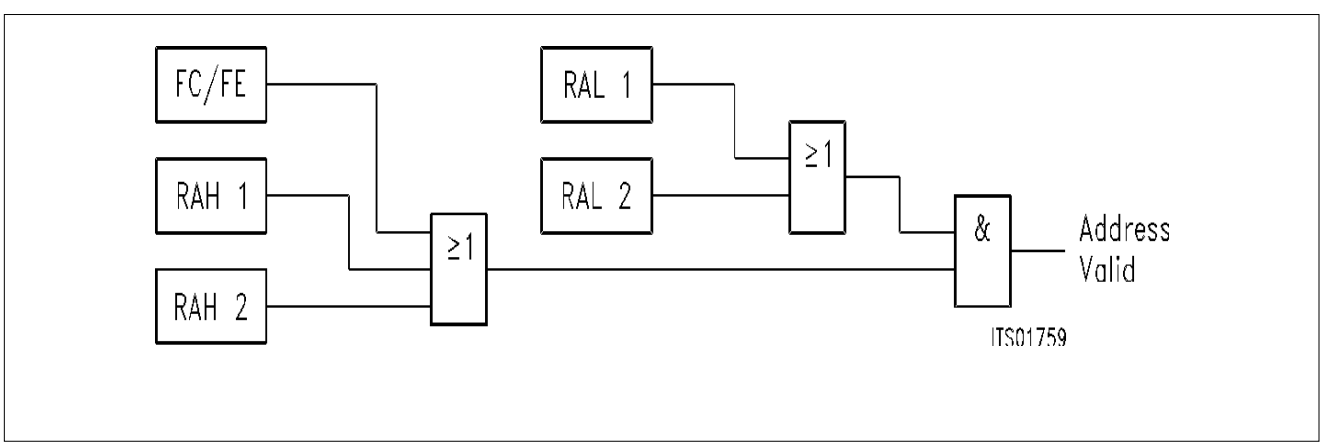


Figure 6
Internal Address Compare

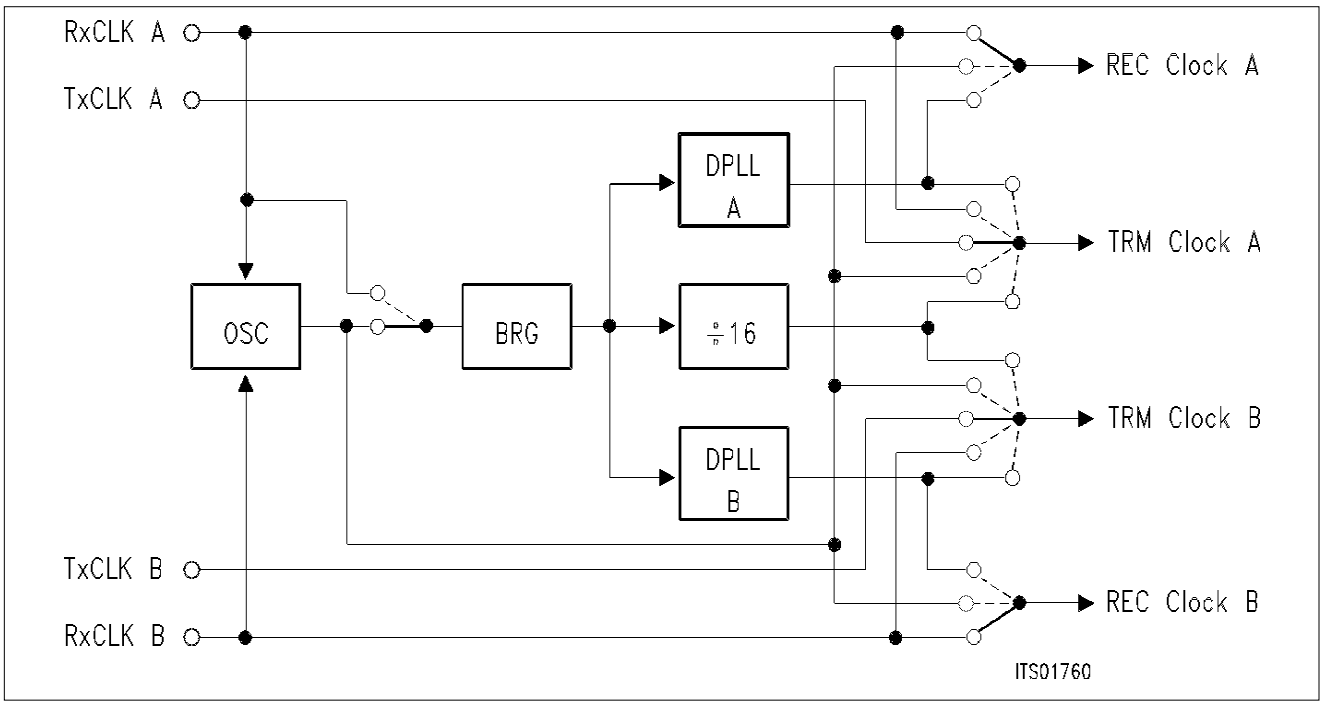


Figure 7
HSCC Clock Sources

2.2 Operating Modes of the Clock Multiplexer

The HSCC includes an internal oscillator circuit, a baud rate generator as well as two digital DPLL's. The receive and transmit clock for each channel can be generated separately and/or supplied externally. The component clock, on the other hand, is derived from the transmit clocks for channel A and/or channel B, eliminating the need for additional clock sources. During certain operating modes, a separate receive and transmit strobe can be supplied.

The possible clocking sources are:

For the receive clock

- R × CLK A/R × CLK B-pin
- DPLL channel A/B
- Oscillator

For the transmit clock

- R × CLK A/R × CLK B-pin
- T × CLK A/T × CLK B-pin
- DPLL channel A/B
- Baud rate generator frequency divided by 16
- Oscillator

Note: The ratio between the receive frequency (f_r) and the transmit frequency (f_x) for a channel must satisfy the condition $f_r/f_x < 2.8$; there are no restrictions on the phase shift. Slower transmit data rates can be realized with receive and transmit strobe.

Pins R × CLK A/R × CLK B and T × CLK A/T × CLK B generate the clock for the HSCC. R × CLK A/R × CLK B is used as crystal connection for the internal oscillator circuitry or as clock input. Depending on the programming of the Timing Control Register (TCR), T × CLK A/T × CLK B can be used either as a clock input or clock output. The clock sources for the transmitter, receiver and baud rate generator as well as the sources for the receive and transmit strobe as a function of the operating mode selected in the common configuration register (CCR) and in the Timing Control Register (TCR) are shown in **table 1.**

The clocking source for the DPLL's is always the internal baud rate generator; the scaling factor (divider) of the baud rate generator can be programmed through the Timing Control Register (TCR) and Baud rate Generator Register (BGR) between 1 and 2048.

In power-down mode, all internal clocks as well as the oscillator circuitry are disabled. After a hardware reset, the HSCC will be in the power-down mode.

Clock Mode 0

Separate, externally generated receive and transmit clocks are forwarded for each channel to the HSCC via their respective pins.

Clock Mode 1

Externally generated, but identical, receive and transmit clocks are forwarded for each channel via pins R × CLK A/R × CLK B. In addition, a transmit strobe can be connected via T × CLK B or a receive strobe via T × CLK A. This operating mode can be applied for transmission in the time division multiplex method or for adjusting disparate transmit and receive data rates.

Clock Mode 2

The baud rate generator is driven with an external clock (R × CLK A) and it delivers a reference clock for both DPLL's, which in turn generate the receive clock for the corresponding channels. Depending on the programming of the Timing Control Register (TCR), the transmit clock will be either an external clock signal (pins T × CLK A/T × CLK B) or the clock delivered by the baud rate generator divided by 16. In this case the transmit clock can be outputted via T × CLK A/T × CLK B.

Clock Mode 3

Baud rate generator and DPLL's are operated with an external reference clock (R × CLK A) and provide the receive and transmit clock for the respective channel. This clock can also be supplied via T × CLK A/T × CLK B.

Clock Mode 4

The transmit and receive clock for both channels is directly supplied by the on-chip oscillator. In addition, this clock can be supplied via T × CLK A and T × CLK B.

Table 1
Clock Mode and Clock Sources

Clock mode	TCR		Common Clock Sources		Channel A Clock Sources		Channel B Clock Sources		Common Sources		Clock Output
	TSS	TIO	BRG	DPLLA/B	REC	TRM	REC	TRM	R STROBE	X STROBE	T x CLKA/B
0	0	0	–	–	R x CLKA	T x CLKA	R x CLKB	T x CLKB	–	–	–
1	0	0	–	–	R x CLKA	R x CLKA	R x CLKB	R x CLKB	T x CLKA	T x CLKB	–
2	0	0	R x CLKA	BRG	DPLLA	T x CLKA	DPLLB	T x CLKB	–	–	–
2	1	1	R x CLKA	BRG	DPLLA	BRG:16	DPLLB	BRG:16	–	–	BRG:16
3	0	1	R x CLKA	BRG	DPLLA	DPLLA	DPLLB	DPLLB	–	–	DPLLA/B
4	0	1	–	–	OSC	OSC	OSC	OSC	–	–	OSC
5	0	0	–	–	R x CLKA	R x CLKA	R x CLKB	R x CLKB	TSAR	TSAX	[1]
6	0	0	OSC	BRG	DPLLA	T x CLKA	DPLLB	T x CLKB	–	–	–
6	1	1	OSC	BRG	DPLLA	BRG :16	DPLLB	BRG:16	–	–	BRG:16
7	0	1	OSC	BRG	DPLLA	DPLLA	DPLLB	DPLLB	–	–	DPLLA/B

[1] T x CLKA is used for synchronization, T x CLKB supplies a tristate control signal (cf. 4.1.2.6)

Clock Mode 5

This operating mode has been designed for application in time slot oriented PCM systems. The receive and transmit clock is identical for each channel and must be supplied externally via R × CLK A/ R × CLK B pins. The HSCC receives and transmits during certain 8-bit time slots in each frame. The transmit time slot is additionally indicated by a tristate control signal via T × CLK B, whose output is set to log 0 during the transmit period. The receive time slot may be programmed via Timeslot Assignment Register Receive, TSAR (resp. Transmit, TSAX). A frame synchronization signal is delivered to the HSCC via T × CLK A. The clock shift of the transmit time slot with respect to the synchronization signal may be programmed using TSAR/ TSAX (bits TCS2-0), while the clock shift for the receive time slot is programmed using the Timing Control Register (TCR, bit RCS2-0). The location of the transmit and receive time slots as a function of their programming and the clock shift is shown in **figure 8a; 8b; 8c.**

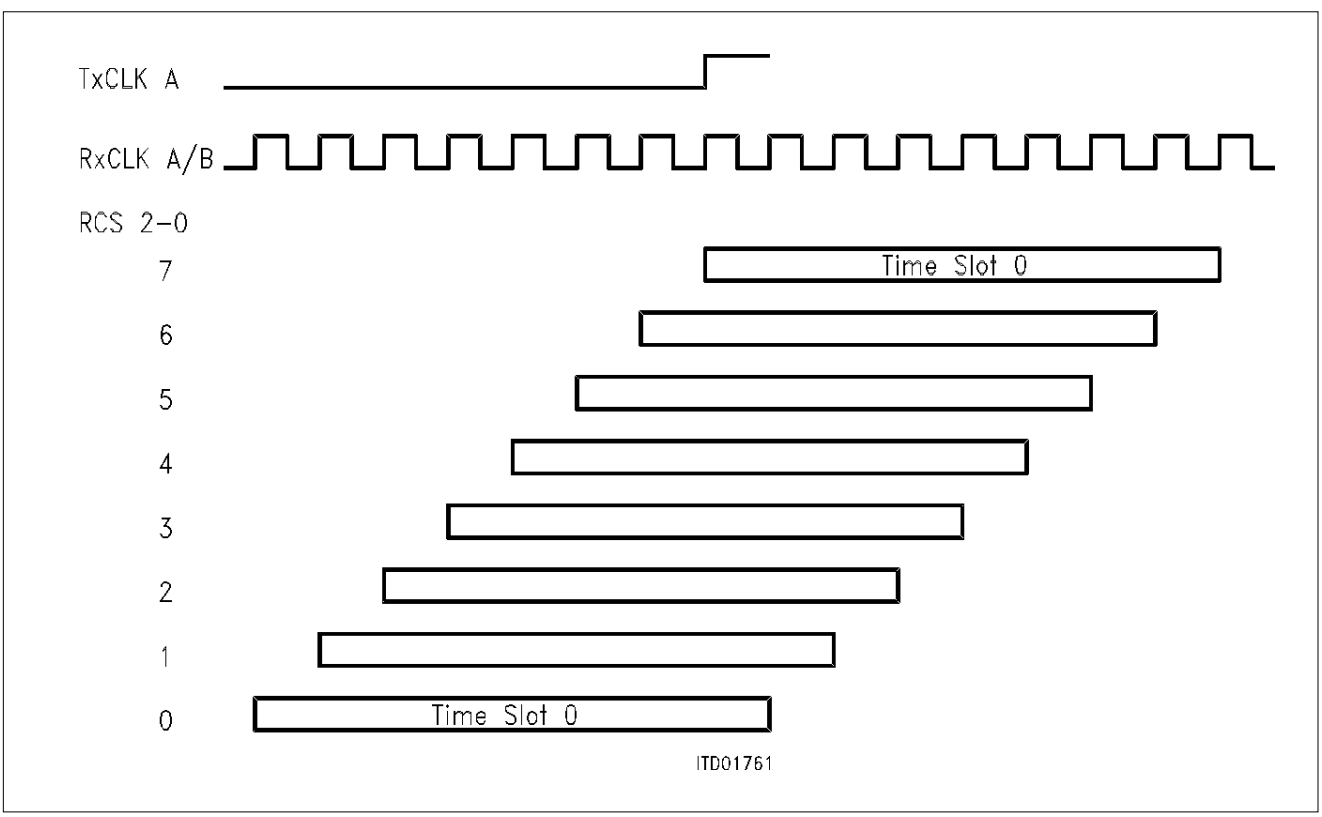


Figure 8
Position of Receive Time Slots

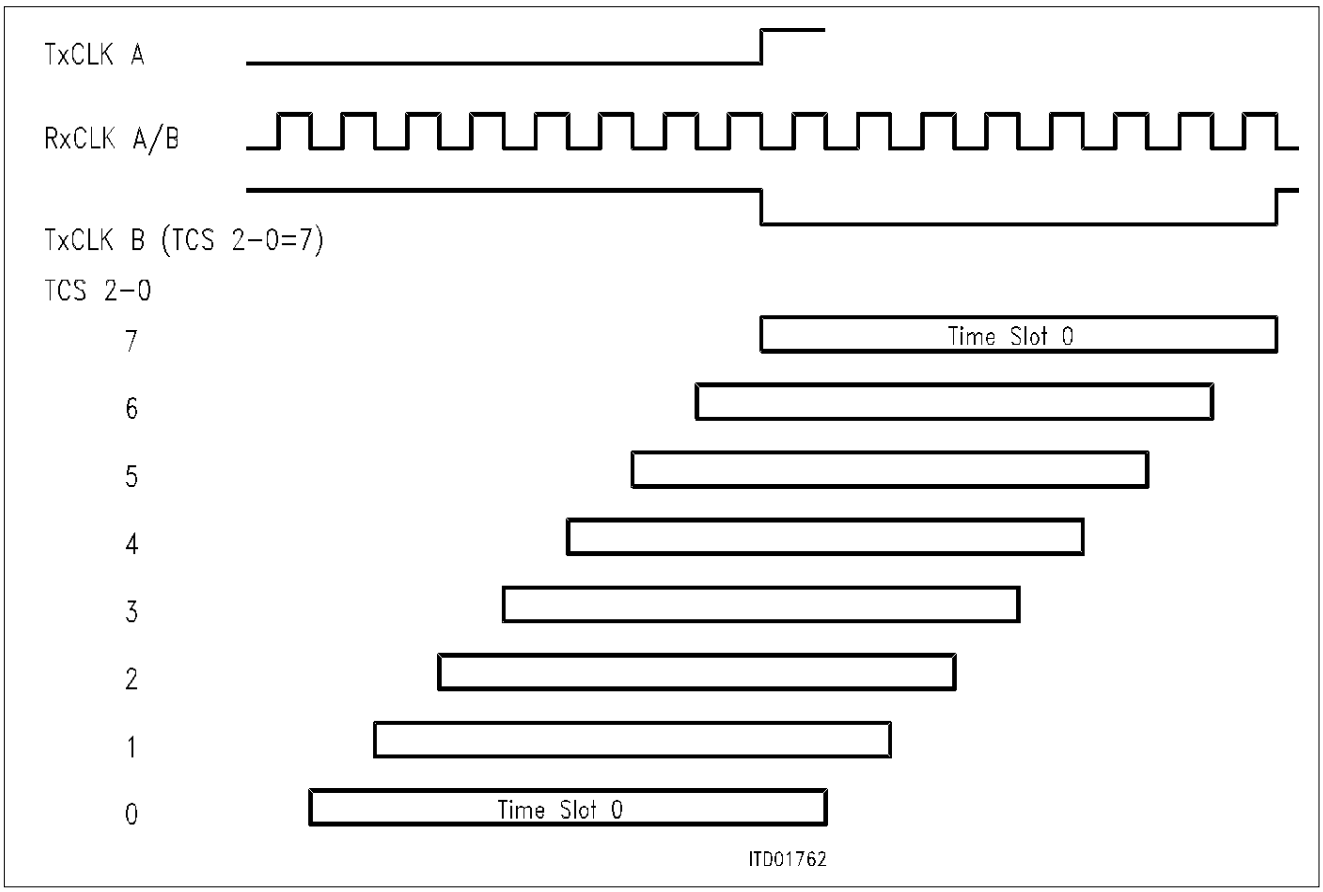


Figure 9
Position of Transmit Time Slots
Timing Mode 1

If the component is used in systems operating with a number of time slots other than 64 or 32, the frame synchronization signal must be supplied for each frame start-up. Also, in this case, the time slot 0 can be used only if the clock shift equals 0 (TCS2-0 resp. RCS2-0 equal to 7).

It is possible to transmit/receive either 64 Kbit or 56 Kbit channels, the selection being made in TCR (bit CCS). When receiving a 56 Kbit channel only, the first seven bits of a time slot will be valid. For transmitting a 56 Kbit channel, the first seven bits are used for data, the last bit being set to one.

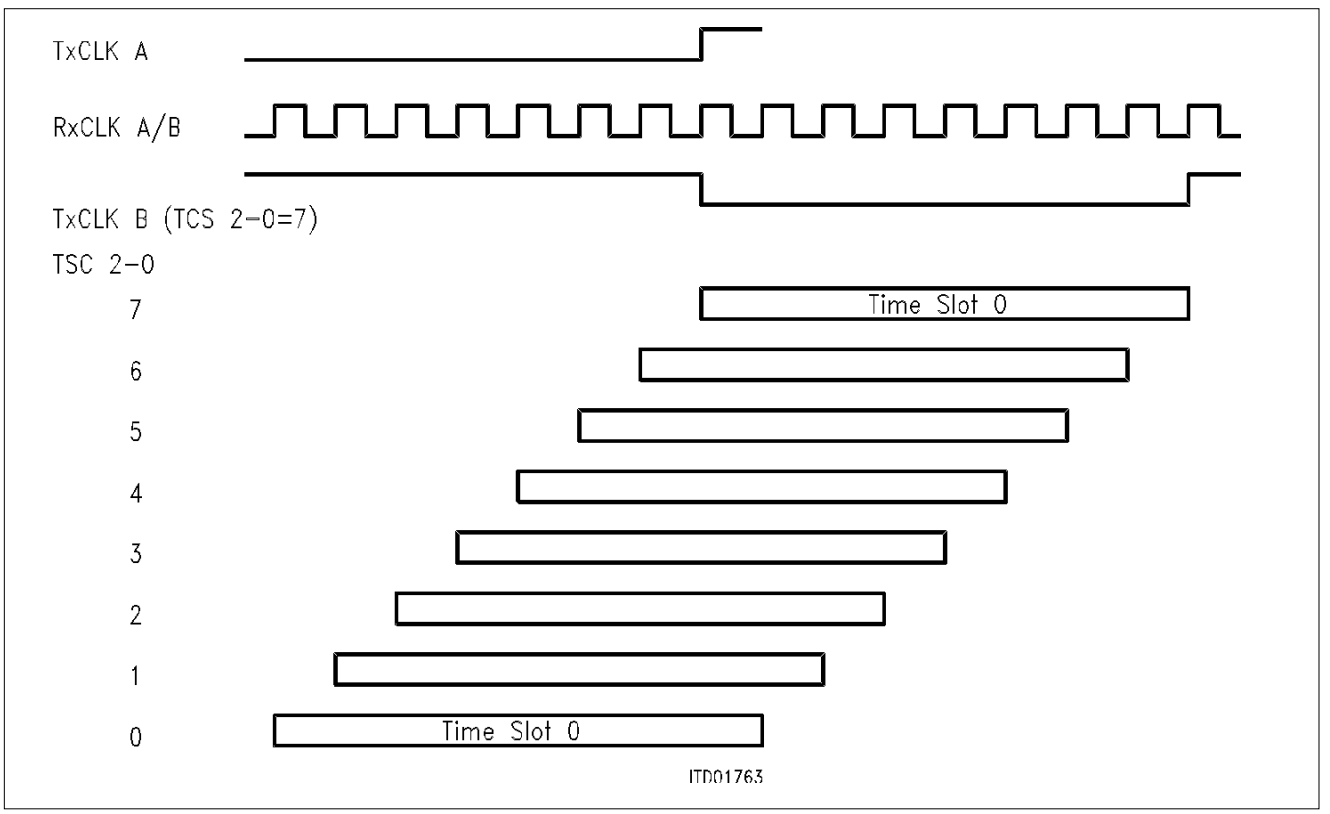


Figure 10
Position of Transmit Time Slots
Timing Mode 2

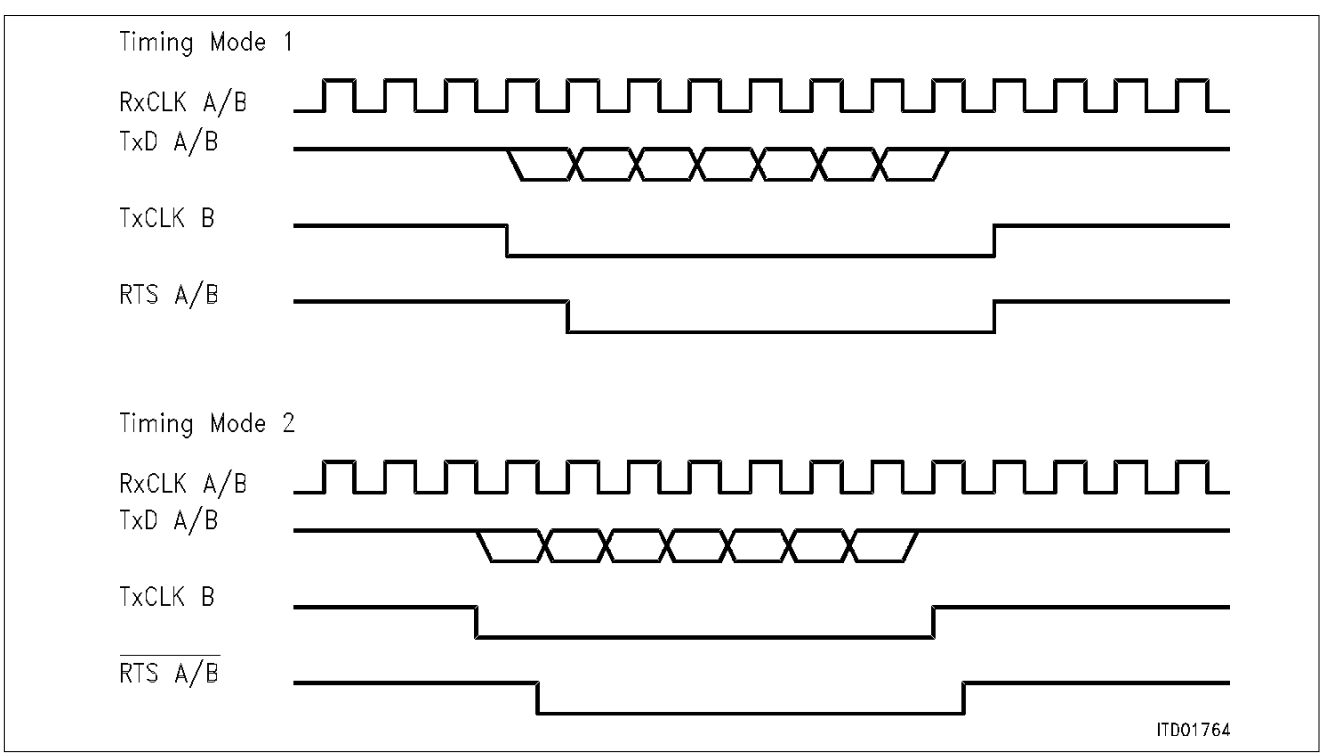


Figure 11
Transmission of 56 Kbit Channels
Bus Mode

Clock Mode 6

Baud rate generator and the DPLL's are operated with the reference clock provided by the on-chip oscillator and supply the receive clock for the respective channel. The transmit clock is taken to be either the externally provided clocking signal (T × CLK A/T × CLK B) or the baud rate generator frequency divided by 16. The transmit clock may also be made available as an output (T × CLK A/T × CLK B).

Clock Mode 7

Baud rate generator and the DPLL's are operated with the reference clock provided by the on-chip oscillator and supply the transmit and receive clock for the respective channel. This clock can be also supplied via T × CLK A/T × CLK B.

2.3 Configuration of the Serial Ports

In addition to the clock pins, the serial interfaces of the HSCC include the data inputs (R × DA/R × DB) and the data outputs (T × DA/T × DB) as well as the pins for the modem control or the bus access control ($\overline{\text{RTSA/RTSB}}$, $\overline{\text{CTSA/CTSB}}$). The data outputs can be operated as driver or as open drain outputs. During the idle state, either the idle code (log 1) or flags are outputted via T × DA/T × DB. These settings as well as the selection of the operating mode of serial interfaces can be performed in the common configuration register (CCR).

A transition on the CTS input will, with a corresponding programming of the Timing Control Register (TCR), generate an interrupt (EXIR). The actual value can subsequently be sent from STAR

Point-to-point, NRZ Encoding

The HSCC transmits and receives data in the NRZ format.

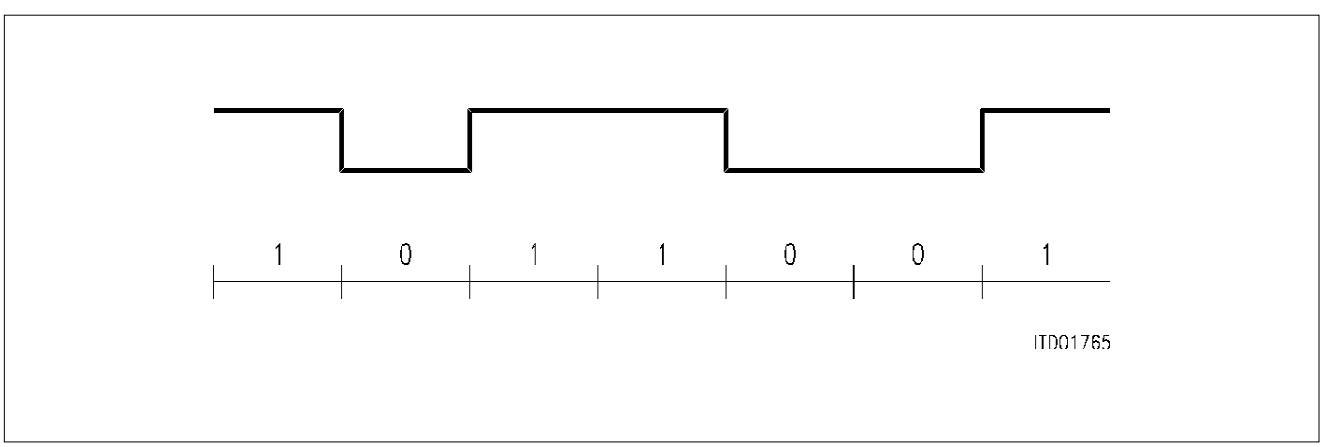


Figure 12
NRZ Encoding

Data output is performed with the rising clock edge, data input with the falling clock edge. A transmit request will be indicated by outputting log 0 at the request-to-send output ($\overline{RTSA}$/$\overline{RTSB}$). It is also possible to program the $\overline{RTS}$ outputs by software. After having received the permission to transmit ($\overline{CTSA}$/$\overline{CTSB}$) the HSCC transmits a frame.

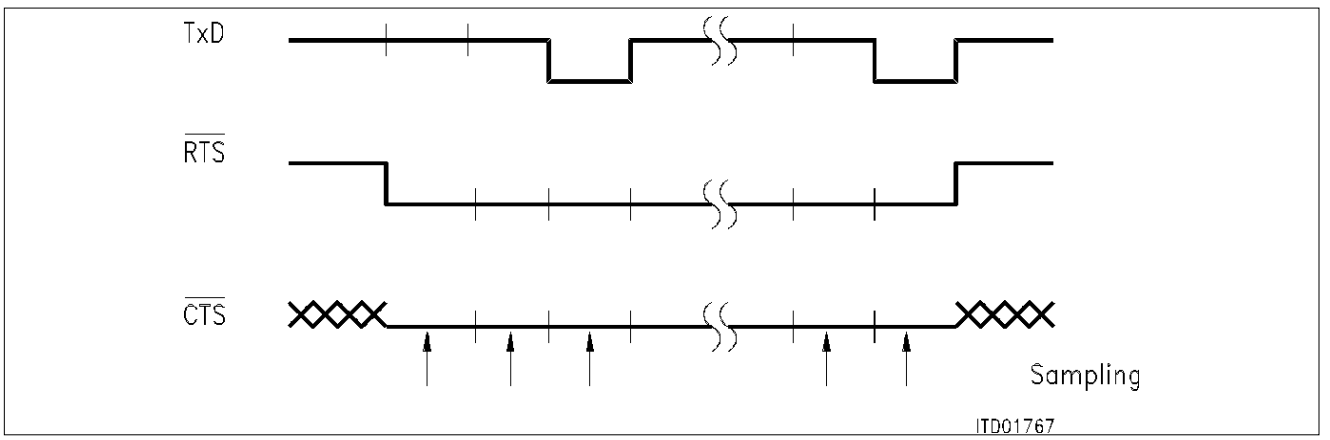


Figure 13
$\overline{RTS}$–$\overline{CTS}$ Handshaking

In the case where permission to transmit is withdrawn during the transmission process, the frame is aborted (idle). After a new permission to transmit has been received and if all of the data are still available in the HSCC, the terminated frame will be re-transmitted (self-recovery), without interrupting the CPU. However, if the permission to transmit is withdrawn after the 32nd byte in the information field, the transmitter and the XFIFO are reset, the RTS output is deactivated and an interrupt is generated for the µC.

Note: In the case where permission to transmit is not required, the $\overline{CTSA}$/$\overline{CTSB}$ inputs can be connected directly to V_{SS}.

Point-to-point, NRZI Encoding

The HSCC transmits and receives data in the NRZI format.

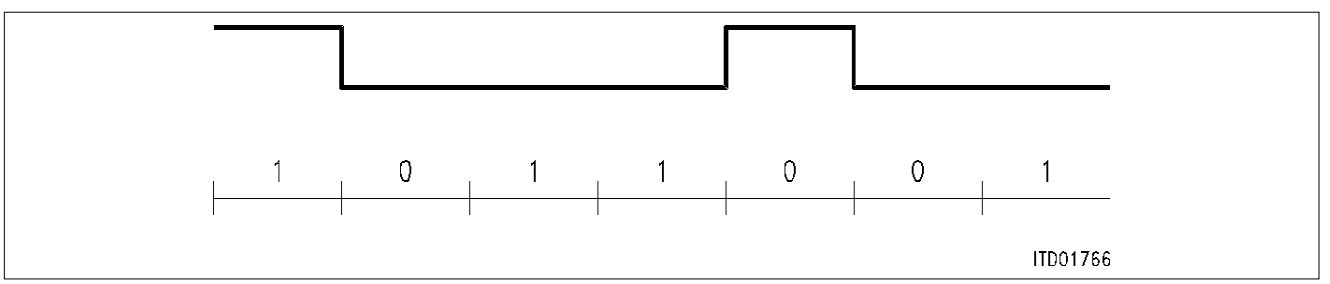


Figure 14
NRZI Encoding

During NRZI encoding, level changes are interpreted as log 0, and no changes in level as log 1. Since no more than 5 successive log 1's can appear in an HDLC frame, this type of encoding is especially suitable for data transfer with an asynchronous clock (DPLL operating mode). The utilization of modem control signals corresponds to NRZ Encoding (**figure 12**).

Bus Configuration, Timing Mode 1

In this bus configuration, the NRZ encoding and a logic wired OR connection of the individual transmitters are required. Data is outputted with the rising clock edge via T × DA/T × DB. The external bus is connected to the C × DA/C × DB input, data is clocked in 1/2 clock period later with the falling clock edge. Similarly, data in the R × DA/R × DB input is also clocked with the falling clock edge. The RTSA/RTSB output indicates, with a delay of one clock period, all bits that could be sent without a collision (**see 5.1**).

Bus Configuration, Timing Mode 2

This operating mode corresponds to bus configuration timing mode 1. However, in this case data are outputted on T × DA/T × DB with the falling clock edge and after one clock period evaluated on C × DA/C × DB. Thus one full clock period is available during the output of data and their evaluation. Transition on the RTSA/RTSB output also takes place with the falling clock edge.

3 Transfer of Data Packets

3.1 Receive Direction

The configuration selected for the FIFO controller is such that for worst case where messages are transmitted in a conditions non-optimized manner, a processor reaction time of more than 0.8 ms will result in messages. Normally, the required reaction time is 1 ms. The 64 byte FIFO has been designed as tandem FIFO.

In the case of short, successive messages, up to 2 messages can be stored. If long messages are transmitted and 32 bytes are stored in the RFIFO, readout by the processor is prompted by interrupt. The processor must handle the interrupt request, before additionally 32 bytes are received via the serial interface (1 ms). After a remaining message of up to 16 bytes has been stored, it is possible to store the first 16 bytes of a new message. The internal memory is now full. The arrival of additional bytes will result in "data overflow", and a third new message in "frame overflow". The generated interrupts are inserted together with all additional information into a wait line to be individually forwarded to the processor. The information whether or not additional interrupts are present in the wait line can also be read out (BMR bit in STAR). After an interrupt has been processed, the HSCC must be informed by the μC accordingly.

Note: The times listed are referenced to a data rate of 256 kbit/s.

Additional Information

In addition to the message end interrupt, the following information is stored by the HSCC in special registers:

– address combination and/or address field of the received frame
– the received frame’s control field
– type of frame (Command/response)
– CRC result
– data in the RFIFO yes/no
– "abort" with received frame yes/no
– data overflow
– length of message

The message length can be read from an 8-bit register, whereby bits 0 – 4 indicate the number of bytes which are still stored in the FIFO. Bits 7 – 5 are ignored after counter status 7 has been reached, indicating in this case a message length exceeding 224 bytes.

Messages of less than 5 bytes (4 bytes with 1 byte address) between the start and the end flag are ignored in all modes except extended transparent mode 0.

Worst Case Reaction Times

When operating as LAP-D controller, the following worst case reaction times can be expected in the frame receiving mode:

– one message, length ≥ 65 bytes
  reaction time equals 1 ms
– two messages, length 1 = 33, length 2 ≥ 17 bytes
  reaction time equals 0.8 ms and/or 0.7 ms in the extended transparent mode
– three successive short frames
  reaction time equals 0.5 ms and/or 0.4 ms in the extended transparent mode

Note: Length of message has been referenced to the length of the information field or, in the extended transparent mode, to the entire length between the start and the CRC field. A data rate of 256 kbit/s has been assumed.

Example to Illustrate Operating Mode of Interrupt Wait Line

The example illustrates the arrival of four successive frames. Additional information with respect to the interrupt/command bits has been included under **chapter 6.1**

– subsequent to the arrival of the 32 bytes, the HSCC generates the "receive pool full" interrupt (RPF)
– no reaction by the µC
– since the µC does not acknowledge this interrupt, the remaining message as well as the subsequent message are stored in the internal message memory.
– since the internal message memory is now full, the next S frame is lost and a "frame overflow" interrupt is generated.
– after the µC acknowledges the first interrupt, the next frame can be received and inserted into the wait line.

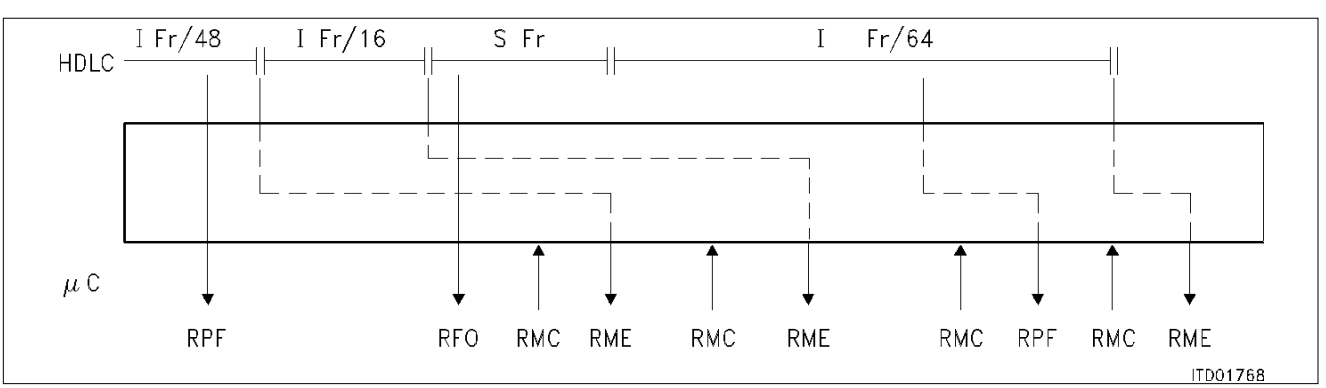


Figure 15
Interactions µC HSCC with Continuous Reception of Messages

3.2 Transmit Direction

Again 2 × 32 byte buffers have been provided in the transmit direction. After writing up to 32 bytes into the XFIFO, the HSCC can be prompted by command to transmit. Two different types of frames can be transmitted. For I frames the address and control field are generated autonomously by the HSCC and the data in the XFIFO are entered into the information field. For transparent frames, the address and control fields must be entered in the XFIFO as well. If the transmit request does not include an end flag, the HSCC will request the next data packet by interrupt, if not more than 32 bytes are stored in the XFIFO. This process will be repeated until the µC indicates by command the end of the message.

In the case where no more data are available in the XFIFO prior to the arrival of the end of message indication, the transmitted message is aborted and the µC is informed accordingly by interrupt (XDU). It is possible to abort a message by software (XRES).

When suitably programmed, the HSCC will perform a bus access control autonomously. Collisions which occur up to the 32nd data byte can be treated by the HSCC without interaction. If a collision is detected after the 32nd data byte, the HSCC terminates the message and prompts the processor to repeat the message (XMR). An interrupt (XPR) will also be generated after a transparent frame has been transmitted in full. In addition, the "ready to write/not ready to write" status of the XFIFO can be read from STAR at any time.

4 Procedural Support

In addition to address recognition, the HSCC autonomously processes all S and I frames (prerequisite window size 1) in the auto mode. The following functions will be performed:

– updating of transmit and receive counter
– evaluation of transmit and receive counter
– processing of S commands
– flow control with RR/RNR
– generation of responses
– recognition of protocol errors
– transmitting of S commands, if acknowledgement is missing
– continuous status query of opposite termination after RNR has been received
– programmable timer/repeater functions

In addition, all U frames are forwarded directly to the processor.

Additional logic connections can be operated in parallel by software. The logic link can be initialized by software at any time (RHR).

4.1 Reception of Frames

The logic processing of received S frames is performed by the HSCC without interrupting the µC. The µC is merely informed by interrupt with respect to status changes in the opposite termination (receive ready/not receive ready) and protocol errors
(unacceptable N (R) or S frame with I field).

I frames are also processed autonomously and checked for protocol errors. The I frame will not be accepted in the case of sequence errors (no interrupt is forwarded to the µC), but is immediately confirmed by an S response. If the µC sets the HSCC into a "receive not ready" status, an I frame will not be accepted (no interrupt) and an RNR response is transmitted. U frames are always stored in the R FIFO and forwarded directly to the µC. The logic sequence and the reception of a frame in the auto mode is illustrated in **figure 16**.

4.2 Transmission of Frames

The HSCC autonomously transmits S commands and S responses in the auto mode. Either transparent or I frames can be transmitted by the user. The software timer has to be operated in the internal timer mode to transmit I frames. After the frame has been transmitted, the timer is self-started, the X FIFO is inhibited, and the HSCC, waits for the arrival of a positive acknowledgement. This acknowledgement can be provided by means of an S or I frame.

If no positive acknowledgement is received during time t_1, the HSCC transmits an S command (p = 1), which must be followed by an S response (f = 1). If the S response is omitted, the process is performed n1 times, before it is terminated. Upon the arrival of an acknowledgement or after the completion of this poll procedure, the XFIFO is enabled and an interrupt is forwarded to the µC. Interrupts may be triggered by the following:

– message has been acknowledged as positive (XPR interrupt)
– message must be repeated (XMR interrupt)
– response has not been received (TIN interrupt)

Upon arrival of an RNR frame, the software timer is started and the status of the opposite termination is queried periodically after expiration of t_1, until the status "receive ready" has been detected. The user is informed accordingly via interrupt. Also, after the n1th absence of a response, an interrupt will be generated (TIN interrupt). As a result, the process will be terminated as illustrated in **figure 17**.

Note: The internal timer mode should only be used in the auto mode.

Transparent frames can be transmitted in all operating modes. After the transmission of a transparent frame, the XFIFO is immediately enabled, which is confirmed by interrupt (XPR). In this case, time monitoring can be performed with the timer in the external timer mode.

4.3 Examples of Interaction between the HSCC and the µC

The interaction between the HSCC and the µC during the transmission and reception of I frames is illustrated in **figure 18** the flow control with RR/RNR during the reception of I frames in **figure 19** and during the transmission of I frames in **figure 20**. Both the sequence of the poll cycle and protocol errors are illustrated in **figure 21**. The definition of the interrupt/command bits is contained under **chapter 6.**

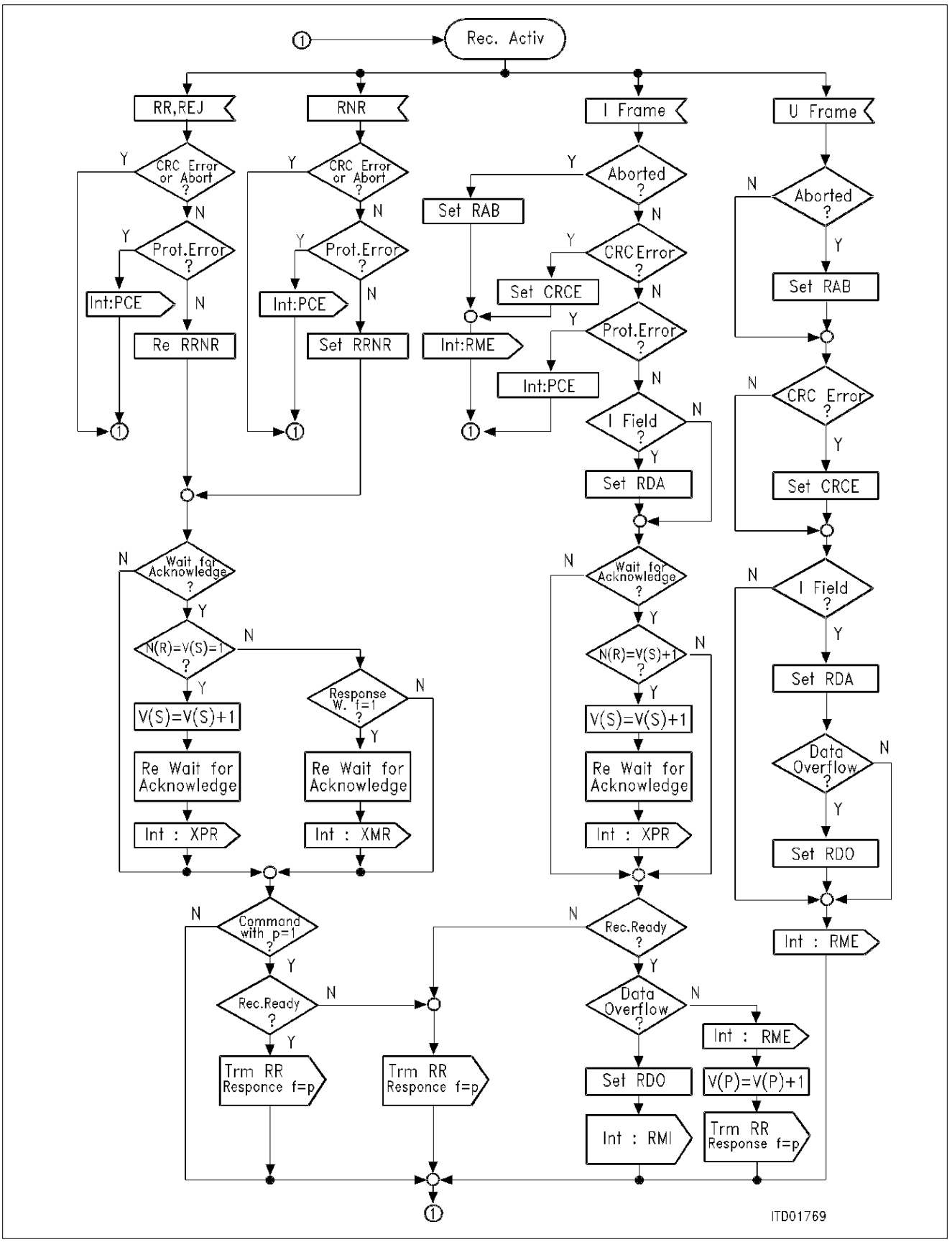


Figure 16
Logical Processing of Received Frames in Auto Mode

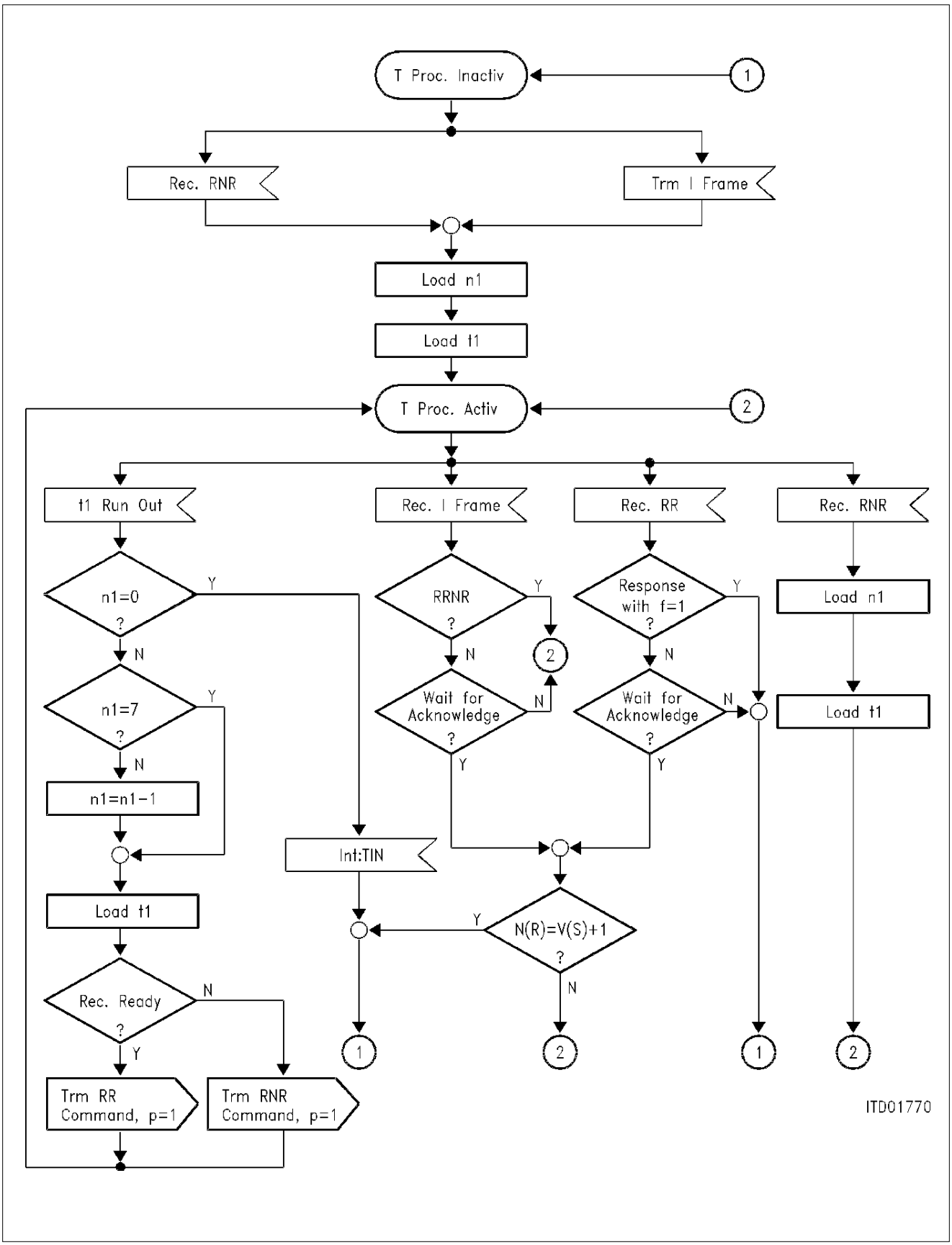


Figure 17
Timer Procedure/Poll Cycle

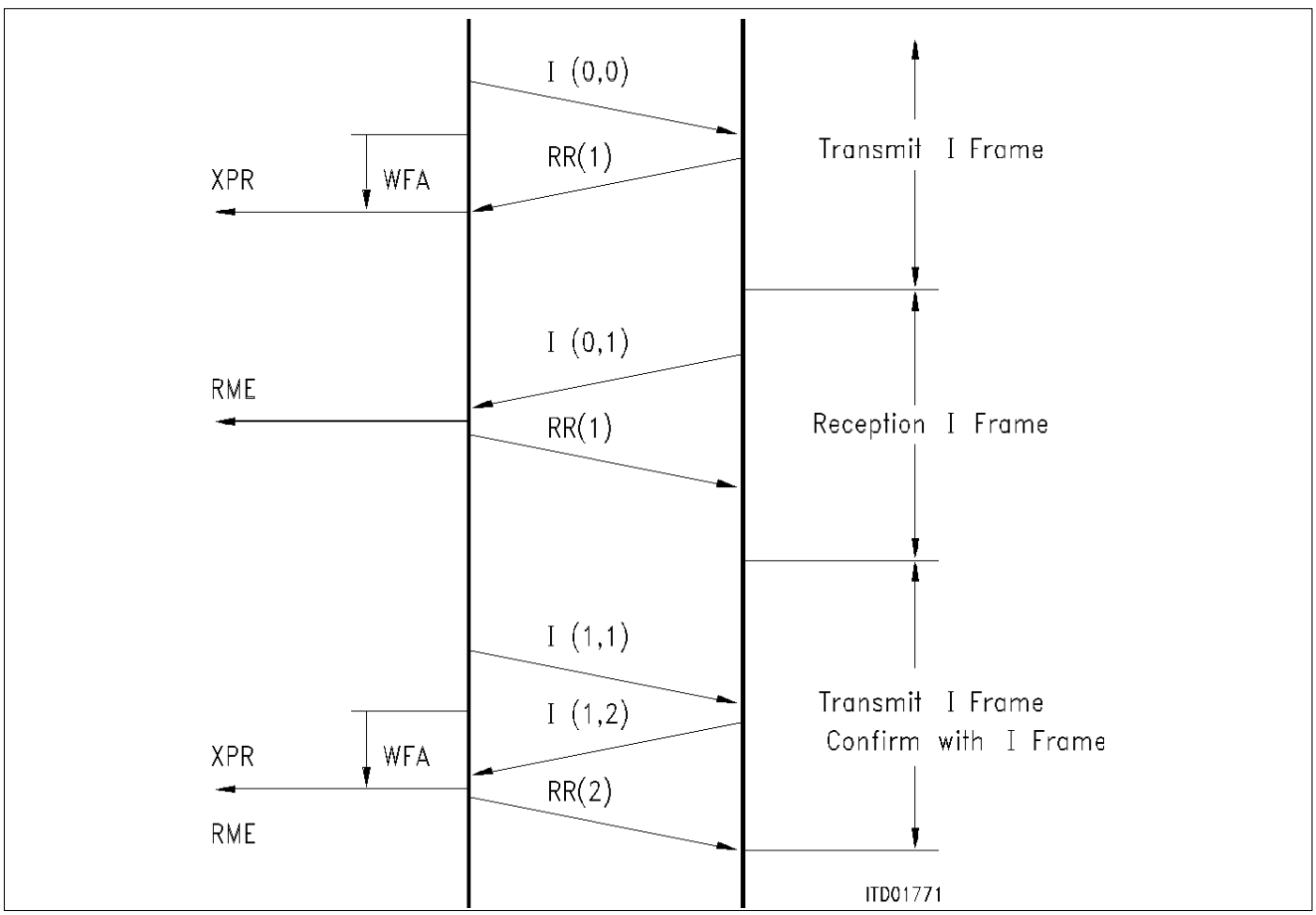


Figure 18
Transmission/Reception I Frames

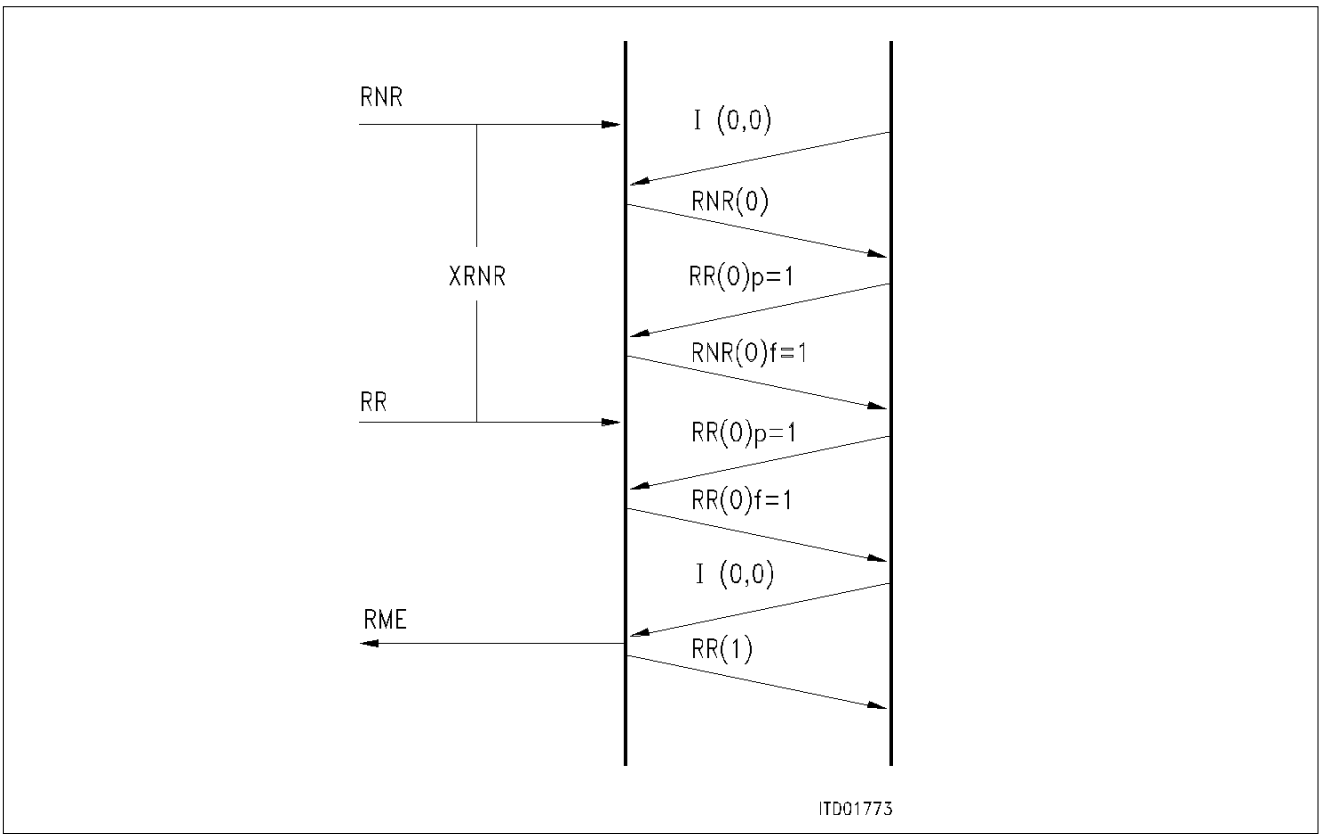
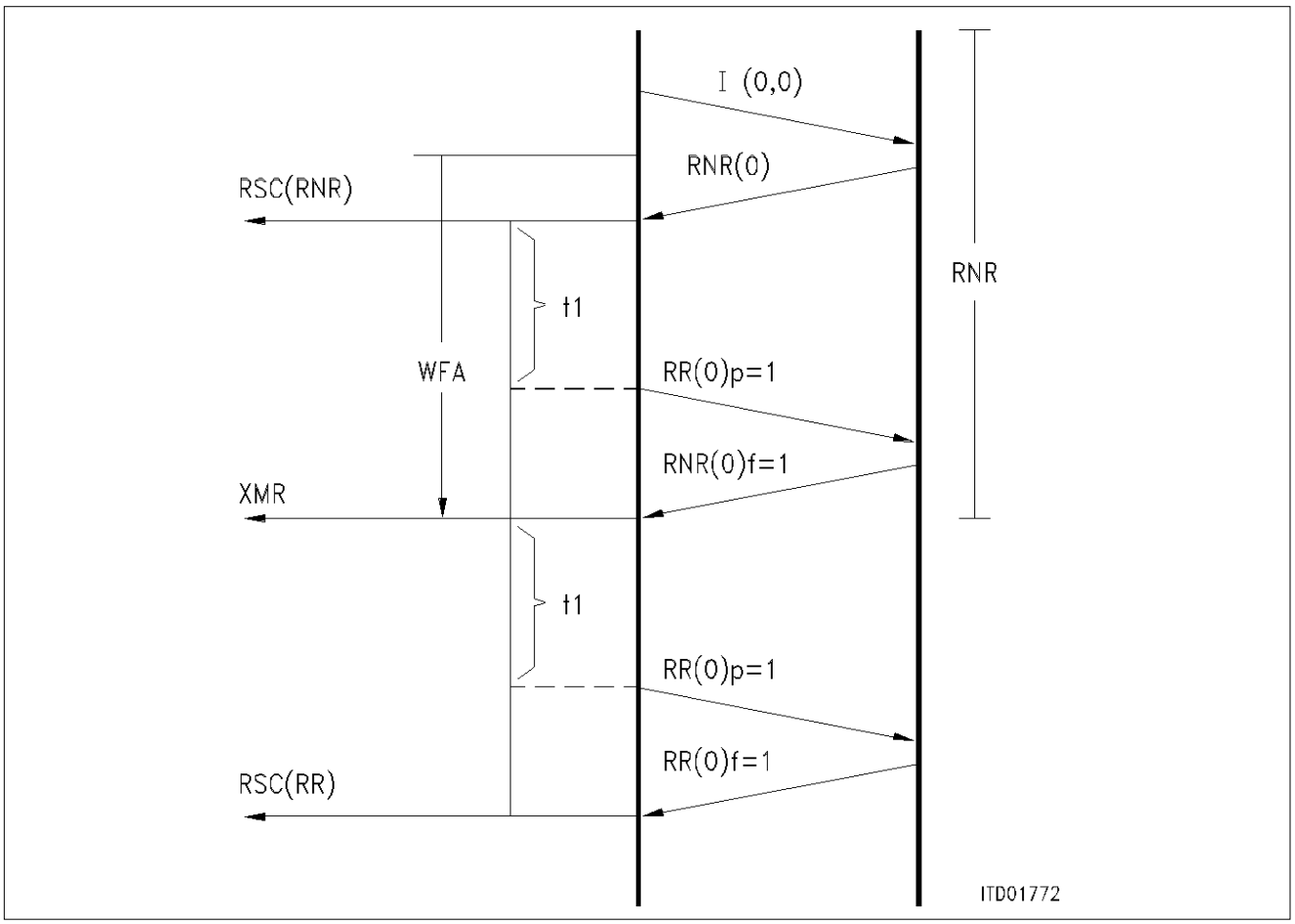


Figure 19
Flow Control with RR/RNR: Receiving I Frame


I (0,0)
RNR(0)
RSC(RNR)
RNR
t1
WFA
RR(0)p=1
RNR(0)f=1
XMR
t1
RR(0)p=1
RR(0)f=1
RSC(RR)
ITD01772

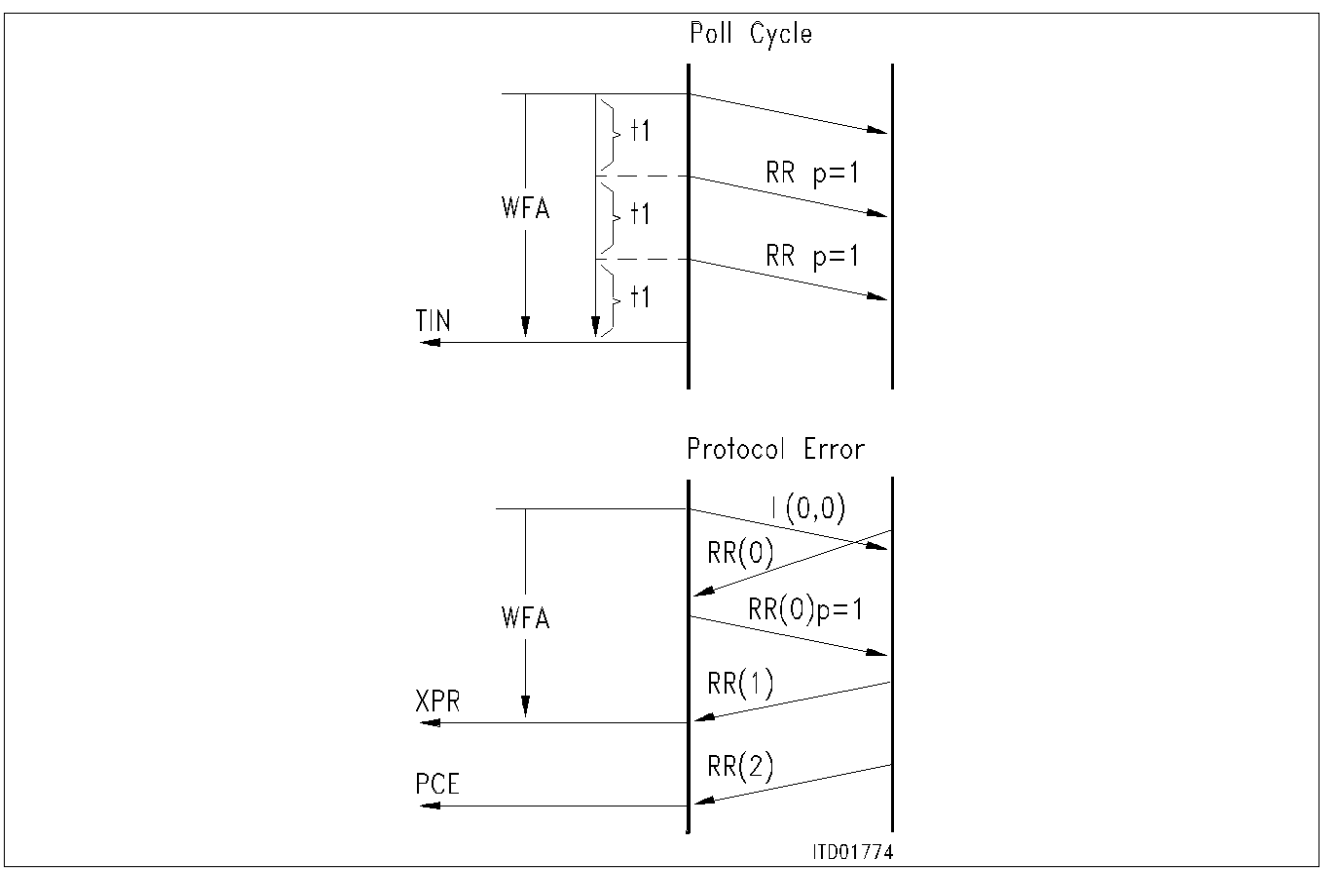

Poll Cycle
t1
RR p=1
WFA
t1
RR p=1
t1
TIN
Protocol Error
I (0,0)
RR(0)
RR(0)p=1
WFA
RR(1)
XPR
RR(2)
PCE
ITD01774

Figure 20

5 Special Functions

5.1 Bus Operation

The balanced procedure with LAPD in a point-to-multipoint configuration is effectively supported by the bus implemented in the HSCC. The component autonomously performs a bus access procedure with collision detection and rotating priorities. As a result, any number of transmitters can be connected to the serial bus configuration.

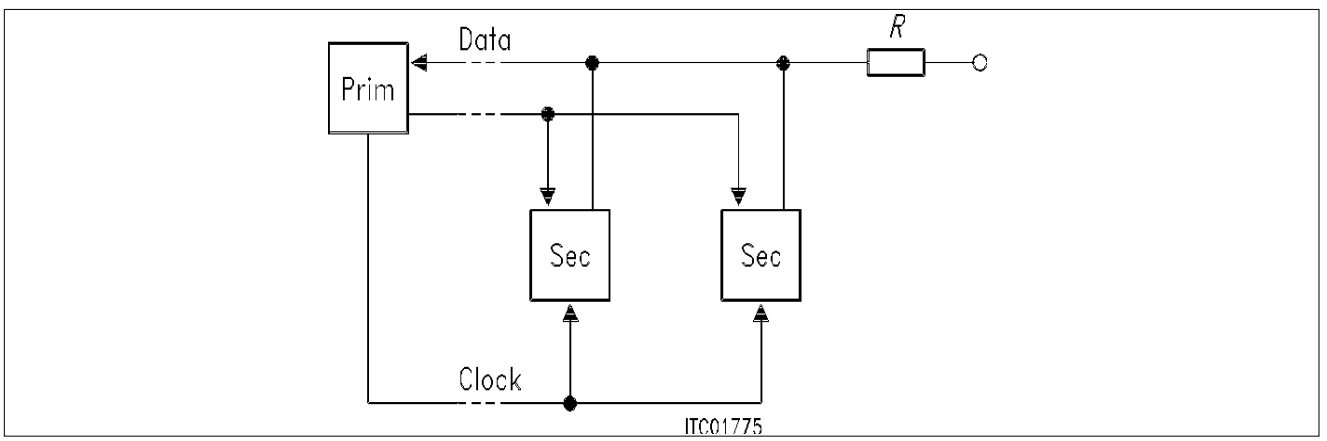


Figure 22
Bus Configuration, Point-to-Multipoint

Additionally, in the bus mode, "multimaster" configuration can be realized, which implies the possibility of communication between any two stations. This communication is autonomously controlled by the HSCC.

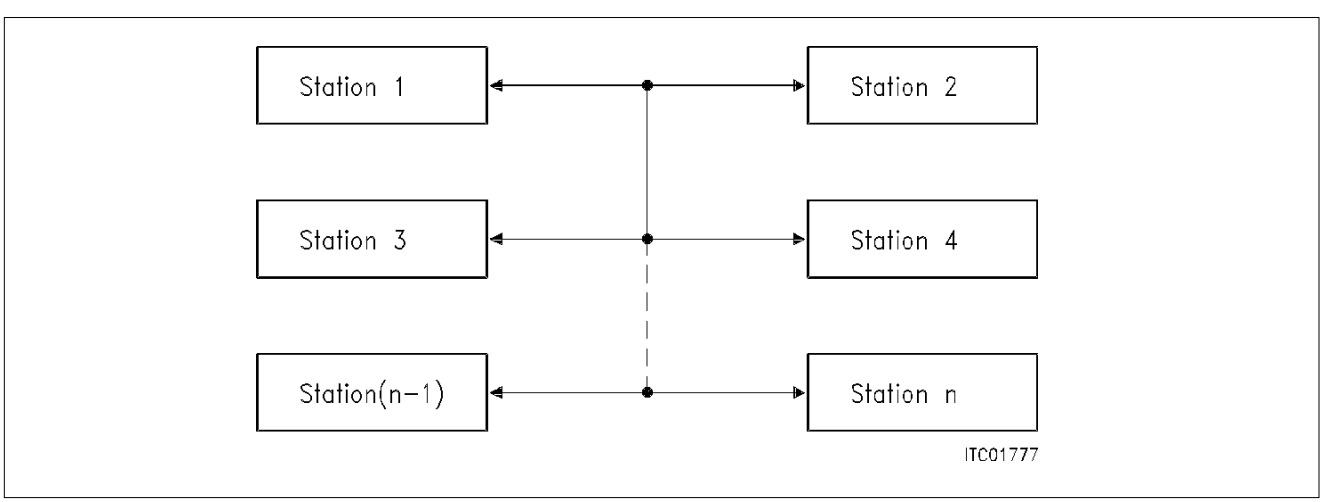


Figure 23
Bus Configuration, Multimaster

Prerequisites for bus operation
– central clock supply for all transmitters
– NRZ encoding
– OR connection of data at the bus
– feedback of bus information ($\overline{\text{CTSA}}$/$\overline{\text{CUTSB}}$ input)

The RTSA/RTSB output will in this case be active only when a frame is being transmitted. The signal is delayed by one clock period with respect to the data output TxDA/TxDB, and marks all data bits that could be transmitted without collision. In this way a configuration may be implemented in which the bus access is resolved on a local basis (collision bus) and where the data are sent one clock period later on a separate transmission line.

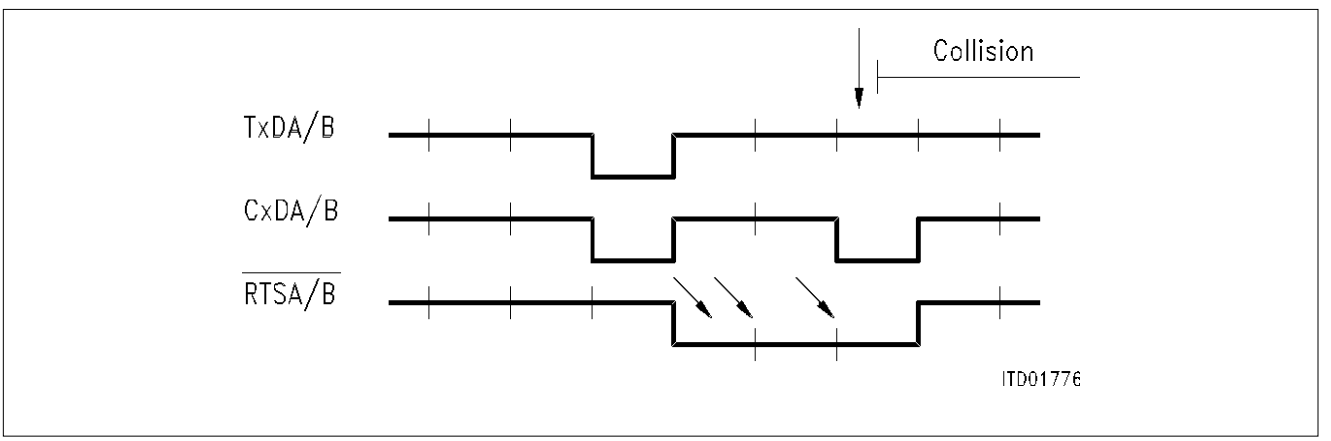


Figure 24
Request-to-Send in Bus Operation

Note: The bus mode can be operated independently of the clock mode, e.g. also during clock mode 1 (receive and transmission strobe) or clock mode 5 (programmable time slots).

Bus Access Procedure

The idle state of the bus is identified by eight or more successive 1's. In case of a transmit request in the HSCC, the frame is transmitted and the bus is identified as busy with the first zero of the opening flag (start flag).

After the frame has been transmitted, the bus becomes available again by transmitting 1's.

Note: If the bus is occupied by other transmitters and/or there is no transmit request in the HSCC, log 1 will be continuously transmitted at the TxDA/TxDB output.

Collisions

During the transmitting process, the data transmitted from the HSCC is compared with the data on the bus. In case an erroneous bit is detected (log 1 sent and log 0 detected, or vice versa) the frame is immediately aborted, and idle (log 1) is transmitted. Transmission will be initiated again by the HSCC as soon as possible.

Since a transmitted zero is given priority over a 1 due to the OR connection at the bus, and since the individually combined stations in the address field of the transmitted HDLC frame differ from one another, the fact that a collision has occurred will be detected prior to or at the latest within the address field. The frame of the transmitter with the highest temporary priority (address field) is not affected and is transmitted without interruptions. All other transmitters terminate their operation immediately.

Note: If a wired OR connection has been realized by an external pull-up resistor without decoupling, the data output (TxDA/TxDB) can be used as an open drain output and connected directly to the $\overline{\text{CTSA}}/\overline{\text{CTSB}}$ output.

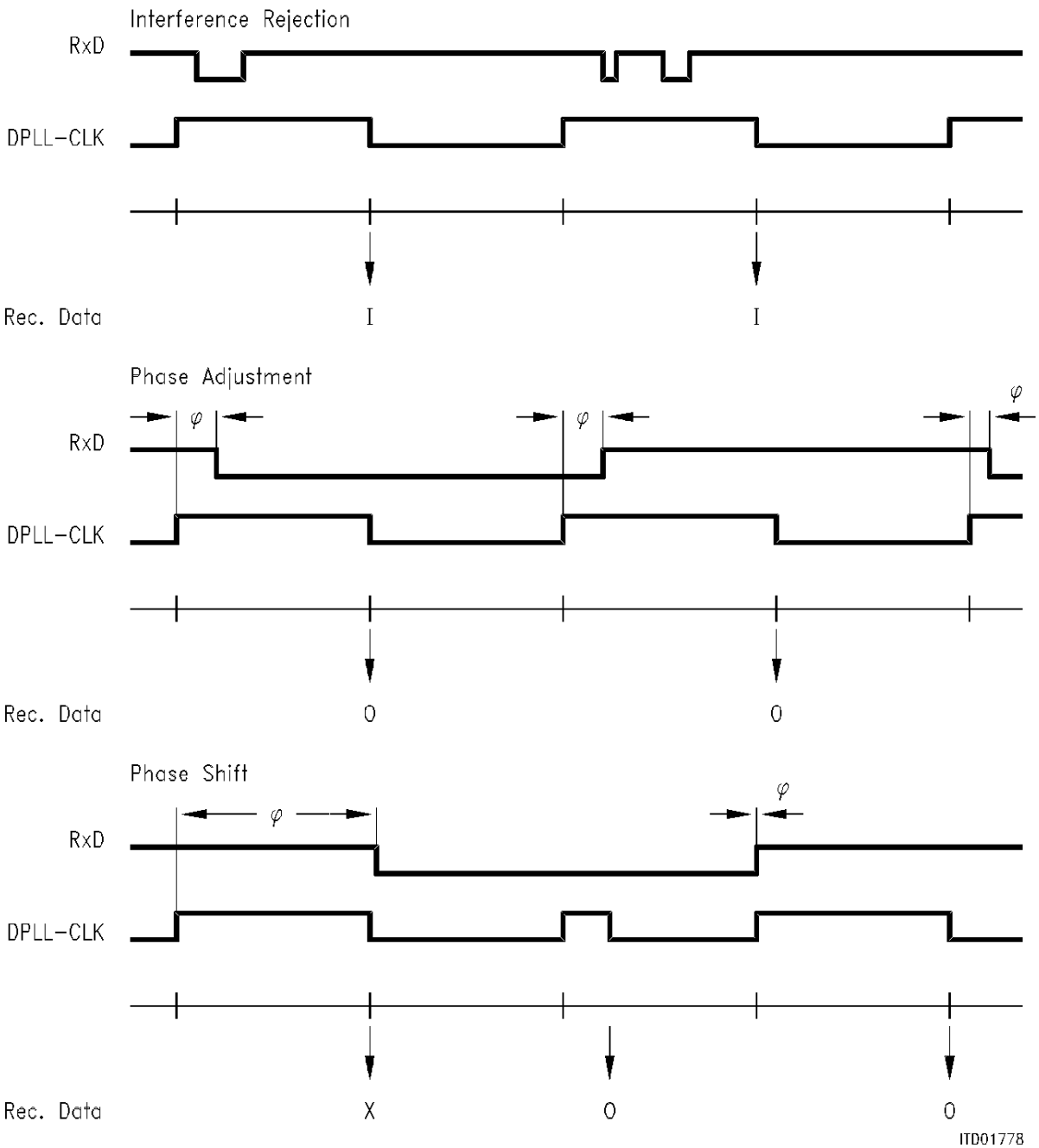


Figure 25
Synchronization of the Data Clock in DPLL Mode

Priority Principle

When an HDLC frame has been successfully transmitted by the HSCC, the priority is decremented. In order to transmit an additional frame, ten successive 1's must be present on the bus. This fact is used as a criterion to ensure that the higher priority transmitters do not contain any transmit requests. It is now possible to transmit a frame and the priority can be increased again (8 successive 1's). This method offers a priority allocation based on the selection of a particular address. It also ensures that each subscriber can access the bus at a pre-determinable time.

5.2 Baud Rate Generation

The internal baud rate generator adjusts the oscillator frequency in an external high-frequency clock to the reference clock required by the DPLL's. The required frequency ratio can be programmed as one of the following: 1, 2, 4, 6 . . . 2048, using the Baud Rate Generator Register (BGR) and the Timing Control Register (TCR).

5.3 DPLL Mode

The DPLL circuits implemented in the HSCC are optimized with respect to the HDLC protocol. The data clock is equal to the reference clock when divided by 16, the phase of the reference clock being synchronized to the received data stream. When using the NRZI encoding, the zero insert/zero delete method ensures that a sufficient number of edges occur in the data stream during the reception of an HDLC frame. The following functions have been implemented to faciliate a high-speed and reliable synchronization (**see figure 25**).

– Interference Rejection

In the case where two or more edges appear in the data stream within a time period of 16 reference clocks, these are detected as interference without performing additional adjustments.

– Phase Adjustment

In the case where an edge with a phase angle of $20^\circ < \varphi \leq 112^\circ$ appears in the data stream within the time window, the phase will be adjusted by $^1/_{16}$ of the data clock.

– Phase Shift

In the case where an edge with a phase angle of $112^\circ < \varphi \leq 180^\circ$ appears within the time window, a second transfer of the bit is forced and the phase is shifted by 180°.

These functions enable error-free reception of the HDLC frame in the data stream without preceding synchronization edges, since the first edge of the operating flag will suffice for synchronization.

5.4 Test Mode

To provide for fast and efficient testing, the HSCC can be operated in the test mode (MODE, TLP bit). The on-chip input and output are connected. As a result, the user can perform a self-test of the HDLC channels of the HSCC.

6 Detailed Register Description

The parameterization of the HSCC as well as the transfer of data and control information between the µC and the HSCC is performed for each channel with two FIFO's (RFIFO, XFIFO) and a set of registers. The addresses 00_H–$1F_H$ and 40_H– 5F have been reserved for accessing FIFO's. The addresses in this range are of equal value and refer to the current byte in the FIFO. As a result, performance oriented move string commands can be applied.

All HSCC registers may be accessed via even or odd CPU addresses, thus enabling a direct connection to the upper or lower half of a 16 bit microprocessor address/data bus.

6.1 Register Set HDLC Controller

Register Addresses

Addr$_H$		Read	Write	Refer to Page
Channel B	Channel A			
40 – 5F	00 – 1F	RFIFO	XFIFO	
30, B1	20, A1	ISTA	MASK	38
31, B0	21, A0	STAR	CMDR	39/40
32, B3	22, A3	MODE	MODE	41
33, B2	23, A2	TIMR	TIMR	42
34, B5	24, A5	EXIR	XAD1	39
35, B4	25, A4	RFBC	XAD2	42
36, B7	26, A7		RAH1	44
37, B6	27, A6	RSTA	RAH2	43/44
38, B9	28, A9	RAL1	RAL1	44
39, B8	29, A8	RHCR	RAL2	45

Control Registers

Interrupt Status Register (ISTA) Read – Address 20/30

Value after reset: 00_H

7								0
RME	RPF	RSC	XPR	TIN	ICA	EXA	EXB	

RME ... receive message end; one complete message ≤ 32 bytes or the last part of message > 32 bytes are in the receive FIFO.

RPF ... receive pool full; 32 bytes of a message are entered in the receive FIFO; message has not yet been completed.

RSC ... receive status change; change in status (receive ready/receive not ready) with respect to the opposite terminator was detected in the auto mode. Current status can be read from STAR (RRNR bit).

XPR ... transmit pool ready; one data block can be entered into the X-FIFO.

TIN ... timer interrupt; expiration of timer and repeat counter.

ICA ... interrupt of channel A; refers to the interrupt status register (ISTA) of channel A.

EXA ... extended interrupt of channel A; refers to the extended interrupt register (EXIR) of channel A.

EXB ... extended interrupt of channel B; refers to the extended interrupt register (EXIR) of channel B.

After the respective register has been read, ICA, EXA and EXB are deleted. All other bits are deleted after reading ISTA. To prevent erroneous functions, each bit is individually monitored and reset.

Note: Bit 2-0 is only used in ISTA/channel B.

Mask Register (MASK) Write – Address 20/30

Value after reset: 00_H

Each interrupt source can be selectively masked by setting the respective bit in MASK. Masked interrupts are not indicated when reading ISTA. Instead, they remain internally stored and will be indicated after the masking process has been terminated.

Note: In the event of an extended interrupt, no interrupt will be generated with a masked EXI bit, instead this bit is set in ISTA.

Extended Interrupt Register (EXIR) Read – Address 24/34

Value after reset: 00_H

7								0
XMR	XDU	PCE	RFO	CSC	0	0	0	

XMR ... transmit message repeat; message has to be repeated due to negative acknowledgement (auto mode) or collision detected after the 32nd data byte.

XDU ... transmit data underrun; transmitted frame was terminated with "idle". No additional data in the XFIFO.

Note: It is not possible to transmit transparent frames or I frames when an XMR or XDU interrupt is set.

PCE ... protocol error; indication of a protocol error in the auto mode. Either an S or I frame with an incorrect N (R), or an S frame with I field has been received.

RFO ... receive frame overflow; frame could not be stored due to occupied internal message buffer.

CSC ... clear-to-send change; if CIE bit is set (TCR) this bit indicates a change on $\overline{CTS}$ input. The actual value can be read from STAR.

Status Register (STAR) Read – Address 21/31

Value after reset: 48_H

7								0
XDOV	XFW	XRNR	RRNR	MBR	CEC	CTS	0	

XDOV ... transmit data overflow; more than 32 bytes have been written into the XFIFO.

XFW ... XFIFO write enable; data can be entered into the X FIFO.

XRNR ... transmit RNR; indication of the status of the HSCC in the auto mode.

RRNR ... received RNR; indication of the status of the remote station.

MBR ... message buffer ready; at least one more frame can be stored in the RFIFO.

CTS ... clear to send; if CIE bit is set (TCR) this bit indicates the state of the CTS input (inverted).

CEC ... command execution control; this bit is set during the time a command, written in CMDR, is executed.

Command Register (CMDR) Write – Address 21/31

Value after reset: 00_H

7							0
RMC	RHR	RNR	STI	XTF	XIF	XME	XRES

RMC ... receive message complete; reaction to RPF or RME interrupt. Current frame or data block was fetched by µC and can be deleted.

RHR ... reset HDLC receiver; HDLC receiver is reset. All data as well as the content of the message buffers are deleted. In the auto mode, the transmit and receive counters are reset as well.

RNR ... receive not ready; status of the ICC is set to "receive not ready" (log 1) and/or "receive ready" (log 0) (auto mode).

STI ... start timer; software timer is started.

XTF ... transmit transparent frame; transmission of a transparent frame is initiated.

XIF ... transmit I frame; transmission of an I frame is initiated.

XME ... transmit message end; last part of frame was entered in X FIFO.

XRES ... transmit reset; HDLC transmitter is reset, XFIFO is deleted and IDLE is transmitted.

Note: Execution of a command written in CMDR takes at most two and a half transmit clock periods. During this time CEC (STAR) is set and CMDR must not be written again.

Mode Register (Mode) R/W – Address 22/32

Value after reset: 00_H

7							0
MDS1	MDS0	ADM	TMD	RAC	RTS	TRS	TLP

MDS1-0 ... mode select; operating mode of HDLC controller is selected.
00 ... auto mode
01 ... non-auto mode
10 ... transparent mode
11 ... extended transparent mode

ADM ... address mode; one byte address field (log 0) or two byte address field (log 1) of the HDLC frame. Differentiation between extended transparent mode 0 and extended transparent mode 1 in the extended transparent mode.

RAC ... receiver active; receiver is activated (log 1) or deactivated (log 0).

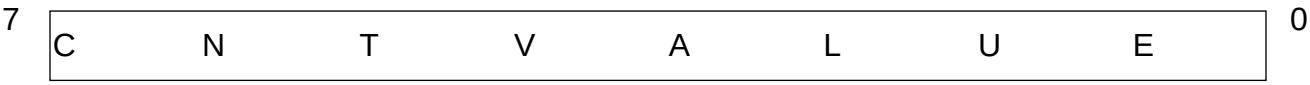
TMD ... timer mode; operating mode of the software timer is set. Internal mode (log 1) or external mode (log 0).

RTS ... request to send; $\overline{\text{RTS}}$ output is activated (log 1) or is autonomously controlled by the HSCC (log 0).

TRS ... timer resolution select; resolution of SW timer (factor *k*) is set to 2^{15} (log 0) and/or 2^9 (log 1) clock periods.

TLP ... test loop; input and output of HDLC channel are connected.

Time Register (TIMR) R/W – Address 23/33



VALUE ... Time period is set. The time period is $t_1 = k \times (\text{value} + 1) + \text{TCP}$
Factor k can be set for 2^{15} or 2^9 clock periods in MODE, TCP is the clock period of transmit data.

CNT ... count; interpreted in accordance with the selected operating mode.

Internal timer mode: CNT indicates the number of S commands (max. 6); in the case where an I frame is not acknowledged, these are autonomously transmitted by the HSCC after the expiration of time t_1. CNT = 7 indicates an unlimited number of S commands.

External timer mode: CNT plus VALUE indicates the time period t_2 after which the timer interrupt will be generated. The time period t_2 is:

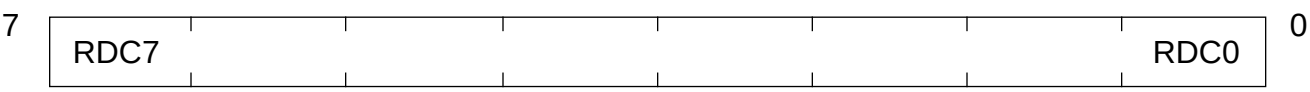
$t_2 = 32 \times k \times \text{CNT} \times \text{TCP} + t_1$

When CNT = 7, a timer interrupt is regularly generated after the expiration of t_1.

Note: Writing TIMR stops the timer, regardless of the timer mode.

Receive Frame Byte Counter (RFBC) Read – Address 25/35

Value after reset: 00_H



RDC7-0 receive data count: message length of received frame. RDC4-0 always indicates the length of data block available in the receive FIFO. When the messages exceed 223 bytes RDC7-5 is held at the value 7.

Receive Status Register (RSTA) Read – Address 27/37

7							0
RDA	RDO	CRC	RAB	HA1	HA0	C/R	LA

RDA ... data received; data are available in the receive FIFO

RDO ... receive data overflow; data overflow with current frame

CRC ... CRC compare; positive CRC comparison

RAB ... receive message aborted; received frame was aborted

HA1,
HA0 ... high byte address compare; identifier for address identification
10 ... RAH1
00 ... RAH2
01 ... group address (FE or FC)

Note: If the identical value is entered into RAH1 and RAH2, the combination 00 will be omitted.

C/R ... command-response; value of the C/R bit in the received frame.

LA ... low byte address compare; RAL1 (log1) or RAL2 (log 0) values have been recognized.

Note: In the transparent and extended transparent mode bit 0 is irrelevant; when AMD = 0 (mode) bits 1–3 are irrelevant.

Data Register

Receive FIFO (RFIFO) Read – Address 0/40

The received data can be read from the R FIFO after an RME or RPF interrupt.

Transmit FIFO (XFIFO) Write – Address 0/40

Data to be transmitted can be written into the X FIFO after an XPR interrupt.

Transmit Address 1 (XAD1) Write – Address 24/34

High address byte high of LAP processed in the auto mode. XAD1 will be interpreted as command in the one byte address mode.

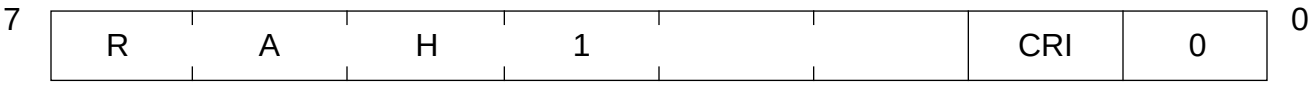
Note: In the two byte address mode bit 1 must be set to log 0.

Transmit Address 2 (XAD2) Write – Address 25/35

Low address byte low of LAP processed in the auto mode. XAD2 will be interpreted as command in the one byte address mode.

Note: In the two byte address mode bit 1 must be set to log 0.

Receive Address Byte High Register (RAH1) Write – Address 26/36



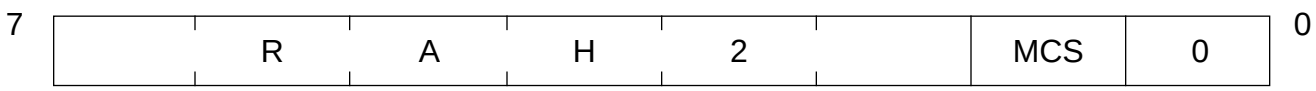
RAH1 ... value of the first individual address, higher byte.

CRI ... command-response bit interpretation: in the case of a two byte address in auto mode the C/R bit will be handled as follows:

	CRI = 1 C/R value	CRI = 0 C/R value
Commands rec	0	1
Responses rec	1	0
Commands trm	1	0
Responses trm	0	1

Note: In the case of a one-byte address RAH1 must be set to 00_H.

Receive Address Byte High Register (RAH2) Write – Address 27/37



RAH2 ... value of the second individual address, higher byte.

MCS ... modulo count select (valid in auto mode only).
The MCS bit determines the control field format according to HDLC
0: basic operation (modulo 8)
1: extended operation (modulo 128)

Receive Address Byte Low Register (RAL 1) R/W – Address 28/38

Value of the first address lower byte (auto, non-auto mode); in the case of a one byte address, interpreted as command. The received lower byte address (transparent mode), the first byte after the flag (extended transparent mode 1), or a data byte (extended transparent mode 1, with bypassing of the HDLC receiver) can be read out from this register. RAL1 can be written in auto/non-auto mode and it can be read in other modes.

Receive Address Byte Low Register (RAL 2) Write – Address 29/39

Value of the second individual address, lower byte (auto, non-auto mode), with a one byte address interpreted as response.

Receive HDLC Control Register (RHCR) Read – Address 29/39

Value of the received HDLC control field; in the transparent mode 0 value of the second byte after the flag.

When modulo 128 is selected (MCS bit of RAH2) in auto mode, the RHCR register contains compressed information of the extended control field, making it similar to a modulo 8 control field.
Bit 0 of the RHCR register has the following meaning:
0 $\rightarrow$ an I-frame has been received
1 $\rightarrow$ a U-frame has been received.
(S-frames will be handled autonomously by the HSCC).

When message transfer modes other than the auto mode are used and a HDLC protocol is used with "modulo 128", then the first octet of the extended control field is available in the RHCR register. The second octet is available in the RFIFO in accordance with to the message transfer mode.

In extended transparent mode 0 (no address recognition) RHCR contains the second byte of a received frame after the opening flag.

6.2 Common Register

Register Addresses

Addr$_H$	Read	Write
2B, AA		BGR
2C, AD	TCR	TCR
2D, AC		TSAR
2E, AB		TSAX
2F, AE	CCR	CCR

Description of Registers

Common Configuration Register (CCR) R/W – Address 2 F

Value after reset: 00_H

7								0
	PU	SC1	SC0	0DS	LSS	CM2	CM1	CM0

PU ... power up; switch-over between power-up and power-down mode.

SC1,
SC0 ... serial port configuration (**see page 23**)

00 ... point-to-point configuration, NRZ encoding

10 ... point-to-point configuration, NRZI encoding

01 ... bus configuration, timing mode 1

11 ... bus configuration, timing mode 2

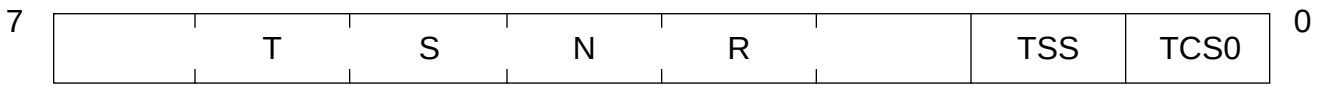
Note: In the bus mode, only NRZ encoding can be used.

0DS ... output driver select; the serial data outputs (T×DA, T×DB) are operated as push-pull (log 1) or open drain outputs (log 0).

LSS ... line sync select; in the idle state non shared zero flags (log 1) or idle (log 0) will be output at the serial data outputs.

CM2-0 ... clocking mode; setting of the clock modes 0 – 7 (**see page 17**).

Time-Slot Assignment Register Receive (TSAR) Write – Address 2 D

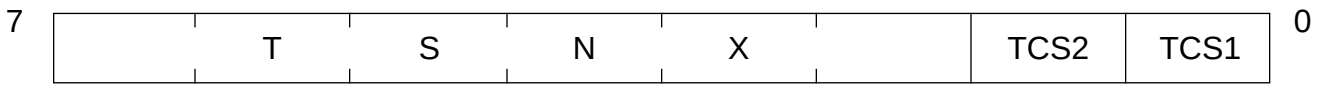


TSNR ... time-slot number receive; number of the receive time slot.

TSS ... time-slot select; 32 time slots in the frame (log 1) or 64 (log 0).

TCS0 ... clock shift 0; setting of the clock shift in transmit direction, bit 0.

Time-Slot Assignment Register Transmit (TSAX) Write – Address 2 E



TSNX ... time-slot number transmit; number of the transmit time slot (00_H–$3F_H$)

TCS2, TCS1 ... clock shift; setting of the clock shift in transmit direction, bit 2 and bit 1 (**see page 20**).

Timing Control Register (TCR) R/W – Address 2 C

Value after reset: 00_H
The effect of TCR depends on the clock mode.

Clock mode 5

7							0
RCS2	RCS1	RCS0	CCS	TI0	CIE	0	0

Clock mode 2, 6

7							0
BR9	BR8	BDF	TSS	TI0	CIE	0	0

Clock mode 3, 4, 7

7							0
BR9	BR8	BDF	0	TI0	CIE	0	0

Clock mode 0, 1

7							0
0	0	0	0	0	CIE	0	0

RCS 2-0 ... receive clock shift; timing shift of receive data

Note: The value of RCS2-0 must be set whenever a reset has been applied to the device.

CCS ... channel capacity select; 56 kbit (log 1) or 64 kbit channels (log 0) will be transmitted.

BR9-8 ... baud rate, bit 9–8

BDF ... baud rate division factor; the division factor of the baud rate generator is one (log 0) or is adjusted by BR9–0 (log 1).

TSS ... transmit clock source select; the source for the transmit clock is T×CLK A/ T×CLK B (log 0), or the baud rate generator output frequency divided by 16 (log 1).

TI0 ... transmit clock input/output switch; T×CLK A/ T×CLK B pins are inputs (log 0) or output (log 1).

Note: In clock mode 5 only T×CLK B can be programmed as output.

CIE ... clear to send interrupt enable; CSC interrupt (EXIR) is masked (log 0) or not (log 1).

Baud Rate Generator Register (BGR) Write – Address 2 B

BR7							BR0

BR7-0 ... baud rate, bit 7–0; will determine, along with BR9, BR8, the division factor of the baud rate generator. Supposing value N (0 ... 1023) has been programmed, the division factor is $k = 2 * (N + 1)$.

7 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Storage temperature	T_{stg}	– 65	125	˚C
Operating temperature: SAB 82520	T_A	0	70	˚C
Operating temperature: SAF 82520	T_A	– 40	85	˚C
Voltage at any pin vs. ground	V_S	– 0.4	V_{CC} + 0.4	V

DC Characteristics

SAB 82520 : T_A = 0 to 70 ˚C; V_{CC} = 5 V ±10 %; GND = 0 V
SAF 82520 : T_A = – 40 to 85 ˚C; V_{CC} = 5 V ±5 %; GND = 0 V

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
L-input voltage	V_{IL}	V_{CC}–0.4		0.8	V	
H-input voltage	V_{IH}	2.0		V_{CC}+0.	V	
L-output voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
H-output voltage	V_{OH}	2.4			V	I_{OH} = – 400 µA
		V_{CC}–0.5	V_{CC}		V	I_{OH} = – 100 µA
Input leakage current	I_{IL}	– 10		10	µA	V_{IN} = V_{CC} to 0 V
Output leakage current	I_{OL}	– 10		10	µA	V_{OUT} = V_{CC} to 0 V
V_{CC} supply current						
p. d.	I_{CC}		0.5	1.8	mA	
p. u.	I_{CC}		5	7	mA	V_{CC} = 5 V C_p = 4 MHz Inputs at V_{SS}/V_{CC} No output loads

Capacitance

T_A = 25 ˚C; V_{CC} = GND = 0 V

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Input Capacitance f_C = 1 MHz	C_{IN}		5	10	pF
Input/output capacitance	$C_{I/O}$		10	20	pF
Output capacitance unmeasured pins returned to GND	C_{OUT}		8	15	pF

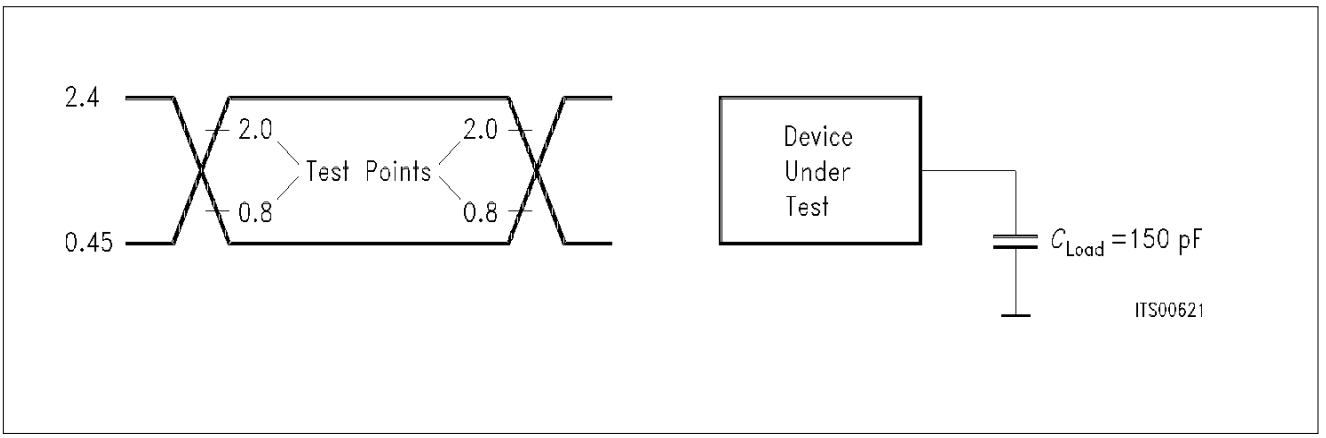


Figure 26
AC Testing Input, Output Waveform **AC Testing Load Circuit**

AC Testing

Inputs are driven at 2.4 V for logic "1" and 0.45 V for logic "0".
Timing measurements are made at 2.0 V for logic "1" and at 0.8 V for logic "0".

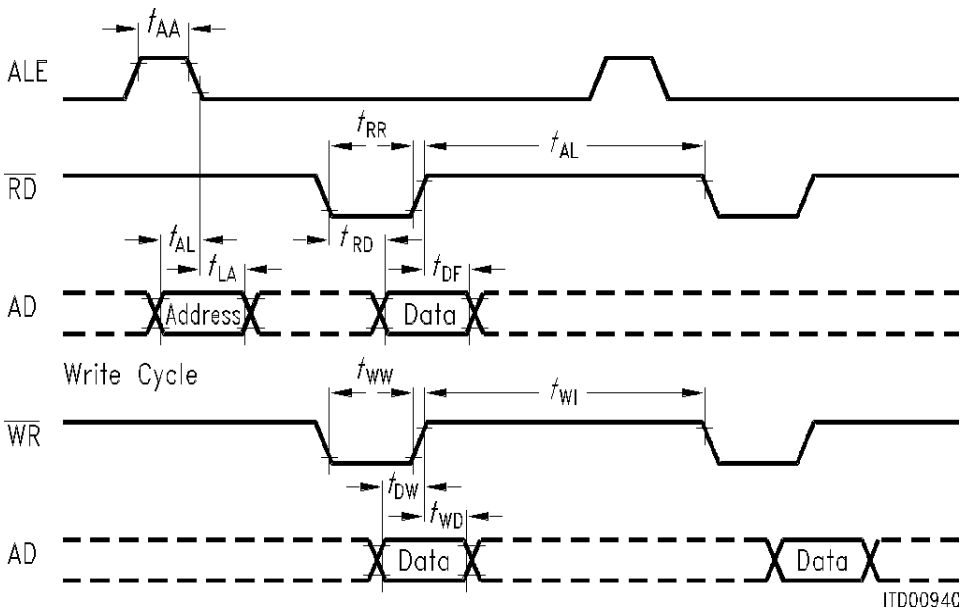


Figure 27
µP Interface Timing
Read Cycle

Read Cycle

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address hold after ALE	t_{LA}	25		ns
Address to ALE setup	t_{AL}	20		ns
Data delay from RD	t_{RD}		110	ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Output float delay	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	60		ns
ALE pulse width	t_{AA}	50		ns

Write Cycle

Parameter	Symbol	Limit Values		Unit
		min.	max.	
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup to $\overline{WR}$	t_{DW}	30		ns
Data hold after $\overline{WR}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	60		ns

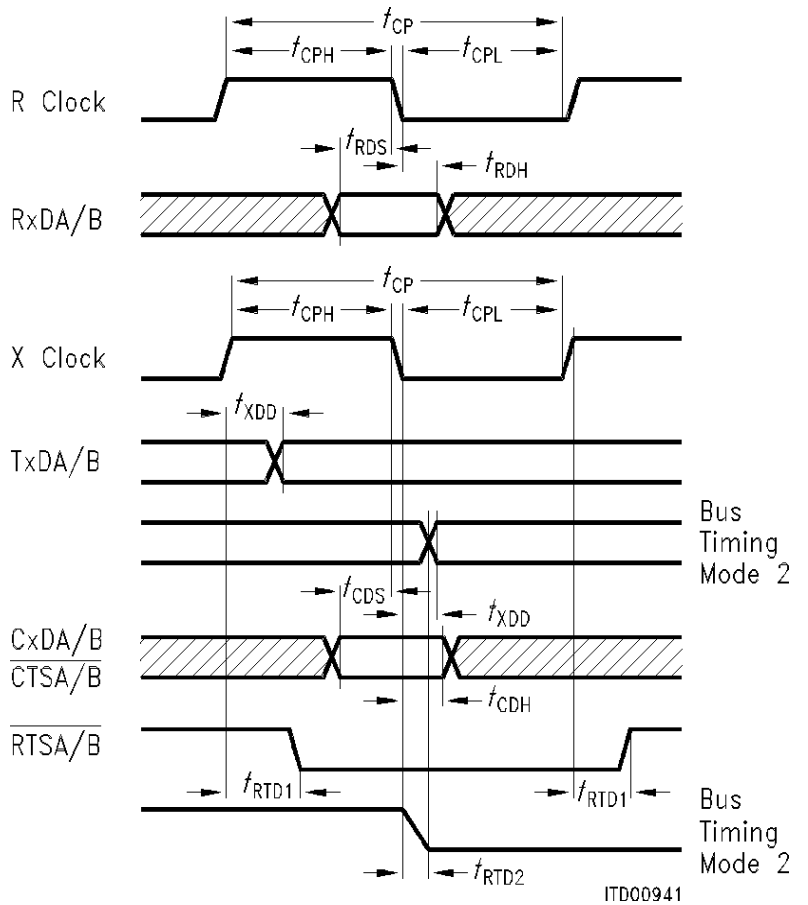


Figure 28
Serial Interface Timing

DC Characteristics

SAB 82520 : T_A = 0 to 70 °C; V_{CC} = 5 V ±10 %; GND = 0 V
SAF 82520 : T_A = – 40 to 85 °C; V_{CC} = 5 V ±5 %; GND = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Receive data setup Receive data hold	t_{RDS} t_{RDH}	0 30		ns ns
Collision data setup Collision data hold	t_{CDS} t_{CDH}	0 30		ns ns
Transmit data delay	t_{XDD}	20	68	ns
Request to send delay 1 Request to send delay 2	$t_{RTD\,1}$ $t_{RTD\,2}$	30 20	130 85	ns ns
Clock period	t_{CP}	240		ns
Clock period Low Clock period High	t_{CPL} t_{CPH}	90 100		ns ns

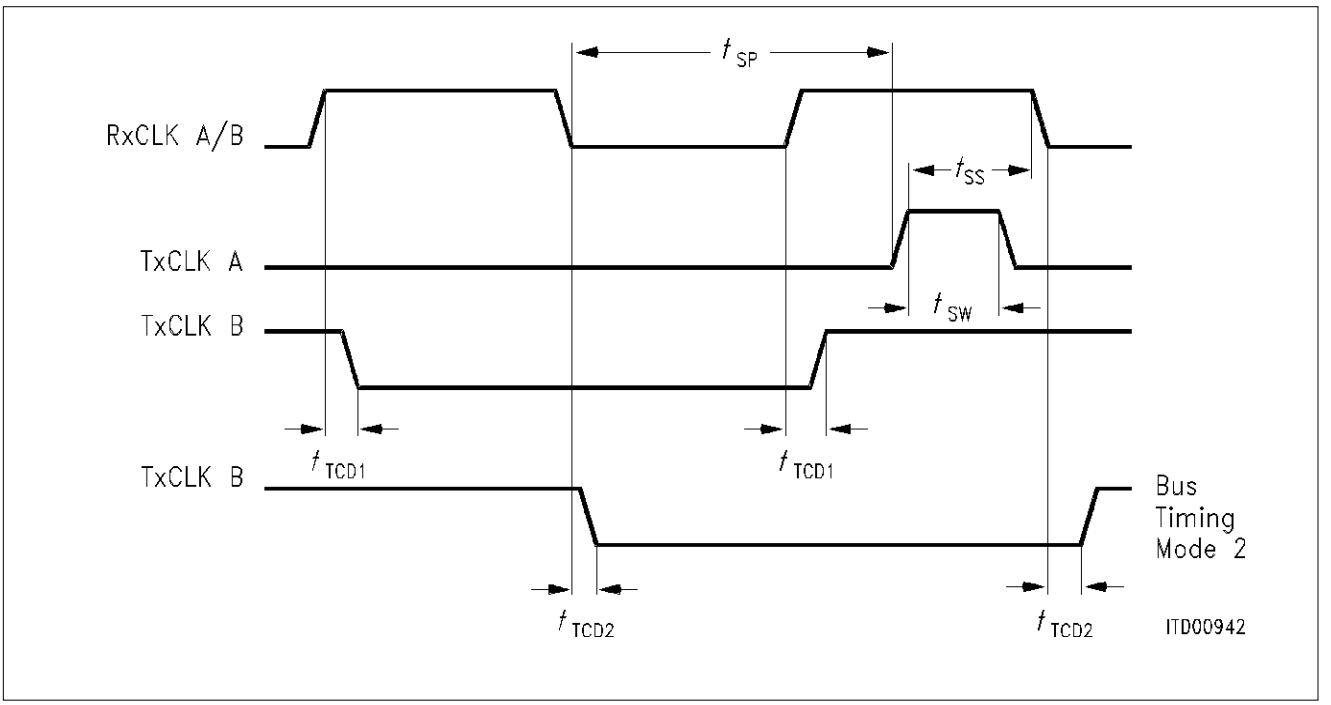


Figure 29
Clock Mode 5

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Sync pulse delay	t_{SD}	30		ns
Sync pulse setup	t_{SS}	30		ns
Sync pulse width	t_{SW}	40		ns
Time-slot control 2 delay	$t_{TCD\,2}$	20	95	ns
Time-slot control 1 delay	$t_{RCD\,1}$	30	120	ns

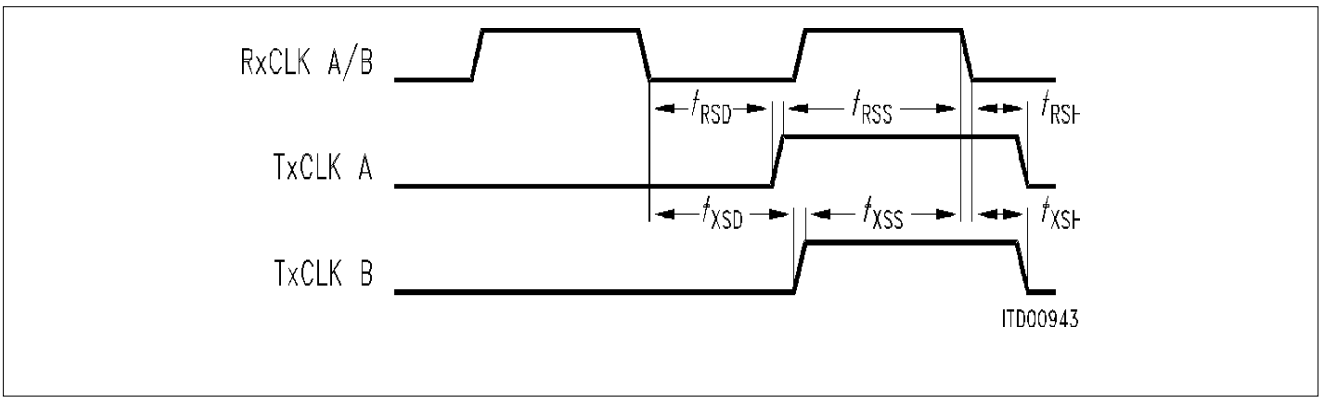


Figure 30
Clock Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Receive strobe delay	t_{RSD}	30		ns
Receive strobe setup	t_{RSS}	70		ns
Receive strobe hold	t_{RSH}	30		ns
Transmit strobe delay	t_{XSD}	30		ns
Transmit strobe setup	t_{XSS}	90		ns
Transmit strobe hold	t_{XSH}	30		ns

Clock Mode 2, 3, 6, 7

Internal Clocking

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency Baudrate generator used	f_{CLK}		12.3	MHz
Clock frequency Baudrate generator not used	f_{CLK}		19.3	MHz

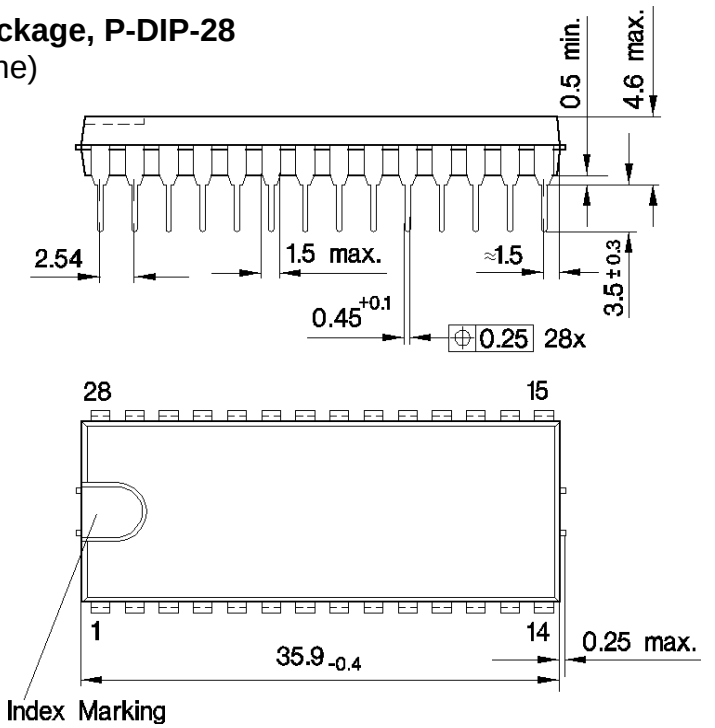
RESET Timing

RES Characteristics

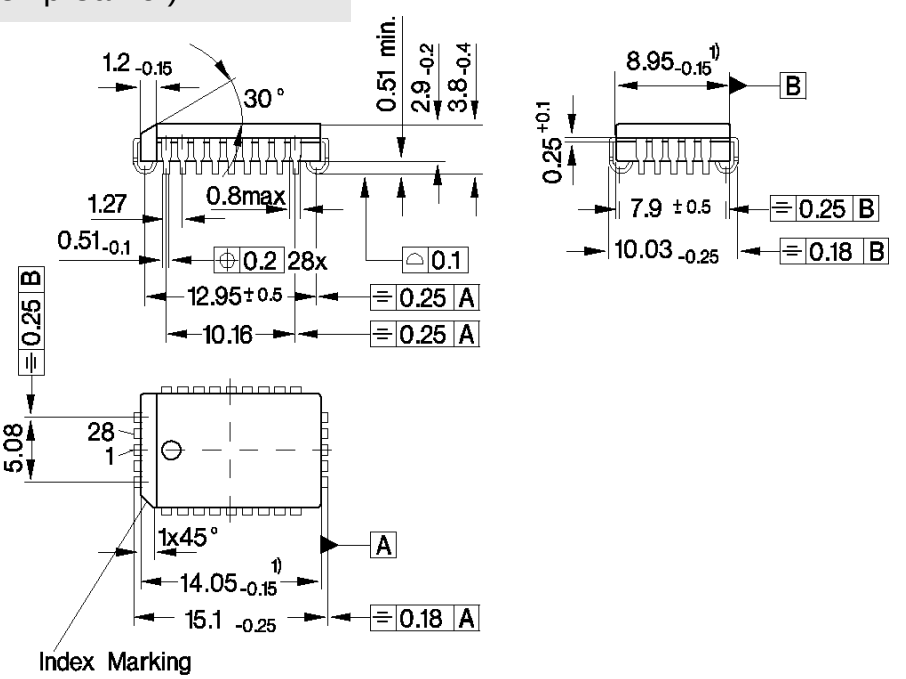
Parameter	Symbol	Limit Values		Unit
		min.	max.	
RES HIGH	t_{RWH}	1800		ns

8 Package Outlines

Plastic Package, P-DIP-28
(Dual-in-Line)



Plastic Package, P-LCC-28-R (SMD)
(Plastic-Leaded Chip Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm