DATA SHEET

SAA7184; SAA7185B
Digital Video Encoders (DENC2-M6)

Preliminary specification
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Digital Video Encoders (DENC2-M6) SAA7184; SAA7185B

FEATURES

- CMOS 5 V device
- Digital PAL/NTSC encoder
- System pixel frequency 13.5 MHz
- Accepts MPEG decoded data
- 8-bit wide MPEG port
- Input data format Cb, Y, Cr etc. (CCIR 656)
- 16-bit wide YUV input port
- I^2C-bus control port or alternatively MPU parallel control port
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- OVL overlay with Look-Up Tables (LUTs) 8×3 bytes
- Colour bar generator
- Line 21 closed caption encoder
- Cross-colour reduction
- Macrovision revision_6 Pay-per-View copy protection system as option (SAA7184 only). **Remark**: This device is protected by U.S. patent numbers 4631603 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anticopy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductors sales office for more information.
- DACs operating at 27 MHz with 10-bit resolution
- Controlled rise and fall times of output syncs and blanking
- Down-mode of DACs
- CVBS and S-Video output simultaneously
- PLCC68 package.

GENERAL DESCRIPTION

The SAA7184 and SAA7185B digital video encoders 2 (DENC2-M6) encode digital YUV video data to an NTSC or PAL CVBS or S-Video signal.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data. The device includes a sync/clock generator and on-chip Digital-to-Analog Converters (DACs).

The circuit is compatible to the DIG-TV2 chip family.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7184WP	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2
SAA7185BWP			

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	50	55	mA
I_{DDD}	digital supply current	–	130	170	mA
V_i	input signal voltage levels	TTL compatible			V
$V_{o(p-p)}$	analog output signal voltages Y, C and CVBS without load (peak-to-peak value)	–	2	–	V
R_L	load resistance	80	–	–	Ω
ILE	LF integral linearity error	–	–	±2	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

BLOCK DIAGRAM

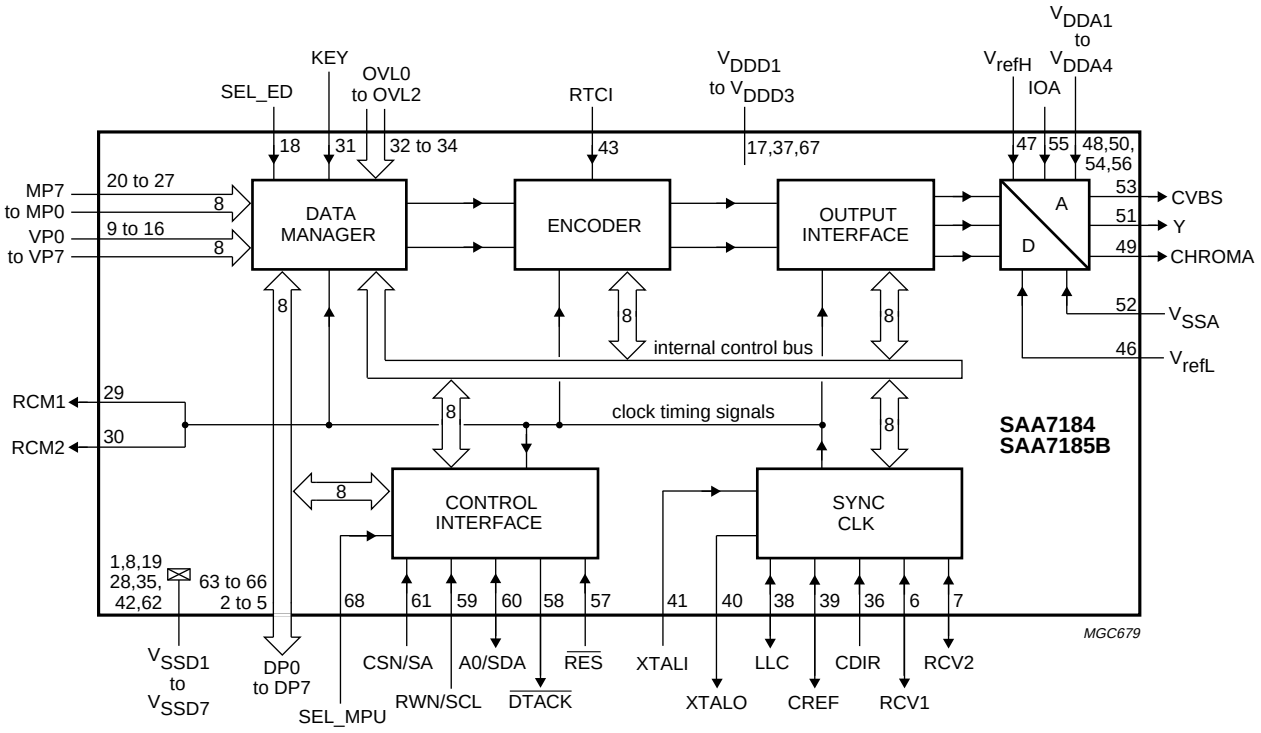


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
V_{SSD1}	1	–	digital ground 1
DP4 to DP7	2 to 5	I/O	Upper 4 bits of the data port; if pin 68 (SEL_MPU) is HIGH, the data bus of the parallel MPU interface is used. If pin 68 is LOW, then the UV lines of the video port are used.
RCV1	6	I/O	Raster control 1 for video port; depending on the synchronization mode, this pin receives or provides a VS/FS/FSEQ signal.
RCV2	7	I/O	Raster control 2 for video port; depending on the synchronization mode, this pin receives or provides an HS/HREF/CBL signal.
V_{SSD2}	8	–	digital ground 2
VP0 to VP7	9 to 16	I	Video port; this is an input for CCIR 656 compatible multiplexed video data. If the 16-bit DIG-TV2 format is used, then Y data is input.
V_{DDD1}	17	I	digital supply voltage 1
SEL_ED	18	I	select encoder data; selects input data either from the MPEG port or from the video port
V_{SSD3}	19	–	digital ground 3
MP7 to MP0	20 to 27	I	MPEG port; it is an input for CCIR 656 style multiplexed YUV data.
V_{SSD4}	28	–	digital ground 4
RCM1	29	O	Raster control 1 for MPEG port; this pin provides a VS/FS/FSEQ signal.
RCM2	30	O	Raster control 2 for MPEG port; this pin provides an HS pulse for the MPEG decoder.
KEY	31	I	key signal for OVL (active HIGH)
OVL0 to OVL2	32 to 34	I	on-screen display data; this is the index for the internal OVL look-up tables
V_{SSD5}	35	–	digital ground 5
CDIR	36	I	Clock direction; if the CDIR input is HIGH, the circuit receives a clock signal, if not LLC and CREF are generated by the internal crystal oscillator.
V_{DDD2}	37	I	digital supply voltage 2
LLC	38	I/O	Line-locked clock; this is the 27 MHz master clock for the encoder. The direction is set by the CDIR pin.
CREF	39	I/O	Clock reference signal; this is the clock qualifier for DIG-TV2 compatible signals. The polarity is programmable by software.
XTALO	40	O	crystal oscillator output (to crystal)
XTALI	41	I	Crystal oscillator input (from crystal). If the oscillator is not used, this pin should be connected to ground.
V_{SSD6}	42	–	digital ground 6
RTCI	43	I	Real time control Input; if the clock is provided by the SAA7151B or SAA7111, RTCI should be connected to the RTCO pin of the decoder to improve the signal quality.
AP	44	–	test pin (should be connected to digital ground for normal operation)
SP	45	–	test pin (should be connected to digital ground for normal operation)
V_{refL}	46	I	lower reference voltage input for the DACs
V_{refH}	47	I	upper reference voltage input for the DACs
V_{DDA1}	48	I	analog positive supply voltage 1 for the DACs and output amplifiers

SYMBOL	PIN	I/O	DESCRIPTION
CHROMA	49	O	analog output of the chrominance signal
V_{DDA2}	50	I	analog supply voltage 2 for the DACs and output amplifiers
Y	51	O	analog output of the luminance signal
V_{SSA}	52	–	analog ground for the DACs and output amplifiers
CVBS	53	O	analog output of the CVBS signal
V_{DDA3}	54	I	analog supply voltage 3 for the DACs and output amplifiers
IOA	55	I	current input for the output amplifiers (connected via a 15 kΩ resistor to V_{DDA})
V_{DDA4}	56	I	analog supply voltage 4 for the DACs and output amplifiers
$\overline{RES}$	57	I	Reset input, active LOW. After reset is applied, all outputs are in 3-state input mode. The I²C-bus receiver waits for the start condition.
$\overline{DTACK}$	58	O	Data acknowledge output of the parallel MPU interface, active LOW, otherwise high impedance.
RWN/SCL	59	I	If pin 68 (SEL_MPU) is HIGH, this is the read/write signal of the parallel MPU interface. Otherwise it is the I²C-bus serial clock input.
A0/SDA	60	I/O	If pin 68 (SEL_MPU) is HIGH, this is the address signal of the parallel MPU interface. Otherwise it is the I²C-bus serial data input/output.
CSN/SA	61	I	If pin 68 (SEL_MPU) is HIGH, this is the chip select signal of the parallel MPU interface. Otherwise it is the I²C-bus slave address select pin. When LOW slave address = 88H, when HIGH slave address = 8CH.
V_{SSD7}	62	–	digital ground 7
DP0 to DP3	63 to 66	I/O	Lower 4 bits of the data port; if pin 68 (SEL_MPU) is HIGH, the data bus of the parallel MPU interface is used. If pin 68 is LOW, then the UV lines of the video port are used.
V_{DDD3}	67	I	digital supply voltage 3
SEL_MPU	68	I	Select MPU interface input; if it is HIGH, the parallel MPU interface is active, if not the I²C-bus interface will be used.

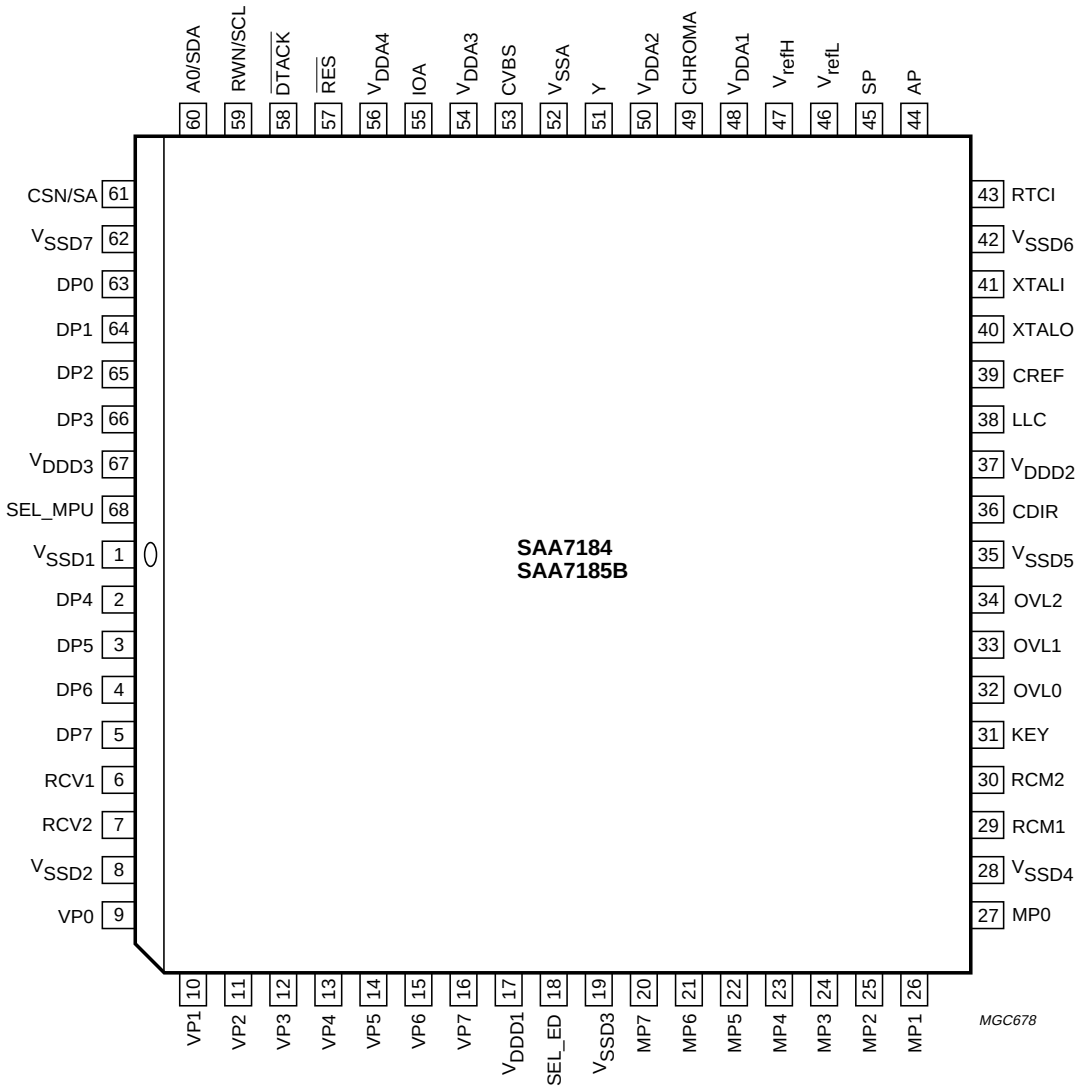


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The digital MPEG-compatible video encoder (DENC2-M6) encodes digital luminance and chrominance into analog CVBS and S-Video (Y/C) signals simultaneously. NTSC-M and PAL B/G standards and sub-standards are also supported.

The basic encoder function consists of subcarrier generation and colour modulation plus insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements of RS-170-A and CCIR 624.

For ease of analog post filtering the signals are twice oversampled, with respect to the pixel clock, before digital-to-analog conversion.

For total filter transfer characteristics see Figs 3, 4, 5 and 6. The DACs are realized with full 10-bit resolution. The encoder provides three 8-bit wide data ports that serve different applications.

The MPEG port and the video port accept 8 lines multiplexed Cb-Y-Cr data.

The video port is also able to accommodate DIG-TV2 family compatible 16-bit YUV signals. In this event, the data port is used for the U/V components.

Alternatively, the data port can accommodate the data of an 8-bit wide microprocessor interface.

The 8-bit multiplexed Cb-Y-Cr formats are CCIR 656 (D1 format) compatible, but the SAV, EAV etc. codes are not decoded.

A crystal-stable master clock (LLC) of 27 MHz, which is twice the CCIR line-locked pixel clock frequency of 13.5 MHz, needs to be supplied externally. A crystal oscillator input/output pair of pins and an on-chip clock driver are provided optionally. It is also possible to connect the Philips Digital Video Decoder (SAA7111 or SAA7151B) in conjunction with a CREF clock qualifier to the DENC2-M6 via the RETCI pin (connected to RTCO) of a decoder. Information concerning the actual subcarrier, PAL-ID and (with SAA7111) definite subcarrier phase can be inserted.

The DENC2-M6 synthesizes all necessary internal signals, colour subcarrier frequency and synchronization signals, from that clock. The DENC2-M6 is always the timing master for the MPEG port but can also be configured as master or slave for the video port.

The IC also contains closed caption and extended data services encoding (line 21), and supports anti-taping signal generation in accordance with Macrovision.
It also supports OVL via KEY and 3-bit overlay techniques using a 24×8 LUT.

The IC can be programmed via the I^2C-bus or via the 8-bit MPU interface, but only one interface configuration can be active at a time. If the 16-bit video port mode (VP and DP) is being used, only the I^2C-bus interface can be selected.

A number of possibilities are provided for setting the different video parameters such as:

- black and blanking level control
- colour subcarrier frequency
- black variable burst amplitude etc.

During reset ($\overline{RES}$ = LOW) and after reset is released, all digital I/O stages are set to the input mode. A reset forces the control interfaces to abort any running bus transfer and to set register 3AH to contents 1FH, register 61H to contents 06H, and registers 6CH and 7AH to contents 00H. All other control registers are not influenced by a reset.

Data manager

Real time arbitration on the data stream to be encoded is performed in the data manager.

Depending on the hardware conditions (signals on pins SEL_ED, KEY, OVL2 to OVL0, MP7 to MP0, VP7 to VP0 and DP7 to DP0) and different software programming, either data from the MP port, from the VP port or from the OVL port, is selected to be encoded to CVBS and Y/C signals.

Optionally, the OVL colour look-up tables located in this block can be read out in a pre-defined sequence (8 steps per active video line) thereby achieving, for example, a colour bar test pattern generator without the need for an external data source. The colour bar function is only under software control.

Encoder

VIDEO PATH

The encoder generates luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y/C signals, from the Y, U and V baseband signals.

The luminance gain and offset are modified (offset being programmable within a certain range to enable different black level set-ups). After the signals have been inserted, a fixed synchronization level in accordance with standard composite synchronization schemes and blanking level, (also programmable in a certain range to allow for manipulations with Macrovision anti-tapping) additional insertion of AGC super white pulses (programmable in height) is supported.

In order to enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, thereby providing luminance in a 10-bit resolution. This filter is also used to define smoothed transients for synchronization pulses and blanking period. The transfer characteristics of the luminance interpolation filter are illustrated in Figs 5 and 6.

The chrominance gain is modified (programmable separately for U and V), a standard dependent burst is inserted before baseband colour signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thereby providing a higher colour bandwidth, which can be used for the Y/C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figs 3 and 4.

The amplitude of the inserted burst is programmable within a certain range, suitable for standard signals and for special effects. Colour in a 10-bit resolution is provided on the subcarrier after the succeeding quadrature modulator.

The numeric ratio between Y and C outputs is in accordance with set standards.

CLOSED CAPTION ENCODER

Using the closed caption encoder circuit, data in accordance with the specification of closed caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field) are possible, each pair preceded by run-in clocks and framing code.

The actual line number where data is to be encoded, can be modified within a certain range.

The data clock frequency is in accordance with the definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode closed caption data for 50 Hz field frequencies at 32 times horizontal line frequency.

Output interface

In the output interface, encoded Y and C signals are converted from digital to analog in a 10-bit resolution and then combined into a 10-bit CVBS signal. Also, in front of the summation point, the luminance signal can be fed through a further filter stage (optional), thereby suppressing components in the subcarrier frequency range. Thus, a type of cross colour reduction is provided, which is useful in a standard TV set with CVBS input.

The slopes of the synchronization pulses are not affected with any active cross colour reduction.

Three different filter characteristics or bypass are available, see Fig.5.

The CVBS output occurs with the same processing delay as the Y and C outputs. Absolute amplitudes at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

Outputs of all DACs can be set together, via software control, to minimum output voltage for either purpose.

Synchronization

The synchronization of the DENC2 is able to operate in two modes; slave mode and master mode.

In the slave mode, the circuit accepts synchronization pulses at the bidirectional RCV1 port. The timing and trigger behaviour, related to the video signal on VP (and DP, if used), can be influenced by programming the polarity and on-chip delay of RCV1. The active slope of RCV1 defines the vertical phase and, as an option, the odd/even and colour frame phase to be initialized. It can also be used to set the horizontal phase.

If the horizontal phase is not to be influenced by RCV1, a horizontal pulse needs to be applied at pin RCV2. Timing and trigger behaviour can also be influenced for RCV2.

If there are missing pulses at RCV1 and/or RCV2, the time base of the DENC2-M6 will become free-running, thus an arbitrary number of synchronization slopes may miss, but no additional pulses must occur (such as with wrong phase).

If the vertical and horizontal phase is derived from RCV1, RCV2 can be used for horizontal or composite blanking input or output.

In the master mode, the time base of the circuit is continuously free-running. At the RCV1 port, the IC can output:

- A vertical sync signal (VS) with 3 or 2.5 lines duration, or
- An odd/even signal which is LOW in odd fields, or
- A field sequence signal (FSEQ) which is HIGH in the first of 4 respectively 8 fields.

The IC can provide a horizontal pulse with programmable start and stop phase at the RCV2 port. This pulse can be inhibited in the vertical blanking period to build up, for example, a composite blanking signal.

The phase of the output pulses at RCV1 or RCV2 are referenced to the VP port, polarity of both signals is selectable.

The DENC2-M6 is **always** the timing master for the source at the MP input. The IC provides two signals for synchronizing this source:

1. At the RCM1 port the same signals as at RCV1 (as output) are available.
2. At RCM2 the IC provides a horizontal pulse with programmable start and stop phase.

The start and end of the active part can be programmed. The active part of a field always starts at the beginning of a line if the standard blanking option SBLBN is not set.

Control interface

DENC2-M6 contains two control interfaces, an I^{2}C-bus slave transceiver and an 8-bit parallel microprocessor interface. The interfaces cannot be used simultaneously.

The I^{2}C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write only, except one status byte which can be read.

Two I^{2}C-bus slave addresses can be selected (pin SEL_MPU must be LOW):

88H: pin 61 = LOW

8CH: pin 61 = HIGH.

The parallel interface is defined by:

D7 to D0 data bus

$\overline{CS}$ active LOW chip select signal

R$\overline{W}$ read/write signal, LOW for a write cycle

$\overline{DTACK}$ 680xx style data acknowledge (handshake), active-LOW

A0 register select, LOW selects address, HIGH selects data.

The parallel interface uses two registers, one auto-incremental containing the current address of a control register (equals subaddress with I^{2}C-bus control), and one containing actual data. The currently addressed register is mapped to the corresponding control register.

The status byte can be read (optionally) via a read access to the address register, no other read access is provided.

Input levels and formats

DENC2-M6 accepts digital YUV data with levels (digital codes) in accordance with CCIR 601.

Deviating amplitudes in the colour difference signals can be compensated for by independent gain control setting, while the gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The MPEG port accepts only 8-bit multiplexed CCIR 656 compatible data.

If the I^{2}C-bus interface is used, the VP port can accommodate both formats, 8-bit multiplexed Cb-Y-Cr data on the VP lines, or the 16-bit DTV2 format with the Y signal on the VP lines and the UV signal on the DP port.

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

Table 1 CCIR signal component levels

SIGNAL	IRE	DIGITAL LEVEL	CODE
Y	0	16	straight binary
	50	126	
	100	235	
Cb	bottom peak	16	straight binary
	colourless	128	
	top peak	240	
Cr	bottom peak	16	straight binary
	colourless	128	
	top peak	240	

Table 2 8-bit multiplexed format (similar to CCIR 656)

TIME	0	1	2	2	4	5	6	7
Sample	Cb_0	Y_0	Cr_0	Y_1	Cb_2	Y_2	Cr_2	Y_3
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Table 3 16-bit multiplexed format (DTV2 format)

TIME	0	1	2	3	4	5	6	7
Sample Y line	Y_0		Y_1		Y_2		Y_3	
Sample UV line	Cb_0		Cr_0		Cb_2		Cr_2	
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Bit allocation map

Table 4 Slave receiver (slave address 88h or 8Ch)

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE (note 1)							
		D7	D6	D5	D4	D3	D2	D1	D0
Null	00	0	0	0	0	0	0	0	0
	↓	↓							
Null	39	0	0	0	0	0	0	0	0
Input port control	3A	CBENB	0	0	V656	VY2C	VUV2C	MY2C	MUV2C
OVL LUT Y0	42	OVLY07	OVLY06	OVLY05	OVLY04	OVLY03	OVLY02	OVLY01	OVLY00
OVL LUT U0	43	OVLU07	OVLU06	OVLU05	OVLU04	OVLU03	OVLU02	OVLU01	OVLU00
OVL LUT V0	44	OVLV07	OVLV06	OVLV05	OVLV04	OVLV03	OVLV02	OVLV01	OVLV00
	↓	↓							
OVL LUT Y7	57	OVLY77	OVLY76	OVLY75	OVLY74	OVLY73	OVLY72	OVLY71	OVLY70
OVL LUT U7	58	OVLU77	OVLU76	OVLU75	OVLU74	OVLU73	OVLU72	OVLU71	OVLU70
OVL LUT V7	59	OVLV77	OVLV76	OVLV75	OVLV74	OVLV73	OVLV72	OVLV71	OVLV70
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	0	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level	5E	GAINV8	0	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
Null	60	0	0	0	0	0	0	0	0
Standard control	61	0	DOWN	INPI1	YGS	RTCE	SCBW	PAL	FISE
Burst amplitude	62	DECTYP	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
Encoder control, CC line	6B	MODIN1	MODIN0	PCREF	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
RCV port control	6C	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE (note 1)							
		D7	D6	D5	D4	D3	D2	D1	D0
RCM, CC mode	6D	0	0	0	0	SRCM11	SRCM10	CCEN1	CCEN0
Horizontal trigger	6E	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Horizontal trigger	6F	HTRIG8	HTRIG9	HTRIG10	0	0	0	0	0
f_{SC} reset mode, Vertical trigger	70	PHRES1	PHRES0	SBLBN	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Begin MP request	71	BMRQ7	BMRQ6	BMRQ5	BMRQ4	BMRQ3	BMRQ2	BMRQ1	BMRQ0
End MP request	72	EMRQ7	EMRQ6	EMRQ5	EMRQ4	EMRQ3	EMRQ2	EMRQ1	EMRQ0
MSBs MP request	73	0	EMRQ10	EMRQ09	EMRQ08	0	BMRQ10	BMRQ09	BMRQ08
Null	74	0	0	0	0	0	0	0	0
Null	75	0	0	0	0	0	0	0	0
Null	76	0	0	0	0	0	0	0	0
Begin RCV2 output	77	BRCV7	BRCV6	BRCV5	BRCV4	BRCV3	BRCV2	BRCV1	BRCV0
End RCV2 output	78	ERCV7	ERCV6	ERCV5	ERCV4	ERCV3	ERCV2	ERCV1	ERCV0
MSBs RCV2 output	79	0	ERCV10	ERCV09	ERCV08	0	BRCV10	BRCV09	BRCV08
Field length	7A	0	0	0	0	0	0	FLC1	FLC0
First active line	7B	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7C	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
MSBs field control	7D	0	0	LAL8	FAL8	0	0	0	0

Note

1. All bits labelled ‘0’ are reserved. They **must** be programmed with logic 0.

I²C-bus format

Table 5 I²C-bus address; see Table 6

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 6 Explanation of Table 5

PART	DESCRIPTION
S	START condition
Slave address	1 0 0 0 1 0 0 X or 1 0 0 0 1 1 0 X (note 1)
ACK	acknowledge, generated by the slave
Subaddress (note 2)	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read, no subaddressing with read.
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Slave Receiver

Table 7 Subaddress 3A

DATA BYTE	LOGIC LEVEL	DESCRIPTION
MUV2C	0	Cb/Cr data at MP is two's complement.
	1	Cb/Cr data at MP is straight binary. Default after reset.
MY2C	0	Y data at MP is two's complement.
	1	Y data at MP is straight binary. Default after reset.
VUV2C	0	Cb/Cr data input to VP or DP is two's complement
	1	Cb/Cr data input to VP or DP is straight binary. Default after reset.
VY2C	0	Y data input to VP is two's complement
	1	Y data input to VP is straight binary. Default after reset.
V656	0	selects YUV 422 format on VP (8 lines Y) and DP (8 lines multiplexed Cb/Cr).
	1	selects CCIR 656 compatible format on VP (8 lines Cb, Y, Cr). Default after reset.
CBENB	0	data from input ports is encoded. Default after reset.
	1	colour bar with programmable colours (entries of OVL_LUTs) is encoded. The LUTs are read in upward order from index 0 to index 7.

Table 8 Subaddress 42 to 59

COLOUR	DATA BYTE(1)			INDEX(2)
	OVLY	OVLU	OVLV	
White	107 (6BH)	0 (00H)	0 (00H)	0
	107 (6BH)	0 (00H)	0 (00H)	
Yellow	82 (52H)	144 (90H)	18 (12H)	1
	34 (22H)	172 (ACH)	14 (0EH)	
Cyan	42 (2AH)	38 (26H)	144 (90H)	2
	03 (03H)	29 (1DH)	172 (ACH)	
Green	17 (11H)	182 (B6H)	162 (A2H)	3
	240 (F0H)	200 (C8H)	185 (B9H)	
Magenta	234 (EAH)	74 (4AH)	94 (5EH)	4
	212 (D4H)	56 (38H)	71 (47H)	
Red	209 (D1H)	218 (DAH)	112 (70H)	5
	193 (C1H)	227 (E3H)	84 (54H)	
Blue	169 (A9H)	112 (70H)	238 (EEH)	6
	163 (A3H)	84 (54h)	242 (F2H)	
Black	144 (90H)	0 (00H)	0 (00H)	7
	144 (90H)	0 (00H)	0 (00H)	

Notes

1. Contents of OVL look-up tables. All 8 entries are 8-bits. Data representation is in accordance with *CCIR 601* (Y, Cb, Cr), but two's complement, e.g. for a $^{100}/_{100}$ (upper number) or $^{100}/_{75}$ (lower number) colour bar.
2. For normal colour bar with CBENB = logic 1.

Table 9 Subaddress 5A

DATA BYTE	DESCRIPTION
CHPS	phase of encoded colour subcarrier (including burst) relative to horizontal sync. Can be adjusted in steps of 360/256 degrees.

Table 10 Subaddress 5B and 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for Cb signal; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE(1)	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE(2)	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal

Notes

1. GAINU = –2.17 × nominal to +2.16 × nominal.
2. GAINU = –2.05 × nominal to +2.04 × nominal.

Table 11 Subaddress 5C and 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for Cr signal; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE[1]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE[2]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal

Notes

1. GAINV = –1.55 × nominal to + 0.55 × nominal.
2. GAINV = –1.46 × nominal to + 0.46 × nominal.

Table 12 Subaddress 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation in accordance with *"CCIR 601"*	white-to-sync = 140 IRE[1]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 49 IRE
		white-to-sync = 143 IRE[2]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 50 IRE

Notes

1. Output black level/IRE = BLCKL × 25/63 + 24; recommended value: BLCKL = 60 (3CH) normal.
2. Output black level/IRE = BLCKL × 26/63 + 24; recommended value: BLCKL = 45 (2DH) normal.

Table 13 Subaddress 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE[1]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 42 IRE
		white-to-sync = 143 IRE[2]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 43 IRE

Notes

1. Output black level/IRE = BLNNL × 25/63 + 17; recommended value: BLNNL = 58 (3AH) normal.
2. Output black level/IRE = BLNNL × 26/63 + 17; recommended value: BLNNL = 63 (3FH) normal.

Table 14 Subaddress 5F (CCRS and BLNVB; note 1)

DATA BYTE		FUNCTION
CCRS1	CCRS0	
0	0	no cross colour reduction (for overall transfer characteristic of luminance see Fig.5)
0	1	cross colour reduction #1 active (for overall transfer characteristic see Fig.5)
1	0	cross colour reduction #2 active (for overall transfer characteristic see Fig.5)
1	1	cross colour reduction #3 active (for overall transfer characteristic see Fig.5)

Note

1. BLNVB = vertical blanking level during vertical blanking interval and its value is typically identical to BLNNL.

Table 15 Subaddress 61

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FISE	0	864 total pixel clocks per line. Default after reset.
	1	858 total pixel clocks per line
PAL	0	NTSC encoding (non-alternating V component)
	1	PAL encoding (alternating V component). Default after reset.
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4)
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4). Default after reset.
RTCE	0	no real time control of generated subcarrier frequency. Default after reset.
	1	real time control of generated subcarrier frequency through SAA7151B or SAA7111 (see Fig.9)
YGS	0	luminance gain for white – black 100 IRE. Default after reset.
	1	luminance gain for white – black 92.5 IRE including 7.5 IRE set-up of black
INPI	0	PAL switch phase is nominal. Default after reset.
	1	PAL switch phase is inverted compared to nominal
DOWN	0	DACs in normal operational mode. Default after reset.
	1	DACs forced to lowest output voltage

Table 16 Subaddress 62

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BSTA	amplitude of colour burst; input representation in accordance with *CCIR 601*	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 1.25 × nominal(1) white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 1.76 × nominal(2) white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.20 × nominal(3) white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 1.67 × nominal(4)	
DECTYP	real time control input (RTCI)	logic 0	control from SAA7151B digital colour decoder
		logic 1	control from SAA7111 video input processor (VIP)

Notes

1. Recommended value: BSTA = 102 (66H).
2. Recommended value: BSTA = 72 (48H).
3. Recommended value: BSTA = 106 (6AH).
4. Recommended value: BSTA = 75 (4BH).

Table 17 Subaddress 63 to 66 (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency)	$FSC = round\left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$ see note 1	FSC3 = most significant byte FSC0 = least significant byte

Note

1. Examples:
   a) NTSC-M: f_{fsc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F07C1FH).
   b) PAL-B/G: f_{fsc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A098ACBH).

Table 18 Subaddress 67 to 6A

DATA BYTE[1]	DESCRIPTION
L21O0	first byte of captioning data, odd field
L21O1	second byte of captioning data, odd field
L21E0	first byte of extended data, even field
L21E1	second byte of extended data, even field

Note

1. LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format.

Table 19 Subaddress 6B

DATA BYTE	DESCRIPTION
SCCLN	selects the actual line, where closed caption or extended data is encoded; see note 1
MODIN	defines video data of MP port or VP (DP) port to be encoded; see Table 20
PCREF	0 = normal polarity of CREF for DIG TV2 compatible input signals; 1 = inverted

Note

1. Line = (SCCLN + 4) for M systems; line = (SCCLN + 1) for other systems.

Table 20 Logic levels and function of MODIN

DATA BYTE		FUNCTION
MODIN1	MODIN0	
0	0	unconditionally from MP port
0	1	from MP port, if pin SEL_ED = HIGH; otherwise from VP port
1	0	unconditionally from VP port
1	1	from VP port, if pin SEL_ED = HIGH; otherwise from MP port

Table 21 Subaddress 6C

DATA BYTE	LOGIC LEVEL	DESCRIPTION
PRCV2	0	polarity of RCV2 as output is active HIGH, rising edge is taken when input, respectively. Default after reset
	1	polarity of RCV2 as output is active LOW, falling edge is taken when input, respectively
ORCV2	0	pin RCV2 is switched to input. Default after reset
	1	pin RCV2 is switched to output
CBLF	0	if ORCV2 = HIGH, pin RCV2 provides an HREF signal (Horizontal Reference Pulse that is defined by RCV2S and RCV2E, also during vertical blanking Interval). Default after reset if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1). Default after reset
	1	if ORCV2 = HIGH, pin RCV2 provides a ‘composite blanking not’ signal i.e. a reference pulse that is defined by RCV2S and RCV2E, excluding vertical blanking Interval, which is defined by FAL and LAL (PRCV2 must be LOW) if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1) and as an internal blanking signal
PRCV1	0	polarity of RCV1 as output is active HIGH, rising edge is taken when input, respectively. Default after reset
	1	polarity of RCV1 as output is active LOW, falling edge is taken when input, respectively
ORCV1	0	pin RCV1 is switched to input. Default after reset
	1	pin RCV1 is switched to output
TRCV2	0	horizontal synchronization is taken from RCV1 port. Default after reset
	1	horizontal synchronization is taken from RCV2 port
SRCV1	–	defines signal type on pin RCV1; see Table 22

Table 22 Logic levels and function of SRCV1

DATA BYTE		AS OUTPUT	AS INPUT	FUNCTION
SRCV11	SRCV10			
0	0	VS	VS	vertical sync each field. Default after reset
0	1	FS	FS	frame sync (odd/even)
1	0	FSEQ	FSEQ	field sequence, vertical sync every fourth field (PAL = 0) or eighth field (PAL = 1)
1	1	not applicable	not applicable	

Table 23 Subaddress 6D

DATA BYTE	DESCRIPTION
CCEN	enables individual line 21 encoding; see Table 24
SRCM	defines signal type on pin RCM1; see Table 25

Table 24 Logic levels and function of CCEN

DATA BYTE		FUNCTION
CCEN1	CCEN0	
0	0	line 21 encoding OFF
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 25 Logic levels and function of SRCM

DATA BYTE		AS OUTPUT	FUNCTION
SRCM1	SRCM0		
0	0	VS	vertical sync each field
0	1	FS	frame sync (odd/even)
1	0	FSEQ	field sequence, vertical sync every fourth field (FISE = 1) or eighth field (FISE = 0)
1	1	not applicable	

Table 26 Subaddress 6E to 6F

DATA BYTE	DESCRIPTION
HTRIG	sets the horizontal trigger phase related to signal on RCV1 or RCV2 input values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed increasing HTRIG decreases delays of all internally generated timing signals reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = 037H

Table 27 Subaddress 70

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VTRIG	–	sets the vertical trigger phase related to signal on RCV1 input increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines variation range of VTRIG = 0 to 31 (1FH)
SBLBN	0	vertical blanking is defined by programming of FAL and LAL
	1	vertical blanking is forced in accordance with CCIR-624 (50 Hz) or RS170A (60 Hz); note 1
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 28

Note

1. If cross-colour reduction is programmed, it is active between FAL and LAL in both events.

Table 28 Logic levels and function of PHRES

DATA BYTE		FUNCTION
PHRES1	PHRES0	
0	0	no reset or reset via RTCI from SAA7111 if bit RTCE = 1
0	1	reset every two lines
1	0	reset every eight fields
1	1	reset every four fields

Table 29 Subaddress 71 to 73

DATA BYTE	DESCRIPTION
BMRQ	beginning of MP request signal (RCM2) values above 1715 (FISE = 1) or 1727 [FISE = 0] are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCM2) at BMRQ = 0F9H [117H]
EMRQ	end of MP request signal (RCM2) values above 1715 (FISE = 1) or 1727 [FISE = 0] are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCM2) at EMRQ = 683H [691H]

Table 30 Subaddress 77 to 79

DATA BYTE	DESCRIPTION
BRCV	beginning of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 [FISE = 0] are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at BRCV = 0F9H [117H]
ERCV	end of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at ERCV = 683H [691H]

Table 31 Subaddress 7A

DATA BYTE		DESCRIPTION
FLC1	FLC0	
0	0	field length control interlaced 312.5 lines/fields at 50 Hz, 262.5 lines/fields at 60 Hz (reset default)
0	1	field length control non-interlaced 312 lines/fields at 50 Hz, 262 lines/fields at 60 Hz
1	0	field length control non-interlaced 313 lines/fields at 50 Hz, 262 lines/fields at 60 Hz
1	1	field length control non-interlaced 313 lines/fields at 50 Hz, 262 lines/fields at 60 Hz

Table 32 Subaddress 7B to 7D

DATA BYTE	DESCRIPTION
FAL	first active line = FAL + 4 for M systems; = FAL + 1 for other systems, measured in lines FAL = 0 coincides with the first field synchronization pulse
LAL	last active line = LAL + 3 for M systems; = LAL for other systems, measured in lines LAL = 0 coincides with the first field synchronization pulse

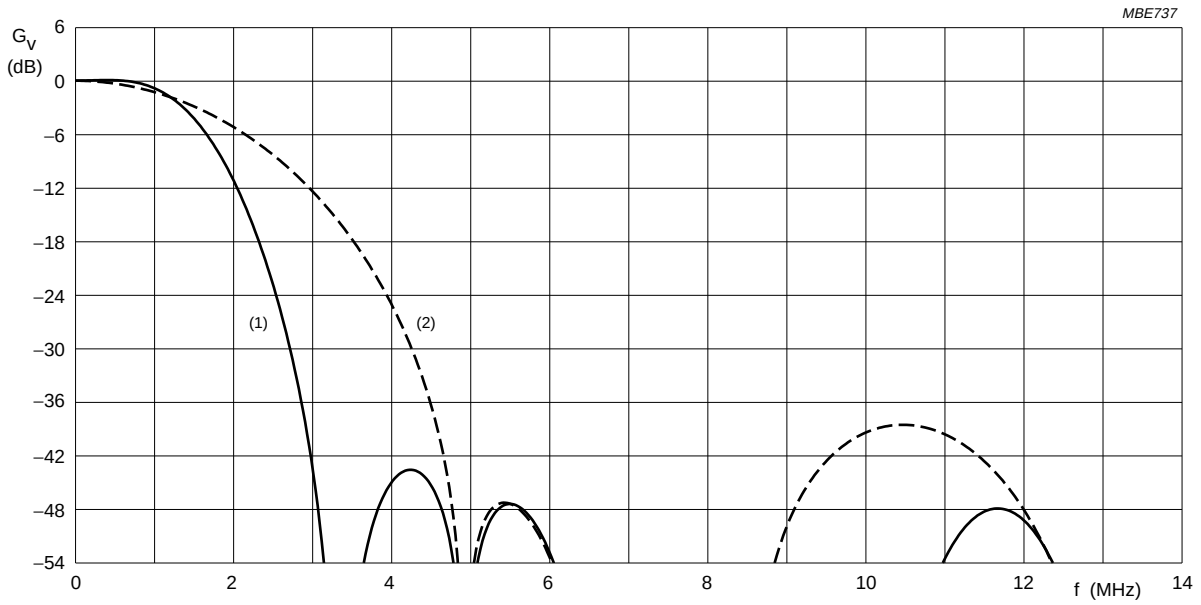
Slave Transmitter

Table 33 Slave Transmitter (slave address 89H or 8DH)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	–	VER2	VER1	VER0	CCRDO	CCRDE	FSQ2	FSQ1	FSQ0

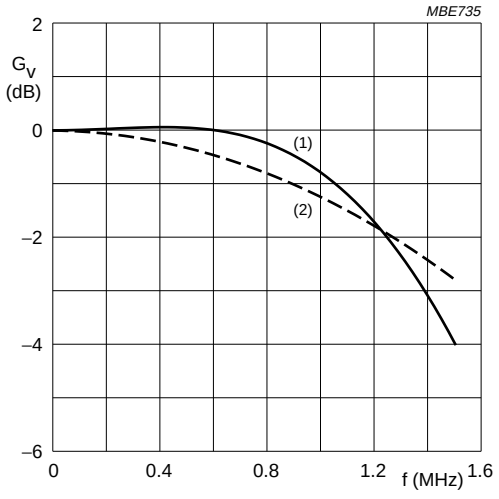
Table 34 No subaddress

DATA BYTE	DESCRIPTION
VER	Version identification of the device. It will be changed with all versions of the IC that have different programming models. Current version is 100 binary.
CCRDO	1 = closed caption bytes of the odd field have been encoded. 0 = the bit is reset after information has been written to the subaddresses 67 and 68. It is set immediately after the data have been encoded.
CCRDE	1 = closed caption bytes of the even field have been encoded. 0 = the bit is reset after information has been written to the subaddresses 69 and 6A. It is set immediately after the data have been encoded.
FSQ	State of the internal field sequence counter. Bit 0 (FSQ0) gives the odd/even information; odd = LOW, even = HIGH.



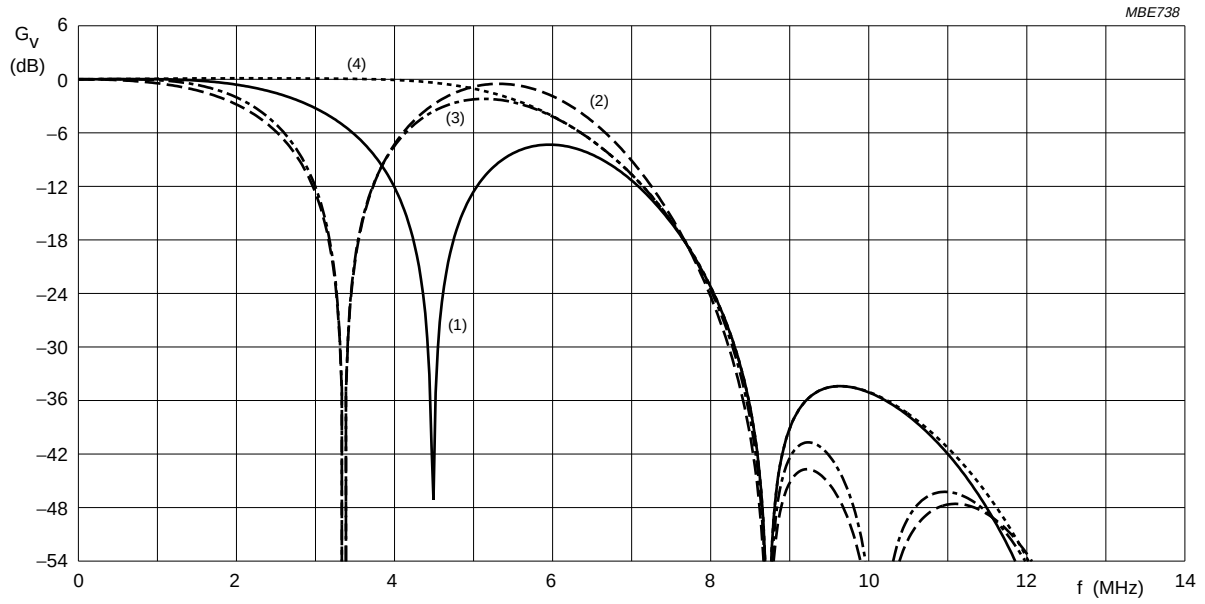
(1) SCBW = 1.
(2) SCBW = 0.

Fig.3 Chrominance transfer characteristic 1.



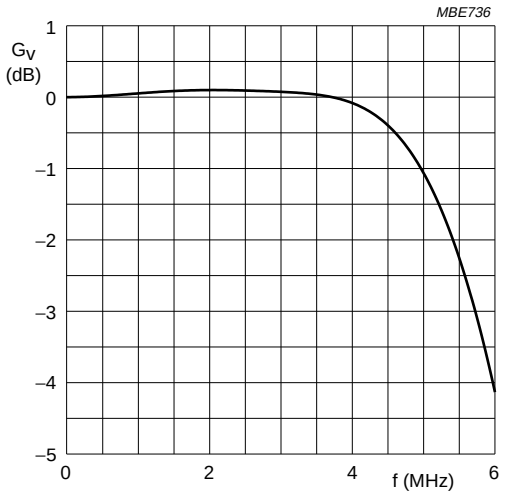
(1) SCBW = 1.
(2) SCBW = 0.

Fig.4 Chrominance transfer characteristic 2.



(1) CCRS1 = 0; CCRS0 = 1.
(2) CCRS1 = 1; CCRS0 = 0.
(3) CCRS1 = 1; CCRS0 = 1.
(4) CCRS1 = 0; CCRS0 = 0.

Fig.5 Luminance transfer characteristic 1.



CCRS1 = 0; CCRS0 = 0.

Fig.6 Luminance transfer characteristic 2.

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DDD}	digital supply voltage		4.5	5.5	V
V_{DDA}	analog supply voltage		4.75	5.25	V
I_{DDD}	digital supply current	note 1	–	170	mA
I_{DDA}	analog supply current	note 1	–	55	mA
Inputs					
V_{IL}	LOW level input voltage (except SDA, SCL, AP, SP and XTALI)		–0.5	+0.8	V
V_{IH}	HIGH level input voltage (except LLC, SDA, SCL, AP, SP and XTALI)		2.0	V_{DDD} + 0.5	V
	HIGH level input voltage (LLC)		2.4	V_{DDD} + 0.5	V
I_{LI}	input leakage current		–	1	µA
C_I	input capacitance	clocks operating	–	10	pF
		data available	–	8	pF
		I/Os at high impedance	–	8	pF
Outputs					
V_{OL}	LOW level output voltage (except SDA and XTALO)	note 2	0	0.6	V
V_{OH}	HIGH level output voltage (except LLC, SDA, $\overline{DTACK}$ and XTALO)	note 2	2.4	V_{DDD} + 0.5	V
	HIGH level output voltage (LLC)	note 2	2.6	V_{DDD} + 0.5	V
I^2C-bus; SDA and SCL					
V_{IL}	LOW level input voltage		–0.5	+1.5	V
V_{IH}	HIGH level input voltage		3.0	V_{DDD} + 0.5	V
I_I	input current	V_I = LOW or HIGH	–10	+10	µA
V_{OL}	LOW level output voltage (SDA)	I_{OL} = 3 mA	–	0.4	V
I_O	output current	during acknowledge	3	–	mA
Clock timing (LLC)					
T_{LLC}	cycle time	note 3	34	41	ns
δ	duty factor t_{HIGH}/T_{LLC}	note 4	40	60	%
t_r	rise time	note 3	–	5	ns
t_f	fall time	note 3	–	6	ns
Input timing					
t_{SU}	input data set-up time (any other except SEL_MPU, CDIR, $\overline{RW}$/SCL, A0/SDA, $\overline{CS}$/SA, $\overline{RES}$, AP and SP)		6	–	ns
t_{HD}	input data hold time (any other except SEL_MPU, CDIR, $\overline{RW}$/SCL, A0/SDA, $\overline{CS}$/SA, $\overline{RES}$, AP and SP)		3	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Crystal oscillator					
f_n	nominal frequency (usually 27 MHz)	3rd harmonic	–	30	MHz
$\Delta f/f_n$	permissible deviation of nominal frequency	note 5	–50	+50	10^{-6}
CRYSTAL SPECIFICATION					
T_{amb}	operating ambient temperature		0	70	°C
C_L	load capacitance		8	–	pF
R_S	series resistance		–	80	Ω
C_1	motional capacitance (typical)		1.5 –20%	1.5 +20%	fF
C_0	parallel capacitance (typical)		3.5 –20%	3.5 +20%	pF
MPU interface timing					
t_{AS}	address set-up time	note 6	9	–	ns
t_{AH}	address hold time		0	–	ns
$t_{R\overline{W}S}$	read/write set-up time	note 6	9	–	ns
$t_{R\overline{W}H}$	read/write hold time		0	–	ns
t_{DD}	data bus floating from $\overline{CS}$ (read)	notes 7, 8 and 9	75	142	ns
t_{DF}	data valid from $\overline{CS}$ (read)	notes 7 and 8	38	105	ns
t_{DS}	data bus set-up time (write)	note 6	9	–	ns
t_{DH}	data bus hold time (write)	note 6	9	–	ns
t_{ACS}	acknowledge delay from $\overline{CS}$	notes 7 and 8	112	180	ns
$t_{\overline{CS}D}$	$\overline{CS}$ HIGH from acknowledge		0	–	ns
t_{DAT}	$\overline{DTACK}$ floating from $\overline{CS}$ HIGH	notes 7 and 8; n = 7	75	142	ns
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_{OH}	output hold time		4	–	ns
t_{OD}	output delay time	CREF in output mode	–	25	ns
Chroma, Y and CVBS outputs					
$V_{o(p-p)}$	output signal voltage (peak-to-peak value)	note 10	1.9	2.1	V
R_I	internal series resistance		18	35	Ω
R_L	output load resistance		80	–	Ω
B	output signal bandwidth of DACs	–3 dB	10	–	MHz
ILE	LF integral linearity error of DACs		–	±2	LSB
DLE	LF differential linearity error of DACs		–	±1	LSB

Notes to the Characteristics

1. At maximum supply voltage with highly active input signals.
2. The levels have to be measured with load circuits of 1.2 kΩ to 3.0 V (standard TTL load) and C_L = 25 pF.
3. The data is for both input and output direction.
4. With LLC in input mode. In output mode, with a crystal connected to XTALO/XTALI duty factor is typically 50%.
5. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.
6. The value is calculated via equation $t = t_{SU} + t_{HD}$
7. The value depends on the clock frequency. The numbers given are calculated with f_{LLC} = 27 MHz.
8. The values given are calculated via equation $t_{dmax} = t_{OD} + n \times t_{LLC} + t_{LLC} + t_{SU}$ and

   $t_{dmin} = t_{OH} + n \times t_{LLC} + t_{LLC} - t_{HD}$
9. The falling edge of $\overline{DTACK}$ will always occur 1 × LLC after data is valid.
10. For full digital range, without load, V_{DDA} = 5.0 V. The typical voltage swing is 2.0 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

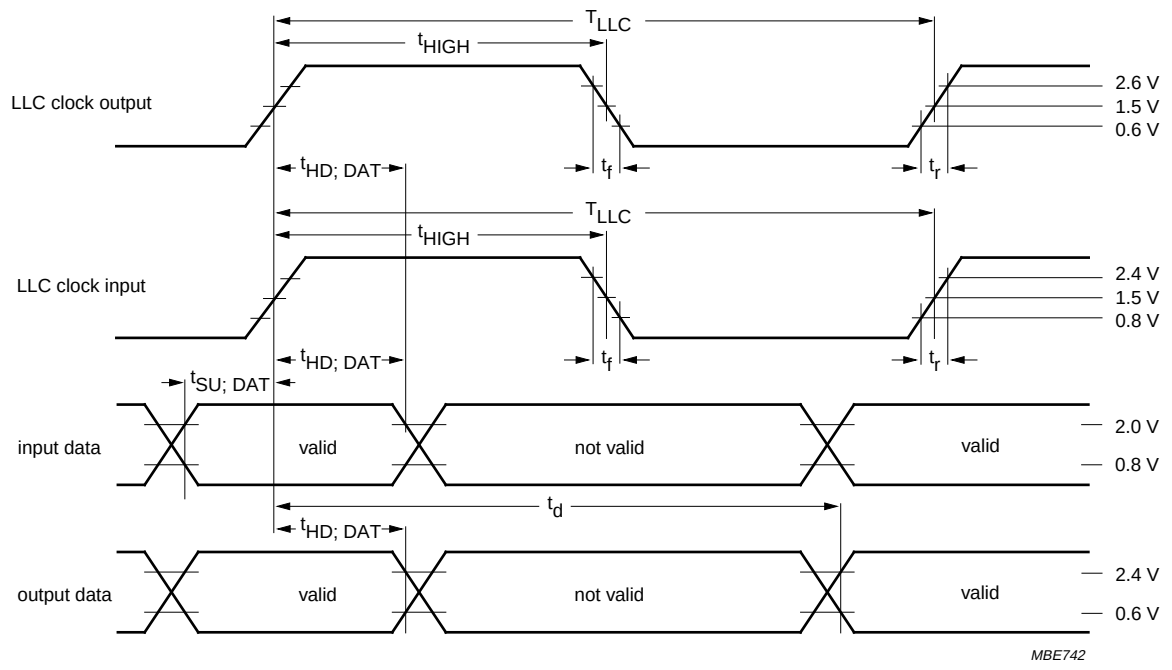
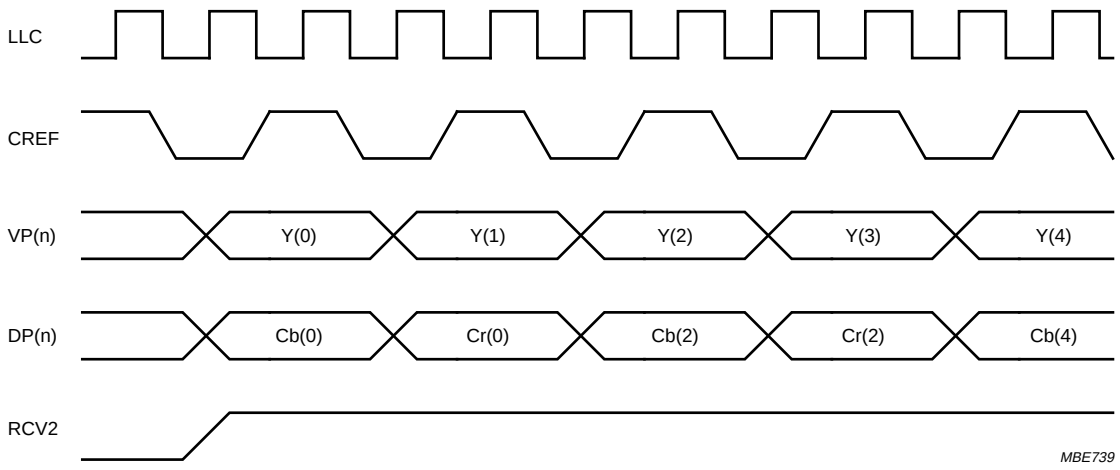
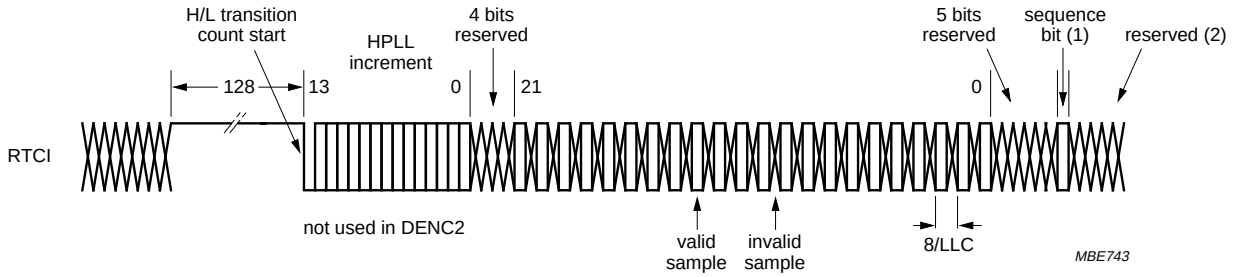


Fig.7 Clock data timing.



The data demultiplexing phase is coupled to the internal horizontal phase.
The CREF signal applies only for the 16 lines digital TV format, because these signals are only valid in 13.5 MHz.
The phase of the RCV2 signal is programmed to tbf (tbf for 50 Hz) in this example in output mode (BRCV2).

Fig.8 Digital TV timing.



(1) Sequence bit:
PAL = logic 0 then (R – Y) line normal; PAL = logic 1 then (R – Y) line inverted.
NTSC = logic 0 then no change.
(2) Reserved bits: 235 with 50 Hz systems; 232 with 60 Hz systems.
(3) Only from SAA7111 decoder.
(4) SAA7111 provides (22:0) bits, resulting in 3 reserved bits before sequence bit.

Fig.9 RTCI timing.

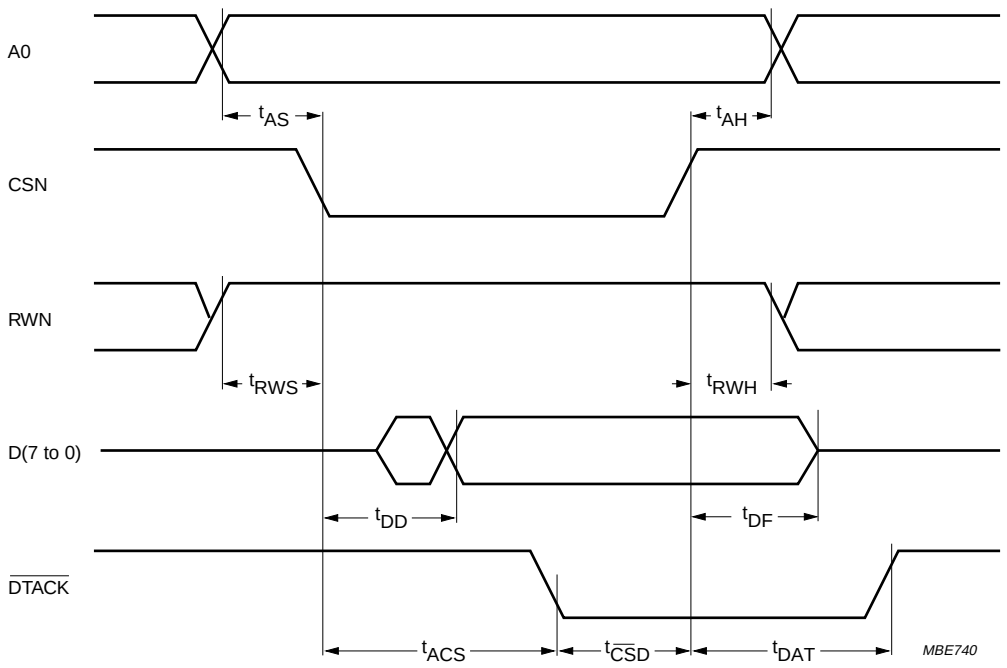


Fig.10 MPU interface timing (READ cycle).

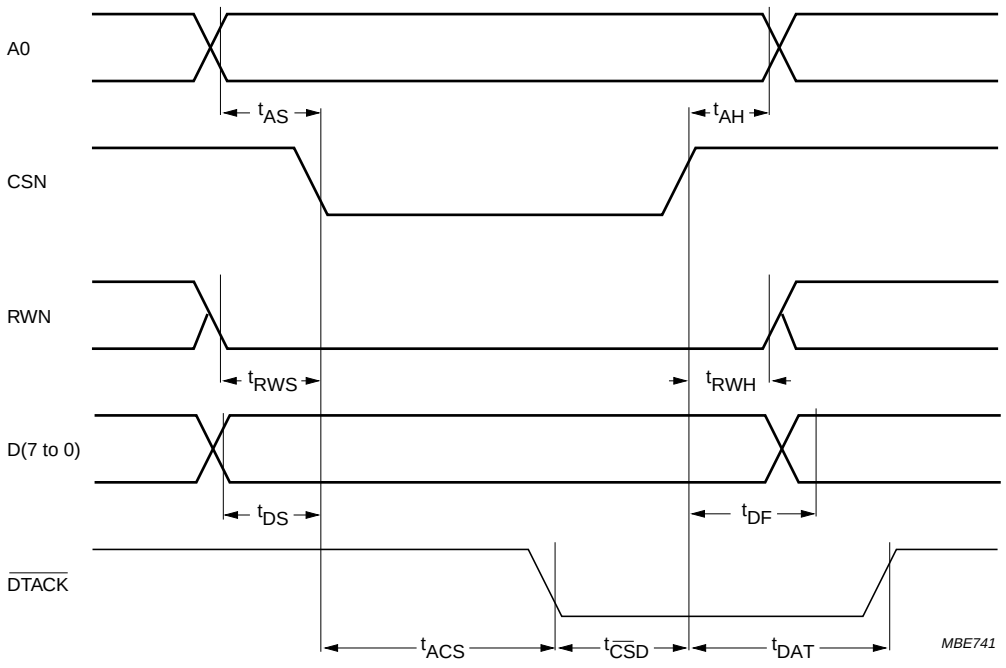


Fig.11 MPU interface timing (WRITE cycle).

APPLICATION INFORMATION

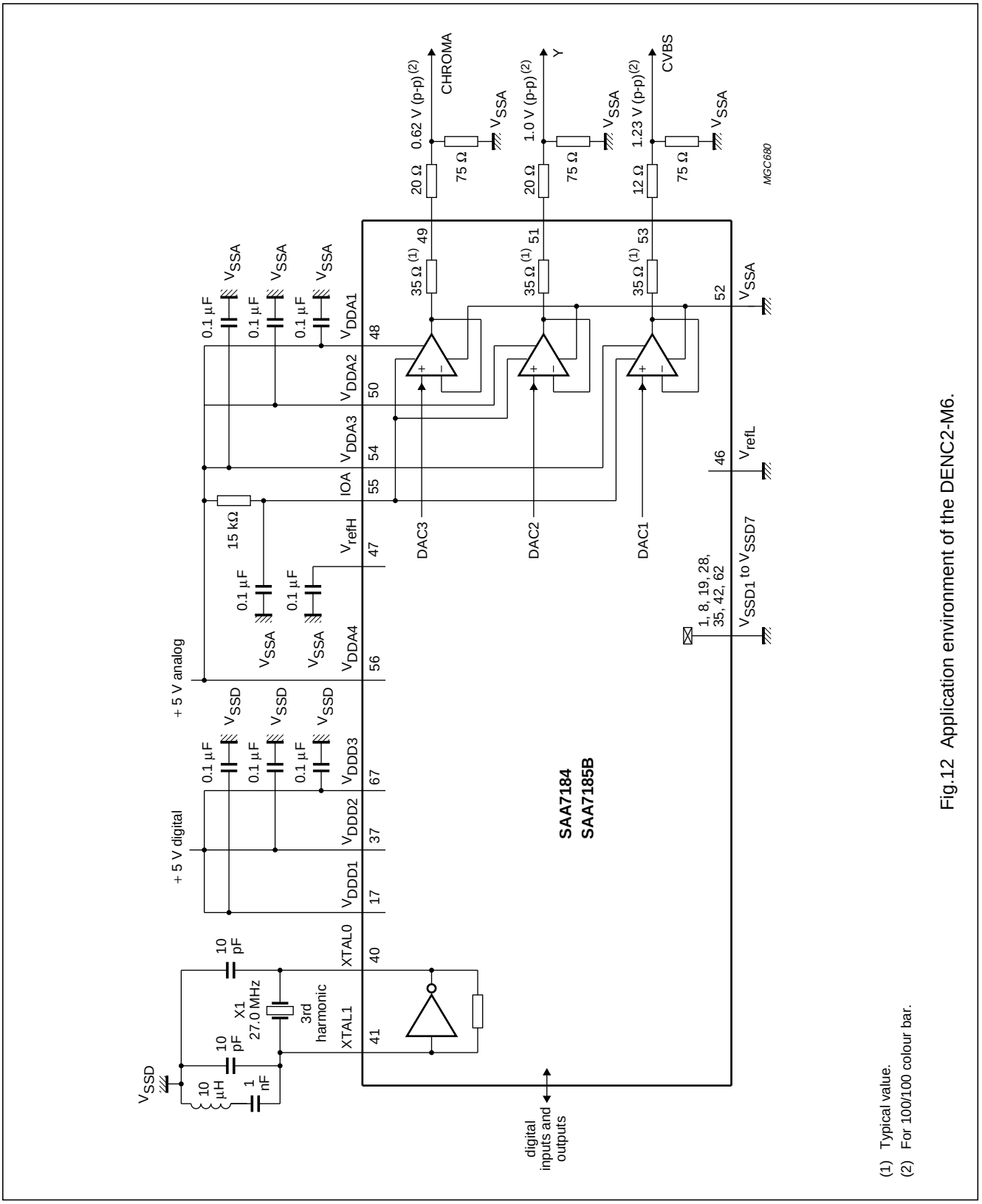
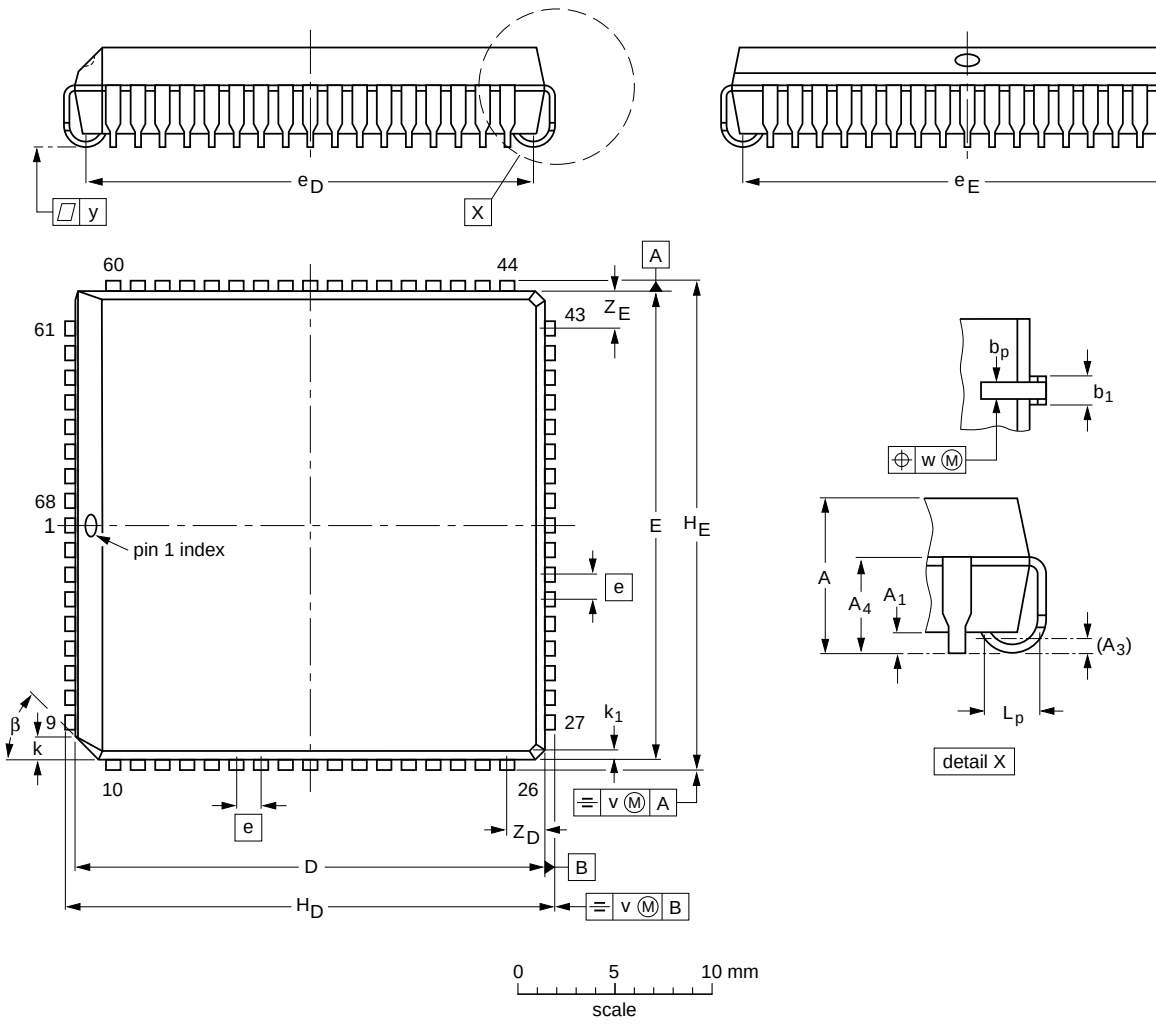


Fig.12 Application environment of the DENC2-M6.

(1) Typical value.
(2) For 100/100 colour bar.

PACKAGE OUTLINE

PLCC68: plastic leaded chip carrier; 68 leads **SOT188-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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