

DATA SHEET

SAA4995WP **PANorama-IC (PAN-IC)**

Preliminary specification
File under Integrated Circuits, IC02

1997 Jun 10

PANorama-IC (PAN-IC)

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FEATURES

- Horizontal sample rate conversion in both zoom and compress direction, with a sample rate conversion factor between 0.5 and 2 (in 384 steps)
- Dynamic sample rate conversion for panorama mode display e.g. 4 : 3 material on a 16 : 9 display
- Dynamic sample rate conversion for amaronap mode display of e.g. 16 : 9 material on a 4 : 3 display
- Operates with 1f_h and 2f_h
- Programmable via microcontroller SNERT (Synchronous No parity Eight bit Receive Transmit) bus.

GENERAL DESCRIPTION

The PAN-IC is an add-on IC to be used, for example, between analog-to-digital conversion and a serial (field) memory. The device performs the following tasks:

- Linear horizontal sample rate conversion in both zoom and compress direction, with a sample rate conversion factor between 0.5 and 2
- Dynamic sample rate conversion for panorama mode display of e.g. 4 : 3 material on a 16 : 9 display
- Dynamic sample rate conversion for amaronap mode display of e.g. 16 : 9 material on a 4 : 3 display.

The PAN-IC has the ability to increase the data rate from the ADC to a maximum of twice the data rate at the output. To achieve this a clock rate at twice the normal output clock rate is needed to write data to the memory. All actions to generate a lower data rate, produces disable cycles in Write Enable (WE).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	supply voltage	4.5	5	5.5	V
I _{DD}	supply current	–	110	–	mA
f _{CLK}	operating clock frequency	–	–	33	MHz
T _{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4995WP	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

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BLOCK DIAGRAM

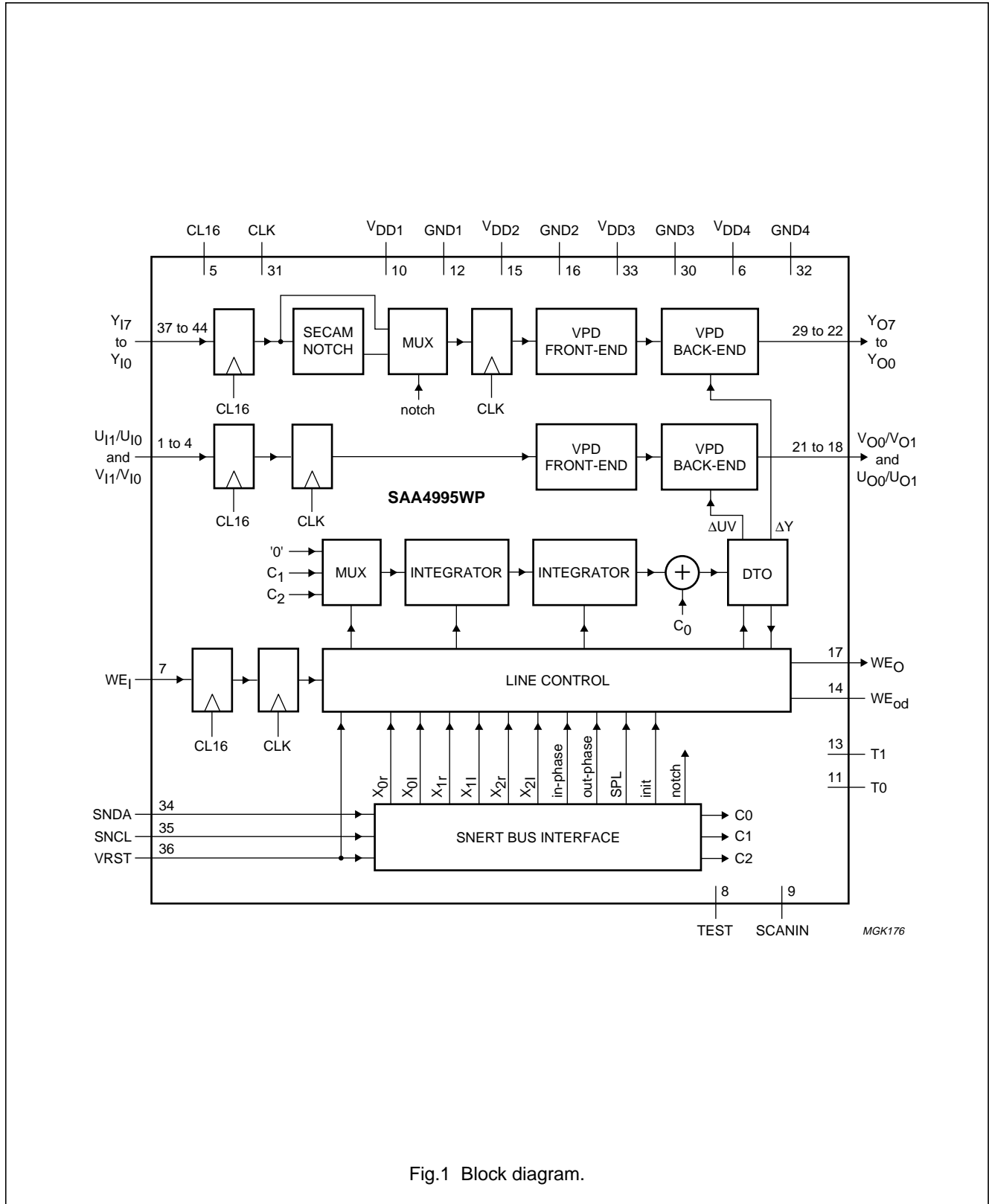


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
U _{I1}	1	U input bit 1
U _{I0}	2	U input bit 0
V _{I1}	3	V input bit 1
V _{I0}	4	V input bit 0
CL16	5	half system clock
V _{DD4}	6	supply voltage 4
WE _I	7	write enable input
TEST	8	test mode switch
SCANIN	9	input for scan chain
V _{DD1}	10	supply voltage 1
T0	11	test mode switch 0
GND1	12	ground 1
T1	13	test mode switch 1
WE _{od}	14	write enable odd samples
V _{DD2}	15	supply voltage 2
GND2	16	ground 2
WE _O	17	write enable output
V _{O0}	18	V output bit 0
V _{O1}	19	V output bit 1
U _{O0}	20	U output bit 0
U _{O1}	21	U output bit 1
Y _{O0}	22	luminance output bit 0
Y _{O1}	23	luminance output bit 1

SYMBOL	PIN	DESCRIPTION
Y _{O2}	24	luminance output bit 2
Y _{O3}	25	luminance output bit 3
Y _{O4}	26	luminance output bit 4
Y _{O5}	27	luminance output bit 5
Y _{O6}	28	luminance output bit 6
Y _{O7}	29	luminance output bit 7
GND3	30	ground 3
CLK	31	system clock
GND4	32	ground 4
V _{DD3}	33	supply voltage 3
SNDA	34	data input from interface SNERT bus
SNCL	35	clock input from interface SNERT bus
VRST	36	reset input in the vertical blanking interval
Y _{I7}	37	luminance input bit 7
Y _{I6}	38	luminance input bit 6
Y _{I5}	39	luminance input bit 5
Y _{I4}	40	luminance input bit 4
Y _{I3}	41	luminance input bit 3
Y _{I2}	42	luminance input bit 2
Y _{I1}	43	luminance input bit 1
Y _{I0}	44	luminance input bit 0

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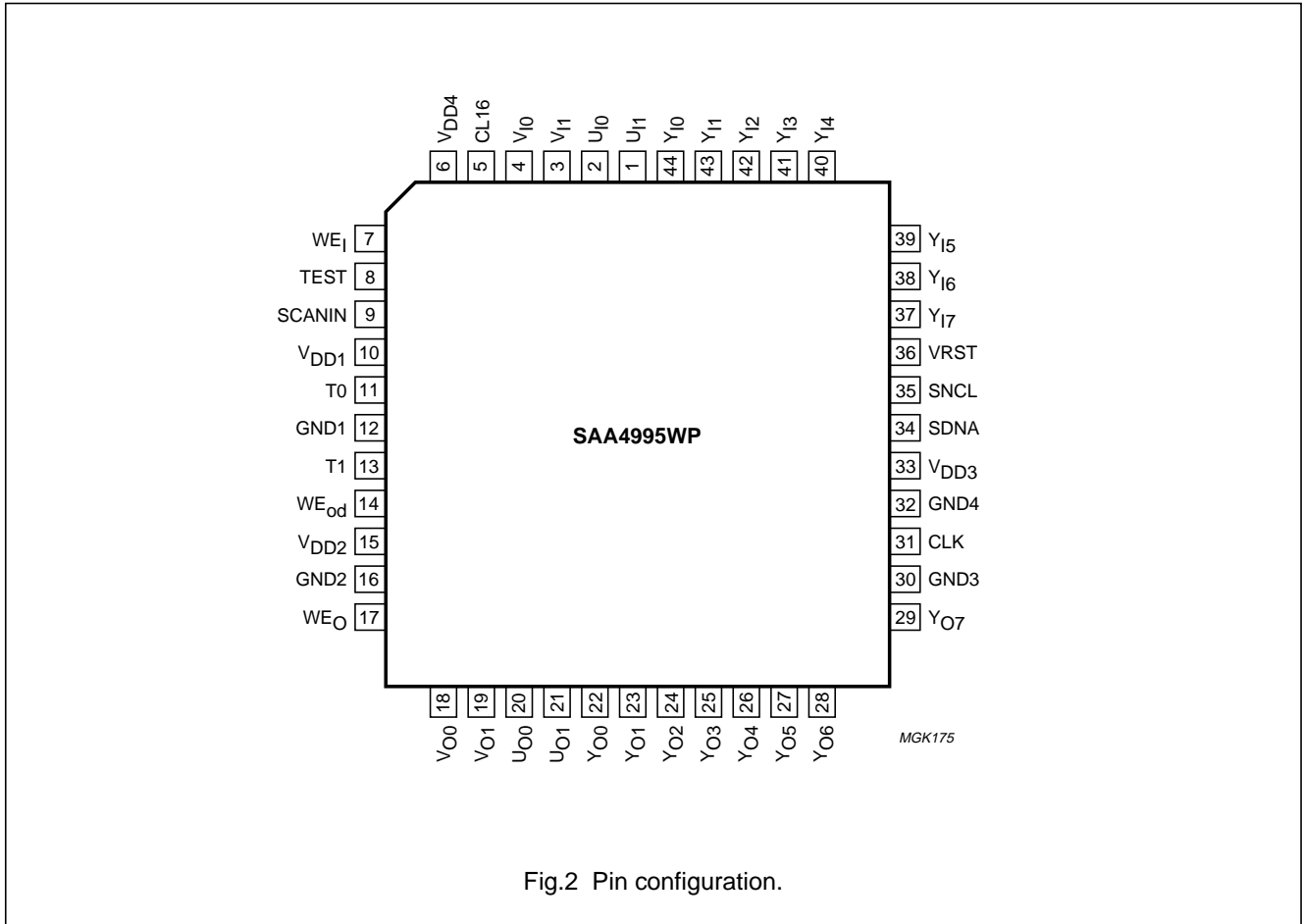


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The PAN-IC is an add-on IC to be used, for example, between analog-to-digital conversion and a serial (field) memory. The device performs the following tasks:

- Linear horizontal sample rate conversion in both zoom and compress direction, with a sample rate conversion factor between 0.5 and 2
- Dynamic sample rate conversion for panorama mode display of e.g. 4 : 3 material on a 16 : 9 display
- Dynamic sample rate conversion for amaronap mode display of e.g. 16 : 9 material on a 4 : 3 display.

The PAN-IC has the ability to increase the data rate from the ADC (maximum 16 MHz in a 16/32 MHz concept) to a maximum of twice the data rate. For this, a 32 MHz clock rate is needed to write to the memory. All actions to generate a lower data rate produces disable cycles in write enable.

In panorama and amaronap modes, the sample rate conversion factor is modulated along the video line.

In the centre of the line a high quality compression (e.g. with a factor $\frac{4}{3}$) has to be made. Towards the sides of the line, more and more expansion and compression respectively is made. The sample rate conversion factor over a line will have a bathtub shape, with parameters illustrated in Fig.3:

- X_{0l} and X_{0r} , where in-between a constant data rate is maintained (area I) and starting points from where a curve can be programmed for its 2nd derivative (in areas II and V)
- X_{1l} and X_{1r} , points from where a new curve can be programmed for its 2nd derivative (for areas III and IV)
- X_{2l} corresponds to the first sample in the output data stream, defined by start of WE_l
- X_{2r} corresponds to the last sample in the output data stream, defined by the programmed number of samples
- C_1 , which controls the second derivatives of the data rate in areas II and V
- C_2 , which controls the second derivatives of the data rate in areas III and IV.

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Interpolation function

The interpolation for phase positions between the original samples, is achieved with a variable phase delay filter with 10 taps for luminance signals and 4 taps for chrominance signals. For luminance the PAN-IC supplies samples up to 32 MHz. For chrominance the PAN-IC supplies each U and V samples with a data rate of 8 MHz (max).

Processing control in the PAN-IC

The compress factor (see Fig.4) at any position in the lines is a function of the dynamically changing DTO-increment. When $DTO_{incr} = 255$, the sample rate is divided by 2; when $DTO_{incr} = 0$, the sample rate in the PAN-IC remains unchanged; when $DTO_{incr} = -128$, the sample rate is doubled.

Control of number of samples per line

Three possibilities exist for the relationship between the end of WE_1 and the required number of samples per line for storage in the field memory:

- WE_1 negative edge coincides with the required last sample in the line; standard operation.
- WE_1 negative edge is reached before the present last sample in the line was required; extra dummy WE cycles will be generated at the maximum rate (zoom factor 2) to arrive at the required number of samples per line.
- The required number of samples per line is reached before WE_1 negative edge; the DTO calculations will continue until the required number of samples is reached, but without generation of WE cycles.

The programmed number of samples per line is thus always realized, independent of all other controls (unless the line period becomes insufficient to store up to the last sample in a line). When using odd/even sample distribution, the programmed number of samples refers to the number of samples in each data stream. Consequently, the total number of samples is twice as many.

There is an offset in the programmed number of samples compared to the effective number of samples per line.

- Effective number of Y samples = $4 \times (\text{programmed number of samples} + 1)$
- Effective number of UV samples = $1 \times (\text{programmed number of samples} + 1)$

SECAM Y notch

A notch filter at the Y input of the PAN-IC can be switched on. The purpose of this filter is to prevent artefacts from scan velocity modulation with SECAM inputs. The notch filter is an FIR filter with coefficients $(-1 \ 0 \ 3 \ 0 \ 3 \ 0 \ -1)$. When $f_s = 16$ MHz, the notch frequency is 4 MHz; the maximum gain of the filter is +3 dB at 2 and 6 MHz.

Timing

The inputs are related to CL16 (half system clock). This clock is used for reference in the PAN-IC from the CL16 pin. The system clock must have a fixed phase relationship to the CL16 enable signal (one clock system).

Relationship of WE to video data

WE inputs and outputs may be used with either coincident or advanced WE to video timing (see Fig.5). The advanced WE to video timing is applicable to field memories, such as the SAA4955TJ. The input and output WEs of the PAN-IC can be programmed separately to either timing by the in-phase and out-phase bits.

Odd/even sample distribution

The PAN-IC usually delivers a complete YUV data stream to one receiving device, e.g. a field memory. Optionally, a data stream can be split into odd and even samples, to be received by two receiving devices.

The relationship between Y and UV samples is then non-trivial (see Tables 1 to 4).

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NO SPLITTING INTO ODD AND EVEN SAMPLE STREAM

Table 1 Normal output YUV data stream

E	O	E	O	E	O	E	O	E	O	E	O	E
Y ⁰	Y ¹	Y ²	Y ³	Y ⁴	Y ⁵	Y ⁶	Y ⁷	Y ⁸	Y ⁹	Y ¹⁰	Y ¹¹	Y ¹²
UV ₇₆ ⁰	UV ₅₄ ⁰	UV ₃₂ ⁰	UV ₁₀ ⁰	UV ₇₆ ⁴	UV ₅₄ ⁴	UV ₃₂ ⁴	UV ₁₀ ⁴	UV ₇₆ ⁸	UV ₅₄ ⁸	UV ₃₂ ⁸	UV ₁₀ ⁸	UV ₇₆ ¹²

SPLITTING INTO ODD AND EVEN SAMPLE STREAM

Keeps corresponding parts of the UV samples in one stream (UV⁰, UV⁸, etc. in even stream and UV⁴, UV¹², etc. in odd stream): The odd data stream misses two samples at the start of a line and has two dummy samples at the end of the line, to keep the UV format correct and maintain the same line length as for the even stream (In the odd stream, the last two Y samples and the last U and V samples of a line are not valid).

Table 2 Even YUV data stream

E	–	E	–	E	–	E	–	E	–	E	–	E
Y ⁰	–	Y ²	–	Y ⁴	–	Y ⁶	–	Y ⁸	–	Y ¹⁰	–	Y ¹²
UV ₇₆ ⁰	–	UV ₅₄ ⁰	–	UV ₃₂ ⁰	–	UV ₁₀ ⁰	–	UV ₇₆ ⁸	–	UV ₅₄ ⁸	–	UV ₃₂ ¹²

Table 3 Odd YUV data stream

–	–	–	–	–	O	–	O	–	O	–	O	–
–	–	–	–	–	Y ⁵	–	Y ⁷	–	Y ⁹	–	Y ¹¹	–
–	–	–	–	–	UV ₇₆ ⁴	–	UV ₅₄ ⁴	–	UV ₃₂ ⁴	–	UV ₁₀ ⁴	–

The even and odd data streams given in Tables 2 and 3 can be distributed to two receiving devices with input enable facilities. A separate input signal for each of the receiving devices must then be applied while the even YUV data stream and odd YUV data stream are again combined.

COMBINED ODD/EVEN OUTPUT YUV DATA STREAM

Table 4 Distribution with odd/even input enable signals

E	–	E	–	E	–	E	O	E	O	E	O	E
Y ⁰	–	Y ²	–	Y ⁴	Y ⁵	Y ⁶	Y ⁷	Y ⁸	Y ⁹	Y ¹⁰	Y ¹¹	Y ¹²
UV ₇₆ ⁰	–	UV ₅₄ ⁰	–	UV ₃₂ ⁰	UV ₇₆ ⁴	UV ₁₀ ⁰	UV ₅₄ ⁴	UV ₇₅ ⁸	UV ₃₂ ⁴	UV ₅₄ ⁸	UV ₁₀ ⁴	UV ₃₂ ⁸

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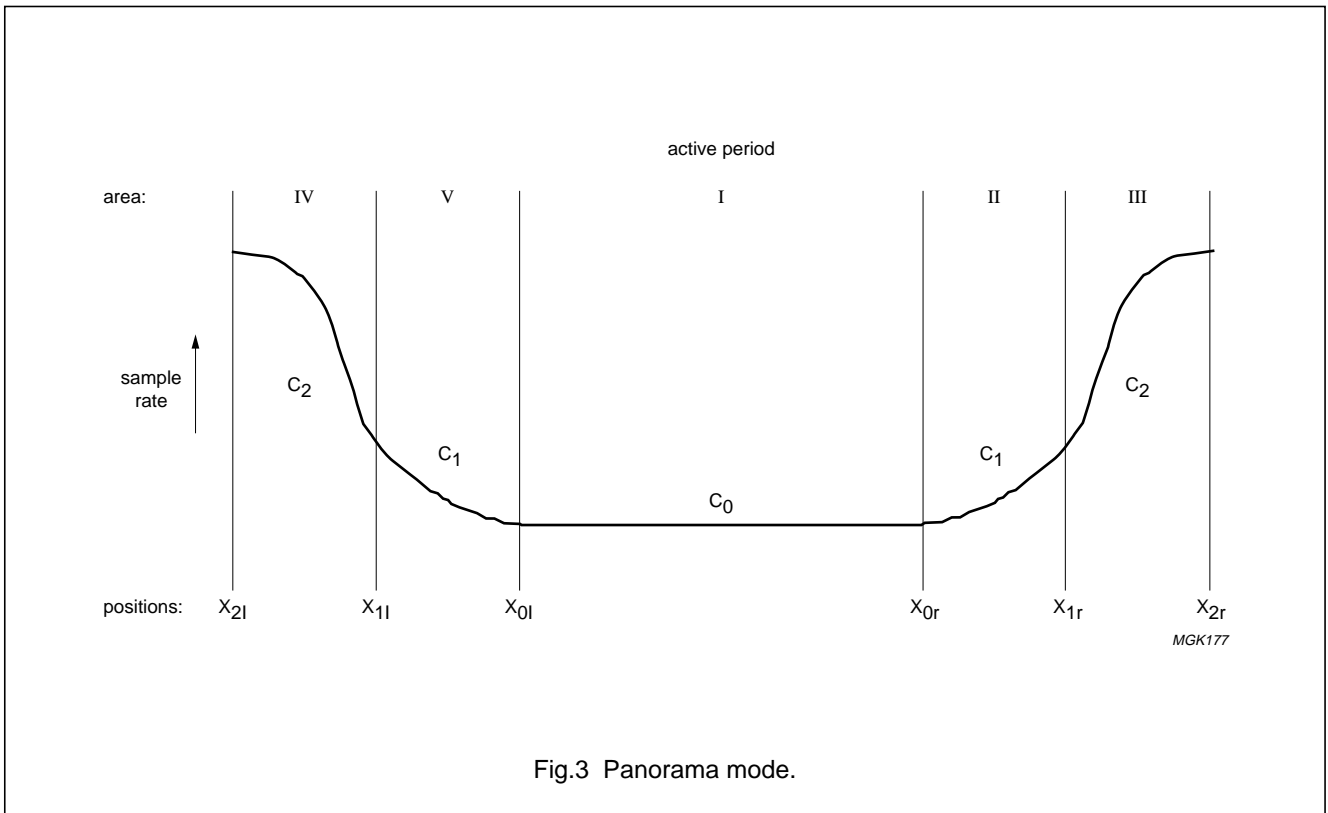


Fig.3 Panorama mode.

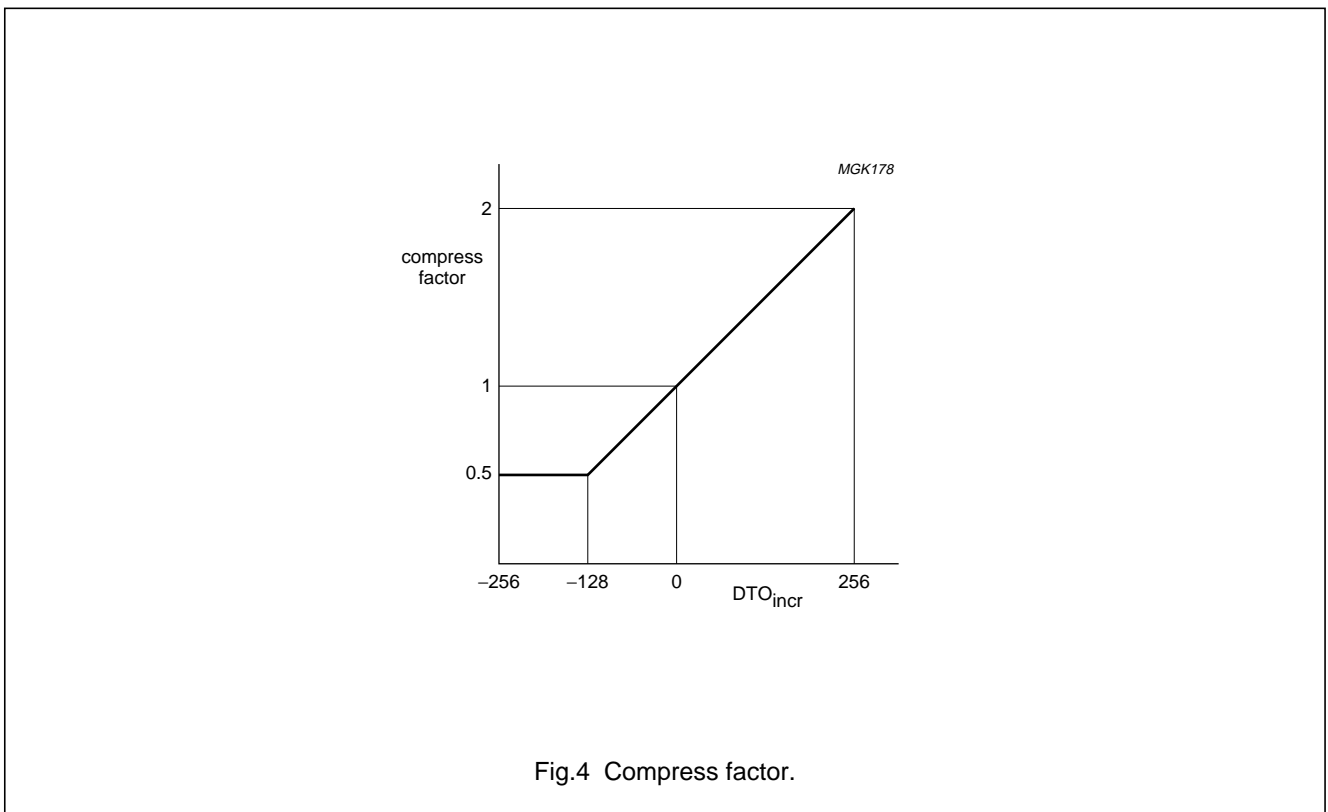


Fig.4 Compress factor.

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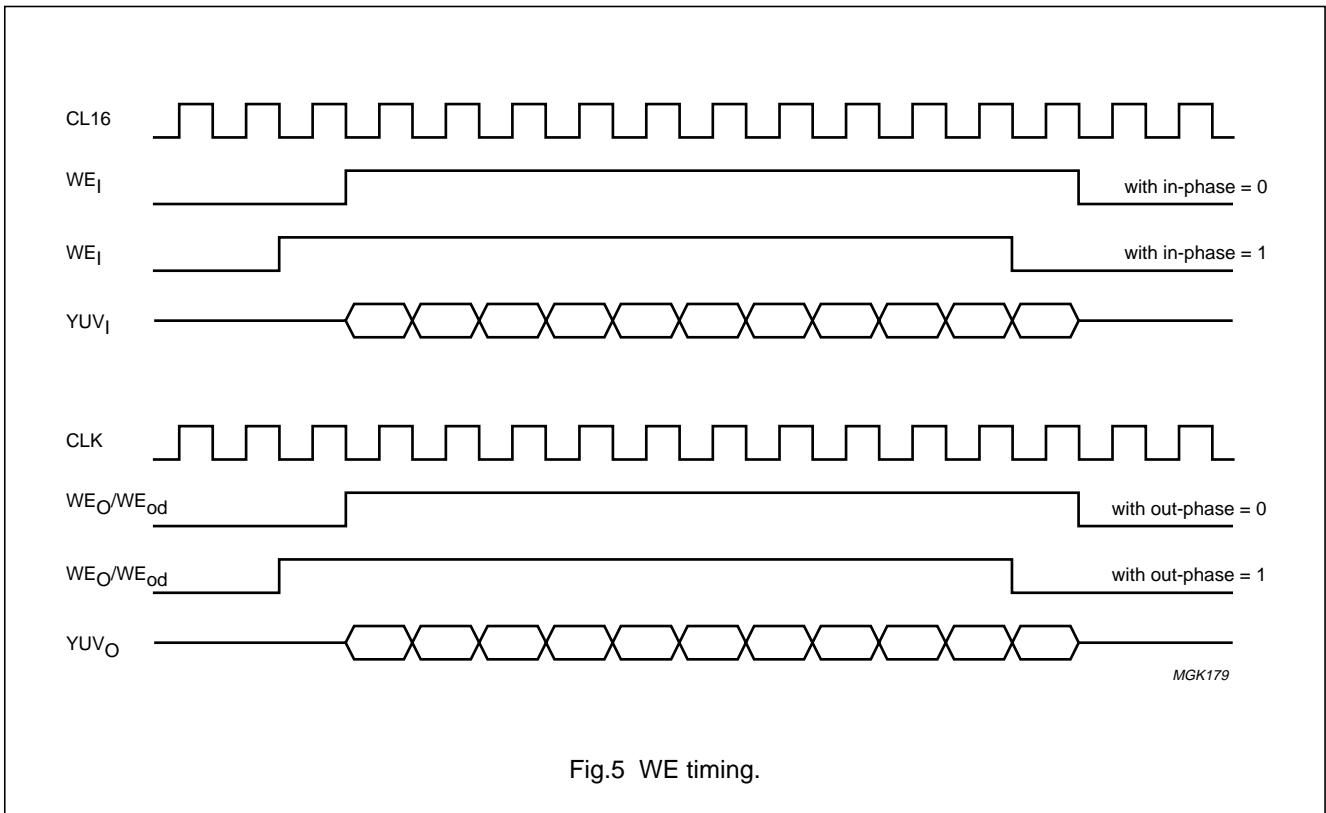


Fig.5 WE timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DD}	supply voltage		-0.5	+6.5	V
V _i , V _o	input and output voltages		-0.5	V _{DD} + 0.5	V
I _{o/out}	output current per output pin		-	20	mA
P/out	power dissipation per output pin		-	100	mW
T _{stg}	storage temperature		-55	+140	°C
T _{amb}	operating ambient temperature		-40	+85	°C
V _{ESD}	electrostatic handling for all pins	note 1	-	±2000	V
		note 2	-	±300	V

Notes

- Human body model: C = 100 pF, R = 1.5 kΩ, V = 2 kV.
- Machine model: C = 200 pF, R = 0 Ω, V = 300 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient in free air	50	K/W

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CHARACTERISTICS

$V_{DD} = 5.0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	5	5.5	V
I_{DD}	supply current		–	110	–	mA
f_{CLK}	operating frequency (CLK)		–	–	33	MHz
f_{CL16}	operating frequency (CL16)		–	$\frac{1}{2}f_{CLK}$	–	MHz
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
C_i	input capacitance		–	10	15	pF
V_{OL}	LOW level output voltage	$I_o = 4\text{ mA}$	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_o = -4\text{ mA}$	2.6	3.4	–	V
$t_{su(i)(D)}$	input set-up time with respect to CL16 rising edge	except pins SNDA, SNCL, VRST and CLK; see Fig.6	8	–	–	ns
$t_{h(i)(CL16)}$	input hold time with respect to CL16 rising edge	except pins SNDA, SNCL, VRST and CLK; see Fig.6	0	–	–	ns
$t_{su(i)(CL16)}$	input set-up time with respect to CLK rising edge	see Fig.6	7	–	–	ns
$t_{h(i)(CL16)}$	input hold time with respect to CLK rising edge	see Fig.6	3	–	–	ns
$t_{h(o)}$	output hold time with respect to CLK	$C_L = 7\text{ pF}$	5	–	–	ns
t_d	output delay time with respect to CLK	$C_L = 15\text{ pF}$	–	–	19	ns
T_{amb}	operating ambient temperature		0	–	70	$^{\circ}\text{C}$
T_j	junction temperature		–	–	125	$^{\circ}\text{C}$

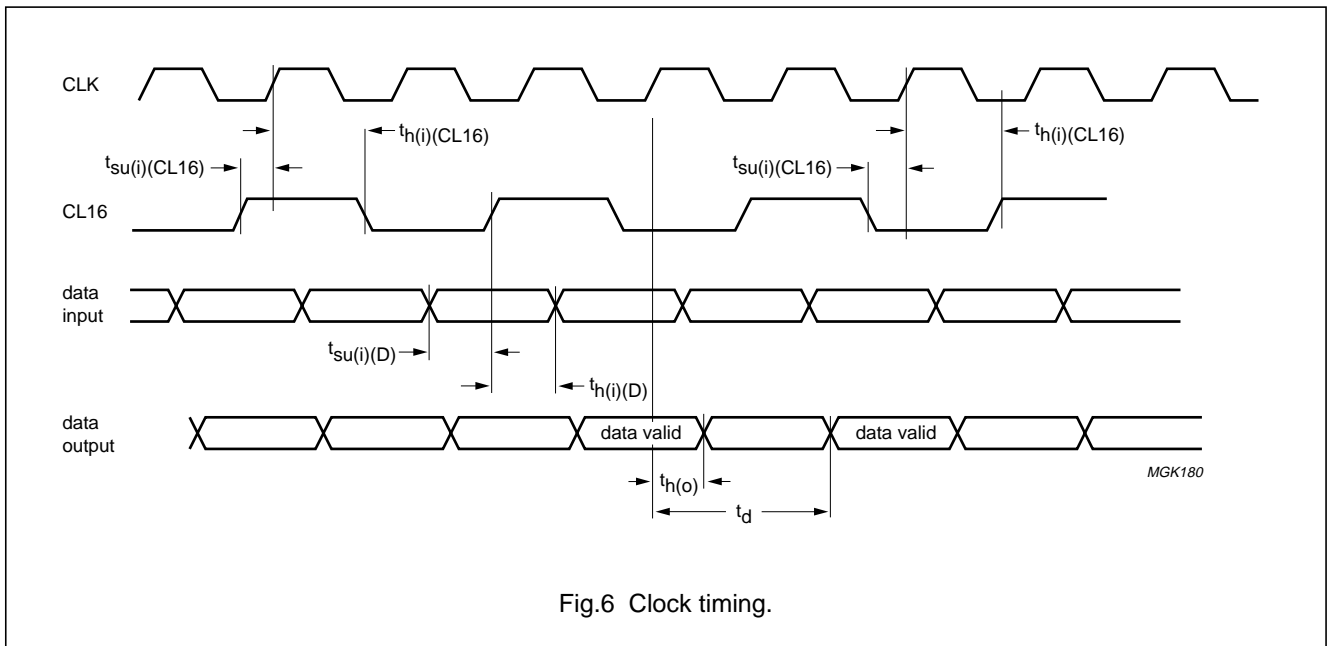


Fig.6 Clock timing.

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MICROCONTROLLER BUS TIMING (SNERT BUS)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$T_{cy(SNCL)}$	SNCL cycle time	see Fig.7	1	–	μs
$t_{su(i)}$	input data set-up time	see Fig.7	90	–	ns
$t_{h(i)}$	input data hold time	see Fig.7	50	–	ns
$t_{h(o)(D)}$	output data hold time	see Fig.7	0	–	ns
t_d	output data delay time	see Fig.7	–	700	ns

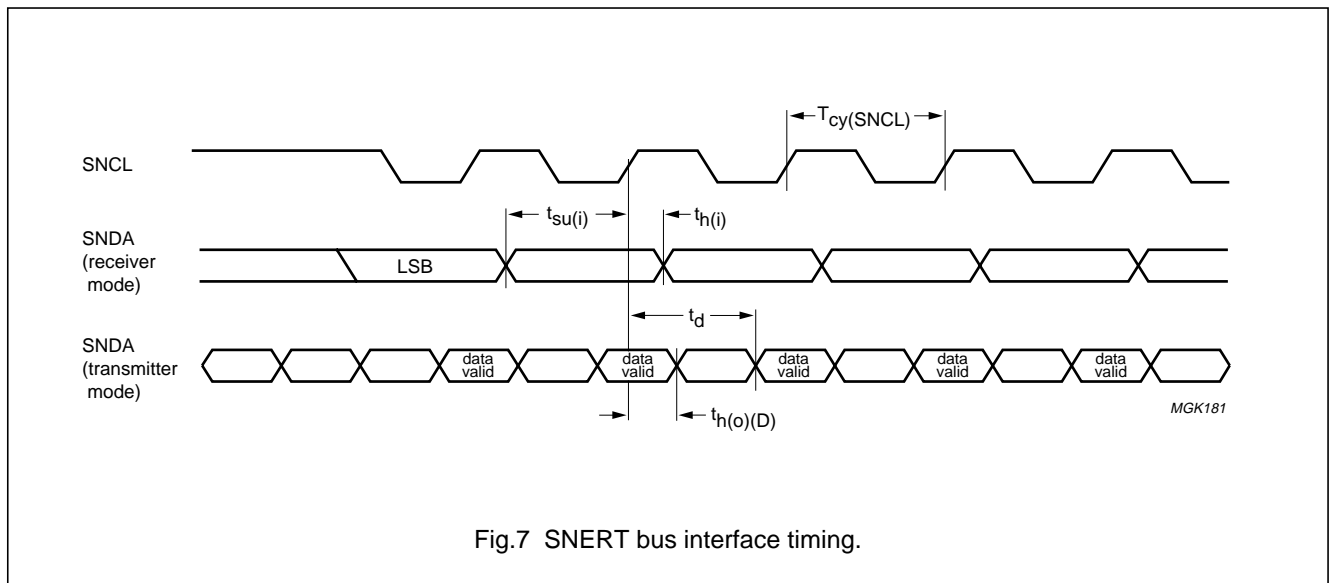


Fig.7 SNERT bus interface timing.

MICROCONTROLLER BUS CONTROL (SNERT BUS)

The following control table applies (Table 5), for control via the microcontroller bus (SNERT bus, consisting of SNCL, SNDA and VRST signals). Data communication is by writing to the PAN-IC (address 40H to 48H) and reading from it (address 49H)

Table 5 SNERT-bus control

ADDRESS (HEX)	FUNCTION	# OF BITS	BIT POSITION	REMARKS
40	X_{11}	8	7 : 0	definition of X_{11} with a resolution of 4 samples; see Fig.3 and note 1
41	X_{0l}	8	7 : 0	definition of X_{0l} with a resolution of 4 samples; see Fig.3 and note 1
42	X_{0r}	8	7 : 0	definition of X_{0r} with a resolution of 4 samples; see Fig.3 and note 1
43	X_{1r}	8	7 : 0	definition of X_{1r} with a resolution of 4 samples; see Fig.3 and note 1
44	output samples per line	8	7 : 0	resolution of 4 luminance samples; actual # samples = (programmed # samples + 1) \times 4; note 2

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ADDRESS (HEX)	FUNCTION	# OF BITS	BIT POSITION	REMARKS
45	C ₀	8	7 : 0	constant DTO _{incr} value for area I, MSB extended by zoom bit at address 48 (twos complement value); see Figs 3 and 4
46	C ₁	6	5 : 0	2nd derivatives for DTO _{incr} for areas II and V (twos complement value); see Figs 3 and 4
	distribution	1	6	enables odd/even sample distribution; see Tables 1 to 4
47	C ₂	6	5 : 0	2nd derivatives for DTO _{incr} for areas III and IV (twos complement value)
	test 1	1	6	test bit, must be logic 0 in normal operation
	notch	1	7	SECAM Y notch on/off (logic 1 = on, logic 0 = off)
48	zoom bit	1	0	logic 1 = zoom, logic 0 = compress in area I
	in-phase	1	1	logic 1 = shifted relation WE _{IN} to input data; see Fig.5
	out-phase	1	2	logic 1 = shifted relation WE _O /WE _{od} to output data; see Fig.5
	init	1	3	circuitry is initialized at VRST pulse
	vrst_xfer	1	4	new settings are activated at VRST pulse
	keep	1	5	compression curve is kept from last active line in field
	test 2	1	6	test bit, must be logic 0 in normal operation
adapt	1	7	adapt bit, must be logic 0 in normal operation	
49	identify read	8 read bits	7 : 0	PAN-IC identifies by pulling all bits LOW (hardware cluck)

Notes

- For a symmetrical bathtub curve $X_{nl} + X_{nr} = \text{output samples per line} + 1$.
- WE_I falling edge delay to the WE_O latest sample should not be equal to the pipeline delay. This can be controlled with the WE_I length via the microcontroller.

TEST

The test mode can be chosen via pins TEST, T0 and T1.

Table 6 Test modes

MODE	PIN NAME		
	TEST	T1	T0
Functional test	0	X ⁽¹⁾	X ⁽¹⁾
Test mode on	1	X ⁽¹⁾	X ⁽¹⁾

Note

- X = don't care.

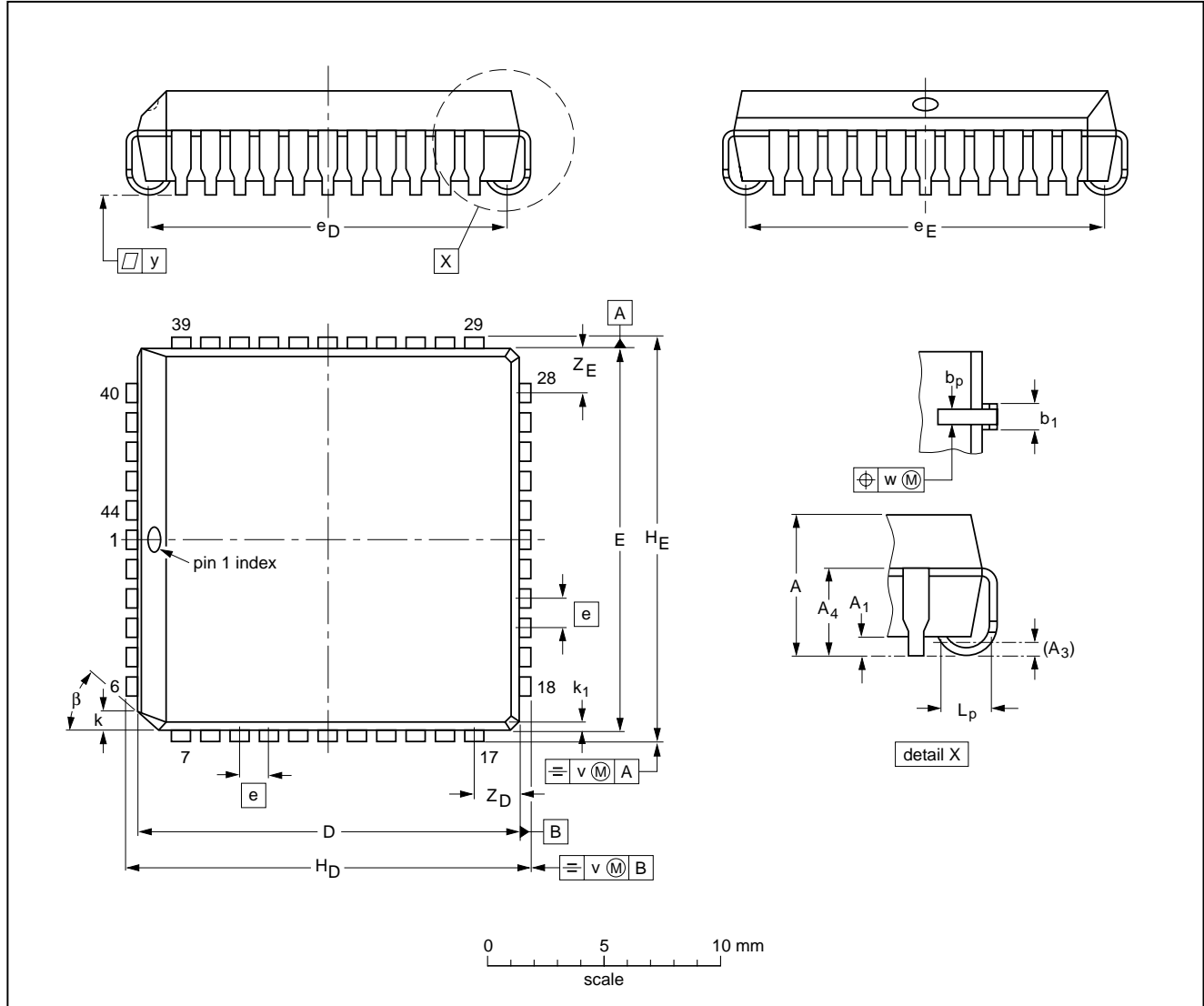
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PACKAGE OUTLINE

PLCC44: plastic leaded chip carrier; 44 leads

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DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A ₁ min.	A ₃	A ₄ max.	b _p	b ₁	D ⁽¹⁾	E ⁽¹⁾	e	e _D	e _E	H _D	H _E	k	k ₁ max.	L _p	v	w	y	Z _D ⁽¹⁾ max.	Z _E ⁽¹⁾ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				92-11-17 95-02-25

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SOLDERING**Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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Printed in The Netherlands

547047/20/01/pp16

Date of release: 1997 Jun 10

Document order number: 9397 750 01609

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