DATA SHEET

SAA2501
Digital Audio Broadcast (DAB) decoder

Preliminary specification
File under Integrated Circuits, IC01

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Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Advanced error protection
- Integrated audio post processing for control of signal level and inter-channel crosstalk
- Demultiplexing of Program Associated Data (PAD) in the input bitstream
- Automatic digital de-emphasis of the decoded audio signal
- Separate master and slave inputs
- Automatic sample frequency and bit-rate switching in master input mode
- Automatic synchronization of input and output interface clocks in master input mode
- Selectable audio output precision; 16, 18, 20 or 22 bit
- Low power consumption
- Decoded sub-band signal and error flag outputs for error concealment.

2 APPLICATION

- Digital Audio Broadcast systems as defined in *"Eureka 147"*.

3 GENERAL DESCRIPTION

The SAA2501 audio source decoder supports ISO/IEC MPEG layers I and II and all DAB specific features as described in *"Eureka 147 draft specification (EU147)"*.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA2501H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

Supply of this *"ISO/IEC 11172-3"* audio standard Layer I or layer II compatible IC does not convey a licence nor imply a right under any patent, or any Industrial or Intellectual Property Right, to use this IC in any ready-to-use electronic product.

5 BLOCK DIAGRAM

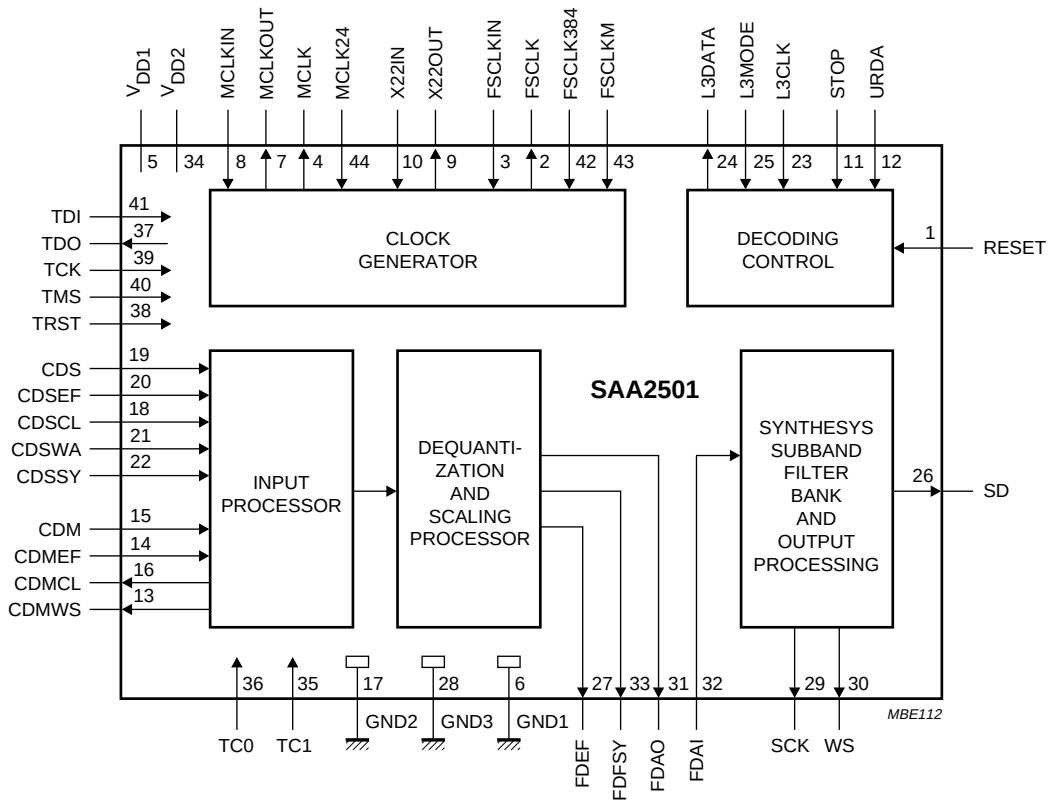

Fig.1 Functional block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
RESET	1	master reset input	I
FSCLK	2	sample rate clock output; buffered signal	O
FSCLKIN	3	sample rate clock signal input (see Table 1)	I
MCLK	4	master clock output; buffered signal	O
V_{DD1}	5	supply voltage 1	–
GND1	6	ground 1	–
MCLKOUT	7	master clock oscillator output	O
MCLKIN	8	master clock oscillator input or signal input	I
X22OUT	9	22.579 MHz clock oscillator output	O
X22IN	10	22.579 MHz clock oscillator input or signal input	I
STOP	11	stop decoding input	I
URDA	12	unreliable data input; interrupt decoding	I
CDMWS	13	coded data (master input) word select output	O
CDMEF	14	coded data (master input) error flag input	I
CDM	15	ISO/MPEG coded data (master input)	I
CDMCL	16	coded data (master input) bit clock output	O
GND2	17	ground 2	–
CDSCL	18	coded data (slave input) bit clock	I
CDS	19	ISO/MPEG or EU147 (see Table 8) coded data (slave input)	I
CDSEF	20	coded data (slave input) error flag	I
CDSWA	21	coded data (slave input) burst window signal	I
CDSSY	22	coded data (slave input) frame sync	I
L3CLK	23	L3 interface bit clock input	I
L3DATA	24	L3 interface serial data input/output	I/O
L3MODE	25	L3 interface address/data select input	I
SD	26	baseband audio I^2S data output	O
FDEF	27	filter data error flag output	O
GND3	28	ground 3	–
SCK	29	baseband audio data I^2S clock output	O
WS	30	baseband audio data I^2S word select output	O
FDAO	31	filter data output	O
FDAI	32	filter data input	I
FDFSY	33	filter data output frame sync	O
V_{DD2}	34	supply voltage 2	–
TC1	35	do not connect; factory test control 1 input, with integrated pull-down resistor	I
TC0	36	do not connect; factory test control 0 input, with integrated pull-down resistor	I
TDO	37	boundary scan test data output	O
TRST	38	boundary scan test reset input; this pin should be connected to ground for normal operation	I
TCK	39	boundary scan test clock input	I

SYMBOL	PIN	DESCRIPTION	TYPE
TMS	40	boundary scan test mode select input	I
TDI	41	boundary scan test data input	I
FSCLK384	42	sample rate clock frequency indication input	I
FSCLKM	43	sample rate clock source selection for the master input	I
MCLK24	44	master clock frequency indication input	I

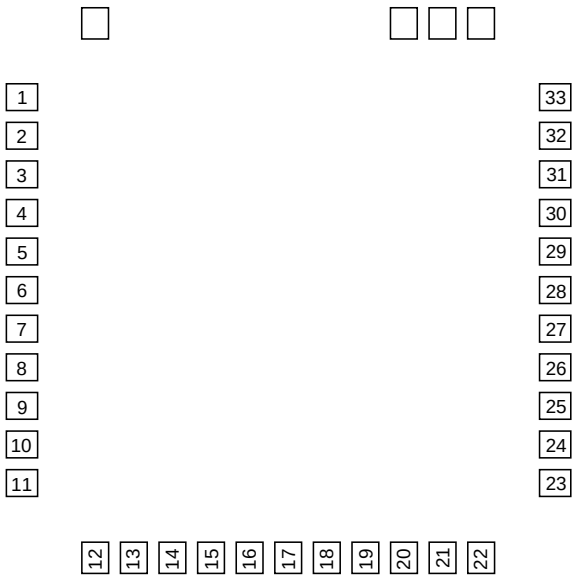

Fig.2 Pin configuration (QFP44).