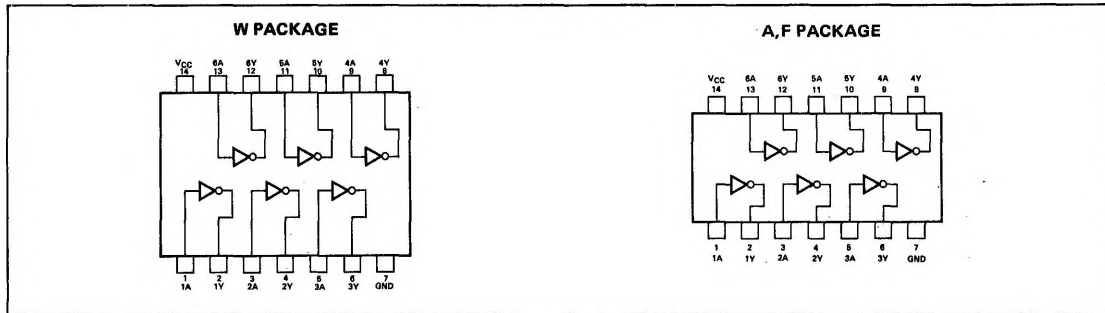


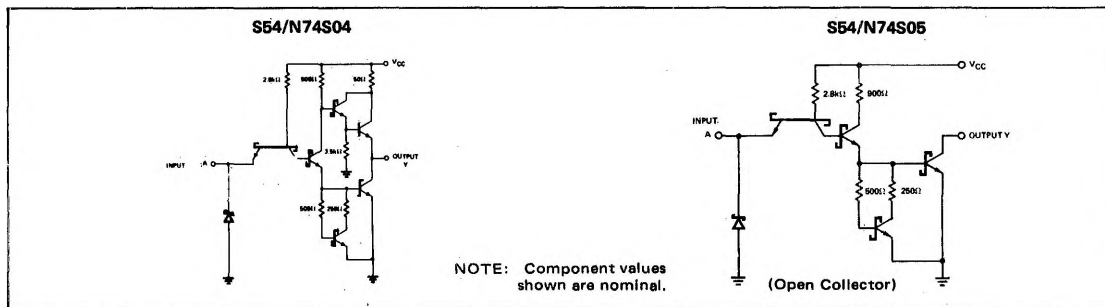
S54S04-A,F,W • S54S05-A,F,W • N74S04-A,F,W • N74S05-A,F

DIGITAL 54/74 TTL SERIES

PIN CONFIGURATIONS



SCHEMATIC (each gate)



RECOMMENDED OPERATING CONDITIONS

	S54S04			N74S04			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	High logic level		20	Low logic level		10	
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input clamp voltage			-1.2	V
V_{OH}	High-level output voltage				V
V_{OL}	Low-level output voltage			0.5	V
I_I	Input current at maximum input voltage			1	mA
I_{IH}	High-level input current (each input)			50	μA
I_{IL}	Low-level input current (each input)			-2	mA
I_{OS}	Short-circuit output current†	-40		-100	mA
I_{CCH}	Supply current, high-level output (average per gate)		2.5	4	mA
I_{CCL}	Supply current, low-level output (average per gate)		5	9	mA

DIGITAL 54/74 TTL SERIES ■ S54S04, S54S05, N74S04, N74S05

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 10$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$	NOTE 1	2	3	4.5	ns
		$C_L = 50\text{ pF}$, $R_L = 280\ \Omega$			4.5		
t_{PHL}	Propagation delay time, high-to-low-level output	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$		2	3	5	ns
		$C_L = 50\text{ pF}$, $R_L = 280\ \Omega$			5*		

S54/N74S05

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}$, $V_{OH} = 5.5V$	$I_I = -18\text{ mA}$, $V_{IL} = 0.8V$,			-1.2	V
I_{OH}	High-level output current	$V_{CC} = \text{MIN}$, $I_{OL} = 20\text{ mA}$	$V_{IH} = 2V_I$			250	μA
V_{OL}	Low-level output voltage					0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$,	$V_I = 5.5V$			1	mA
I_{IH}	High-level input current (each input)	$V_{CC} = \text{MAX}$,	$V_I = 2.7V$			50	μA
I_{IL}	Low-level input current (each input)	$V_{CC} = \text{MAX}$,	$V_I = 0.5V$			-2	mA
I_{CCH}	Supply current, high-level output (average per gate)	$V_{CC} = \text{MAX}$,	All inputs at 0V		1.5	3.3	mA
I_{CCL}	Supply current, low-level output (average per gate)	$V_{CC} = \text{MAX}$,	All inputs at 5V		5	9	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 10$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$	NOTE 1	2	5	7.5	ns
		$C_L = 50\text{ pF}$, $R_L = 280\ \Omega$			7.5		
t_{PHL}	Propagation delay time, high-to-low-level output	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$		2	4.5	7	ns
		$C_L = 50\text{ pF}$, $R_L = 280\ \Omega$			7		

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES:

A. The pulse generator has the following characteristics: $V_{in(1)} = 3V$, $V_{in(0)} = 0V$, $t_1 = t_0 = 2.5\text{ ns}$, $\text{PRR} = 1\text{ MHz}$, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

B. Inputs not under test are at 2.7V.

C. C_L includes probe and jig capacitance.

NOTE 1: Load circuit and waveforms are shown on page 2-293