Features

- **Low-noise Low Drop Out Voltage Regulator**
- **Programmable at 2.8V or 2.9V Output Voltages**
- **3V to 5.5V Supply Operation**
- **30 mA Maximum Load Current**
- **Power-down Mode Consumption Less Than 1 µA**
- **Macrocell for Integration into System-on-chip Products**
- **More Than 70 dB (Typical) PSRR at 1 kHz**
- **32µ V_{RMS} Output Noise**
- **0.35 µm CMOS Technology**
- **Typical Application: Radio Section Supply in Mobile Terminals**

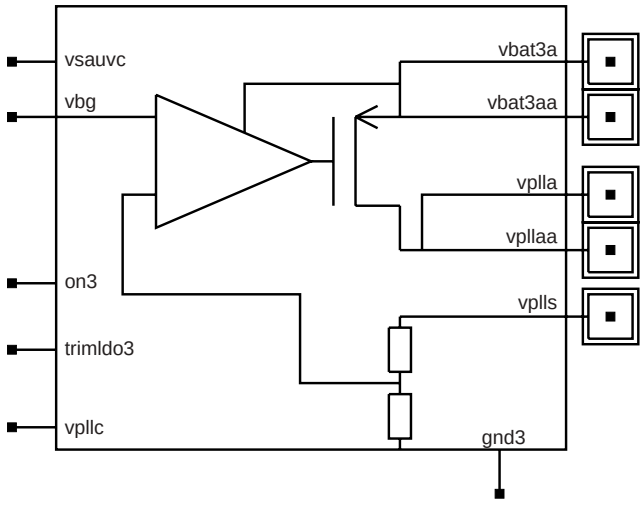
Description

RE025 is a Low Drop Out (LDO) voltage regulator macrocell with programmable 2.8V or 2.9V output voltages, rated for loads of up to 30 mA. It is designed to be integrated with other analog cells, digital logic, microcontrollers, DSP cores and memory blocks into system-on-chip products.

The circuit consists of a PMOS pass device, an error amplifier and a feedback resistive network, sized to achieve the required closed loop gain. These blocks make up the regulating loop. An over-current and short circuit protection circuit has been included to limit the output current delivered by the regulator, thus avoiding destruction in case of a short circuit.

An external reference voltage (bandgap voltage) is necessary for correct functionality. The target reference voltage is 1.231V, delivered, for example, by BG019. Double pads on the supply voltage V_{BAT3A}/V_{BAT3AA} and output voltage V_{PLLA}/V_{PLLAA} are used to reduce the total output resistance. Current reference is generated inside the cell through a circuit supplied by a 2.5V ± 0.1V regulated input voltage on V_{SAUVC}. Remote sense terminal V_{PLLS} provides regulation at the load by connecting it to the output terminal near a critical point to improve performance of the regulator (e.g., connecting them at the package pin by double-bonding thus avoiding the bonding resistance influence). A ceramic capacitor of 2.2 µF connected from V_{PLLA}/V_{PLLAA} to ground is needed as external compensation.

Figure 1. Symbol[1]



Note: 1. Pin names are written as they appear on the user screen when the symbol is opened in the design tool environment.

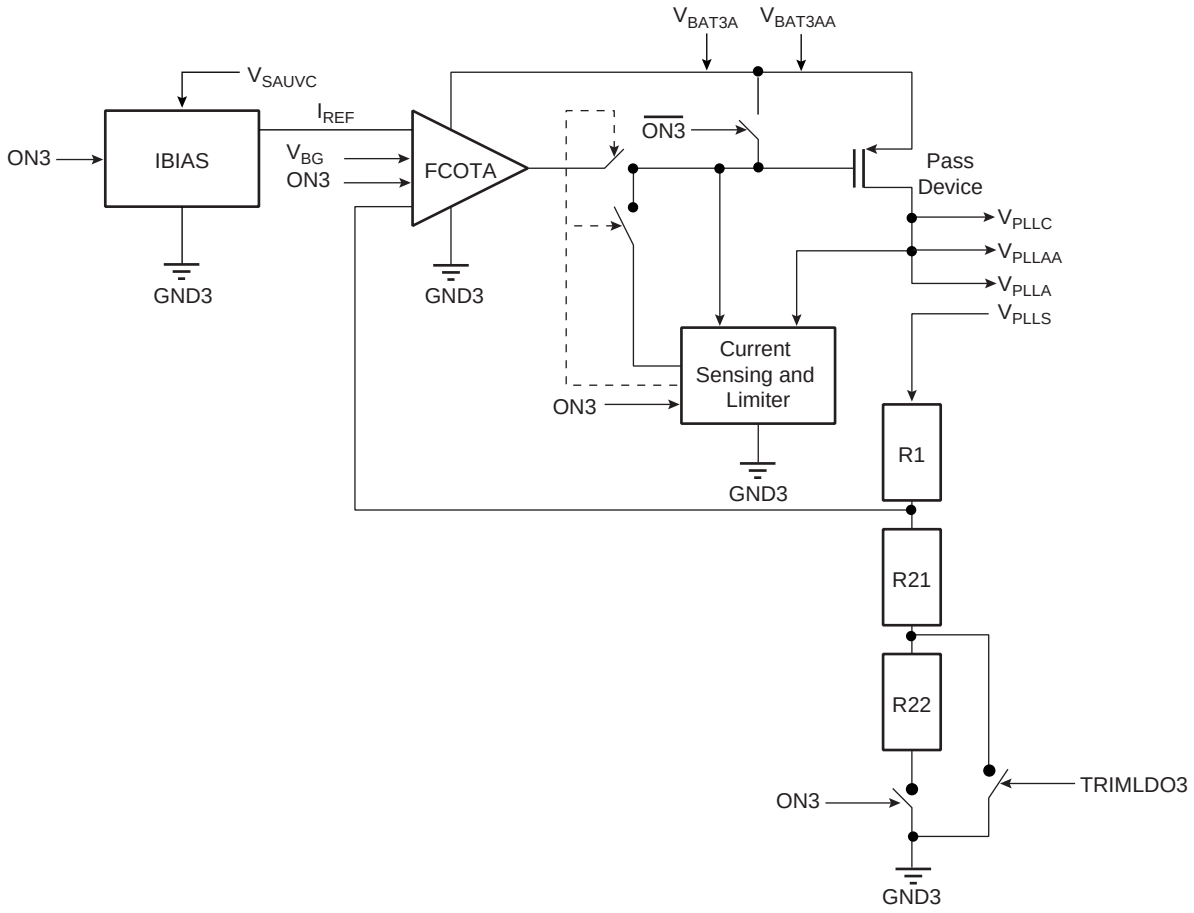
Embedded ASIC Macrocell: Power Management for Mobile Terminals (PM)

RE025 Programmable 2.8V or 2.9V 30 mA Low-noise LDO Voltage Regulator

Rev. 2700B-PMGMT–02/03

Functional Diagram

Figure 2. Functional Diagram



Pin Description

Pin Name	I/O	Type	Function	Value
V_{BAT3A}	Power supply	External pad	Power supply	3V to 5.5V
V_{BAT3AA}	Power supply	External pad	Power supply	3V to 5.5V
V_{PLLA}	Analog output	External pad	Output voltage	2.75V to 2.935V
V_{PLLAA}	Analog output	External pad	Output voltage	2.75V to 2.935V
V_{PLLS}	Analog input	External pad	Sense voltage	2.75V to 2.935V
V_{PLLC}	Analog output	Internal pin	Output voltage	2.75V to 2.935V
GND3	Ground	Internal pin	Ground	0V
V_{SAUVC}	Power supply	Internal pin	Power supply	2.5V ± 0.1V
V_{BG}	Analog input	Internal pin	Voltage reference	1.231V
ON3	Digital input	Internal pin	Enable command	0V or V_{BAT3A}/V_{BAT3AA}
TRIMLDO3	Digital input	Internal pin	Output voltage selection	0V or V_{BAT3A}/V_{BAT3AA}

Absolute Maximum Ratings*

V_{IN}	-0.3V to 6.5V
Digital Signals	-0.3V to 5.5V
Output Current	Internally Limited
Junction Temperature	-40°C to 150°C

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications(1)

T_J = -20°C to 125°C, V_{BAT3A}/V_{BAT3AA} = 3V to 5.5V unless otherwise specified, output capacitance = 2.2 µF.

Table 1. Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{BAT3A}/V_{BAT3AA}	Operating Supply Voltage		3		5.5	V
V_{SAUVC}	Auxiliary Operating Supply Voltage		2.4	2.5	2.6	V
T_J	Junction Temperature Range		-20		125	°C
V_{PLLA}/V_{PLLAA}	Output Voltage	TRIMLDO3 = 0	2.75	2.8	2.85	V
		TRIMLDO3 = V_{BAT3A}/V_{BAT3AA}	2.855	2.9	2.935	V
I_{PLLA}/I_{PLLAA}	Output Current				30	mA
I_{CC}	Quiescent Current	Any condition		140	250	µA
ΔV_{DC}	Line Regulation @2.8V	I_{PLLA}/I_{PLLAA} = 30 mA		2	3	mV
ΔV_{TRAN}	Transient Line Regulation @2.8V	I_{PLLA}/I_{PLLAA} = 30 mA rise time = fall time = 5 µs		2	3	mV
ΔV_{DC}	Load Regulation @2.8V	10% - 90% of I_{PLLA}/I_{PLLAA}		2	3	mV
ΔV_{TRAN}	Transient Load Regulation @2.8V	10% - 90% of I_{PLLA}/I_{PLLAA} rise time = fall time = 5 µs		2	10	mV
ΔV_{DC}	Line Regulation @2.9V	I_{PLLA}/I_{PLLAA} = 30 mA		2	3	mV
ΔV_{TRAN}	Transient Line Regulation @2.9V	I_{PLLA}/I_{PLLAA} = 30 mA rise time = fall time = 5 µs		2	6	mV
ΔV_{DC}	Load Regulation @2.9V	10% - 90% of I_{PLLA}/I_{PLLAA}		2	4	mV
ΔV_{TRAN}	Transient Load Regulation @2.9V	10% - 90% of I_{PLLA}/I_{PLLAA} rise time = fall time = 5 µs		3	13	mV

Table 1. Electrical Specifications (Continued)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
PSRR	Power Supply Rejection Ratio at Full Load	V_{BAT} = 3V	@100 Hz		-75		dB
			@1 kHz		-75		dB
			@20 kHz		-45		dB
			@100 kHz		-35		dB
		V_{BAT} = 4.25V	@100 Hz		-75		dB
			@1 kHz		-75		dB
			@20 kHz		-55		dB
			@100 kHz		-45		dB
		V_{BAT} = 5.5V	@100 Hz		-75		dB
			@1 kHz		-75		dB
			@20 kHz		-60		dB
			@100 kHz		-45		dB
V_N	Output Noise(2)	Bandwidth = 10 Hz to 100 kHz; output current = 30 mA			32	50	µ V_{RMS}
T_R	Rise Time	100% of I_{PLLA}/I_{PLLAA} 10% - 90% of V_{PLLA}/V_{PLLAA}				200	µs
I_{SD}	Shut Down Current					1	µA
I_{CC}	Short-circuit Current Threshold					170	mA

Notes: 1. Obtained by considering the parasitics of a TFBGA100 Package.
2. Obtained by using BG019 as reference voltage generator.

Control Modes

All digital signals are referred to the supply voltage $V_{BAT3A/BAT3AA}$.

Table 2. Truth Table

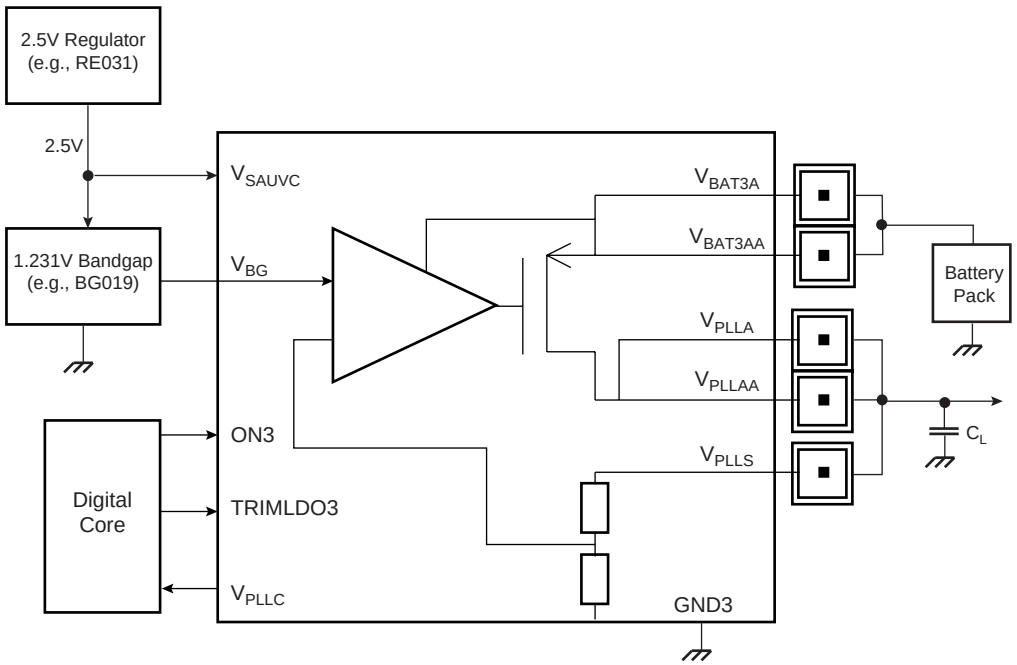
ON3	TRIMLDO3	V_{PLLA}/V_{PLLAA}
0	X	Power down (High-Z)
1	0	Power on, V_{PLLA}/V_{PLLAA} = 2.8V
1	1	Power on, V_{PLLA}/V_{PLLAA} = 2.9V

Application Example

A ceramic capacitor of 2.2 µF with ESR between 20 mΩ and 250 mΩ connected from V_{PLLA}/V_{PLLAA} to ground is needed for external compensation.

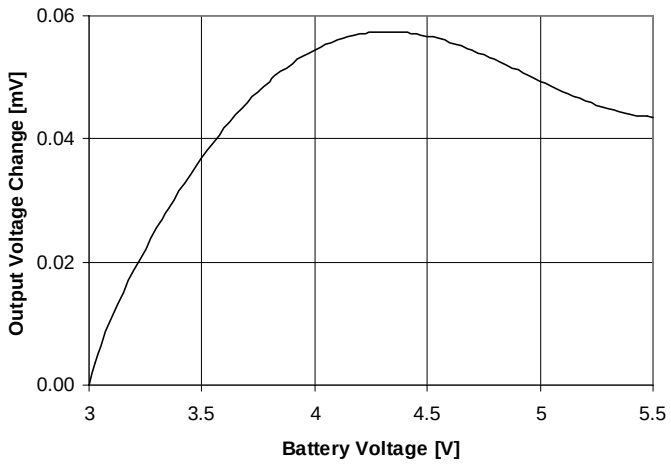
Description	Min	Typ	Max	Units
Capacitor (C_L)	1.8	2.2	2.6	µF

Figure 3. Application Example

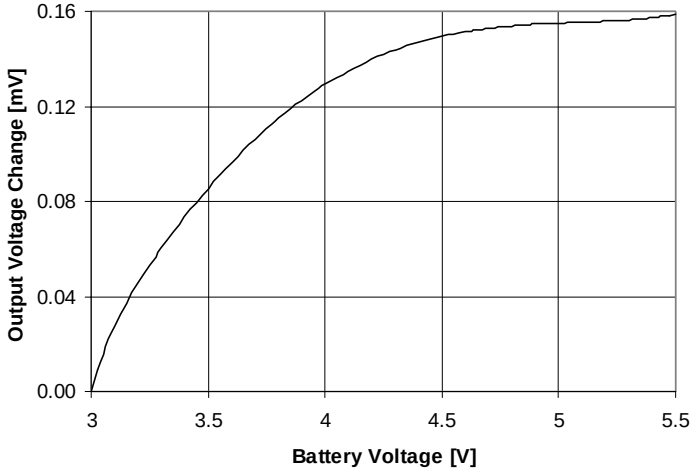


Typical Performance Characteristics (Conditions as specified on page 9)

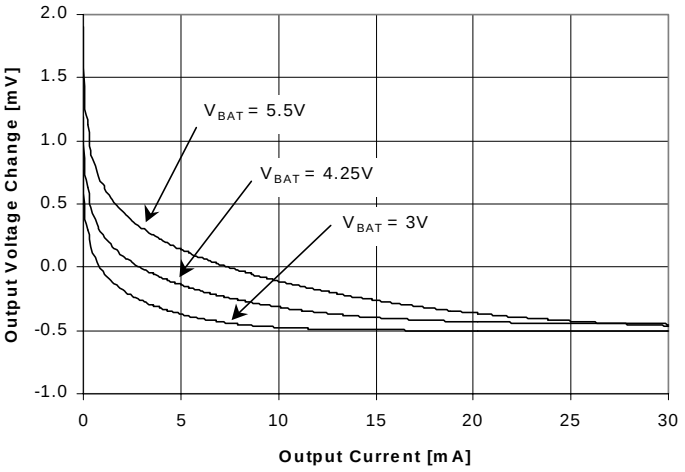
Static Line Regulation at Full Load and TRIMLDO3 = 0



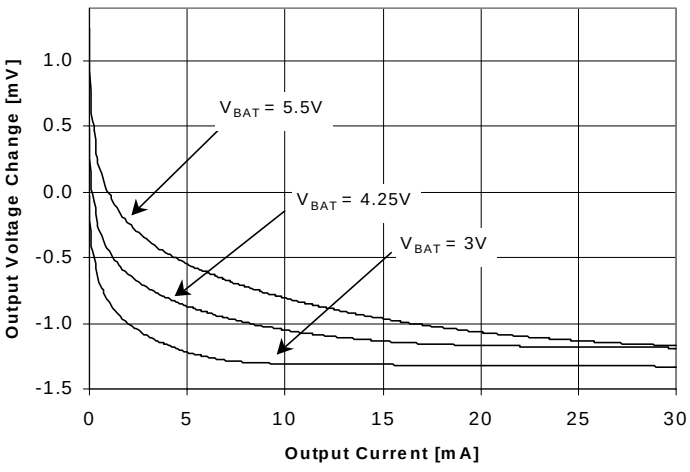
Static Line Regulation at Full Load and TRIMLDO3 = V_{BAT}



Static Load Regulation with TRIMLDO3 = 0

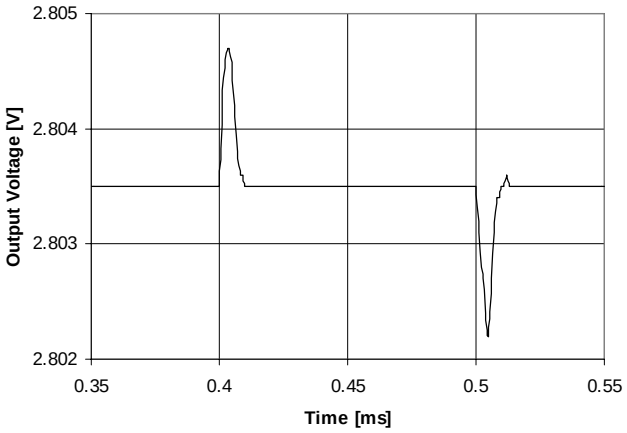


Static Load Regulation with TRIMLDO3 = V_{BAT}

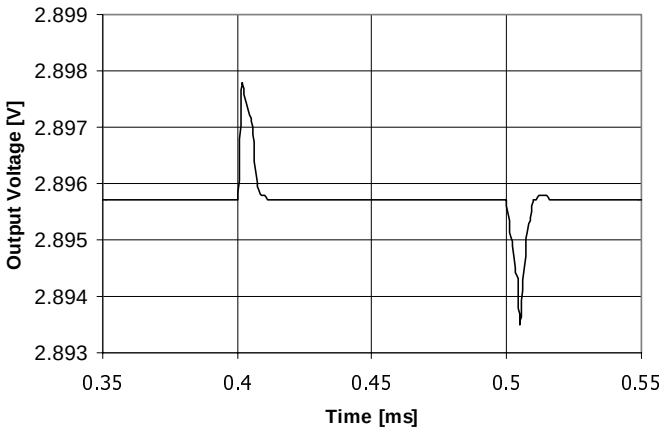


Typical Performance Characteristics (Conditions as specified on page 9)

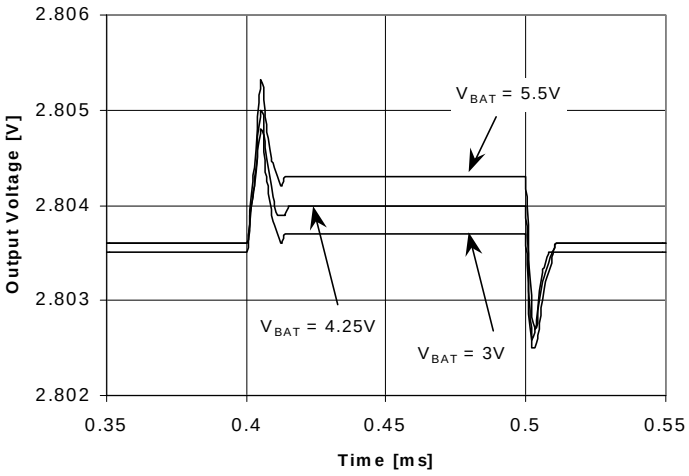
Transient Line Regulation at Full Load and TRIMLDO3 = 0



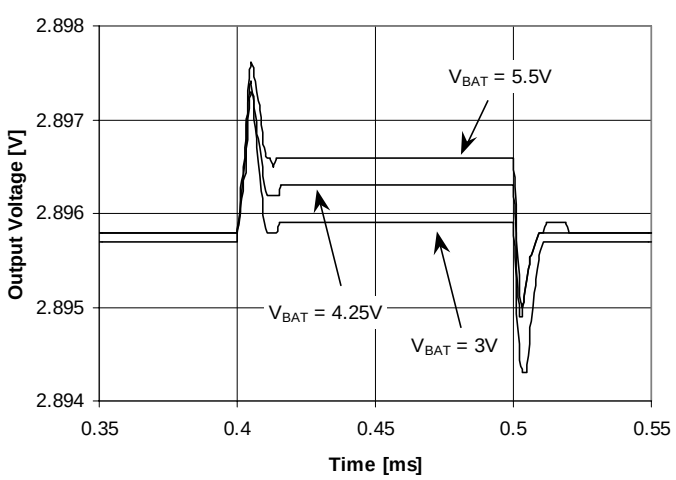
Transient Line Regulation at Full Load and TRIMLDO3 = V_{BAT}



Transient Load Regulation with TRIMLDO3 = 0

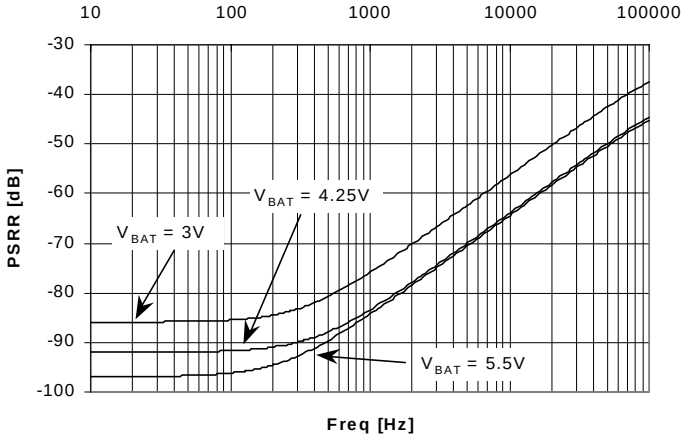


Transient Load Regulation with TRIMLDO3 = V_{BAT}

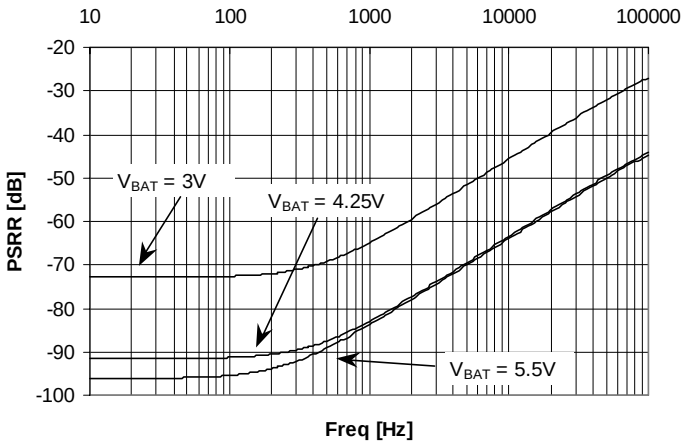


Typical Performance Characteristics (Conditions as specified on page 9)

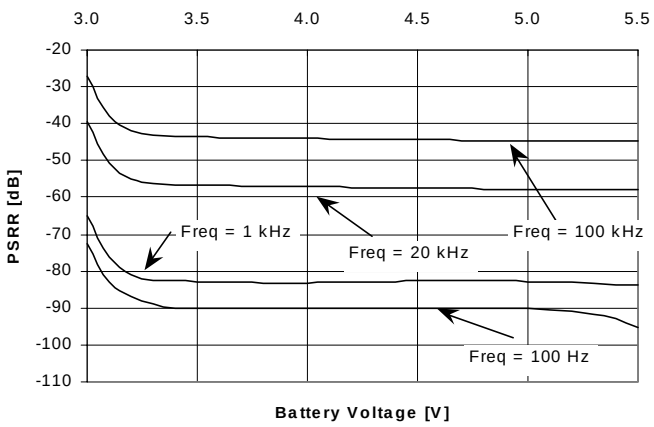
Power Supply Rejection Ratio at Full Load for TRIMLDO3 = 0



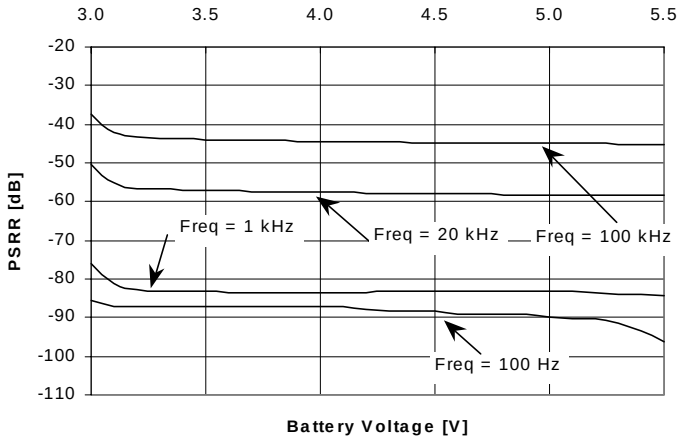
Power Supply Rejection Ratio at Full Load for TRIMLDO3 = V_{BAT}



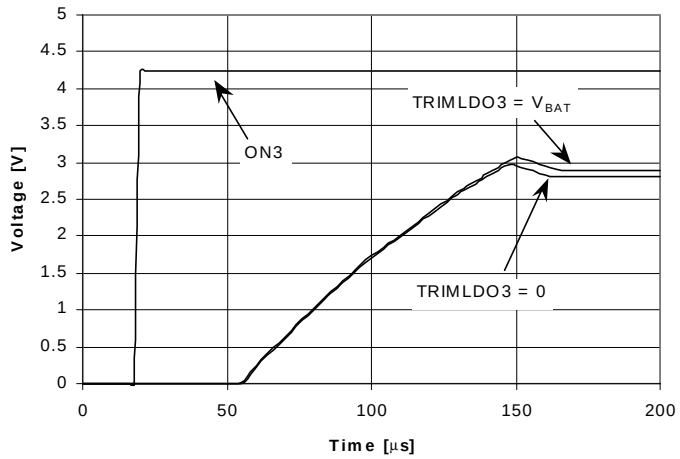
Power Supply Rejection Ratio at Full Load versus Battery Voltage and TRIMLDO3 = V_{BAT}



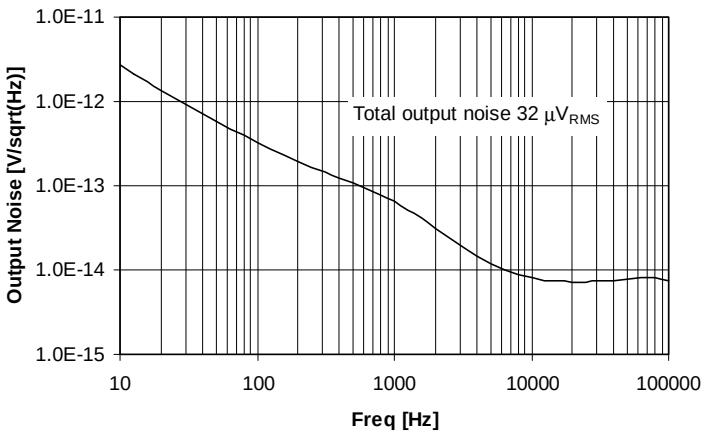
Power Supply Rejection Ratio at Full Load versus Battery Voltage and TRIMLDO3 = 0



LDO Startup at Full Load for V_{BAT} = 4.25V



Output Noise Spectrum at Full Load for TRIMLDO3 = 0, V_{BAT} = 4.25V and C_L = 2.2 µF

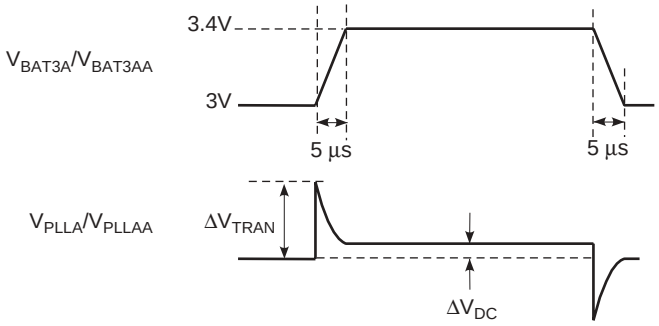


Terminology

Line Regulation

Measures the maximum transient and DC variations of the output voltage of the LDO when the supply changes between two specified values with fixed load current; minimum rise time and fall time is 5 µs.

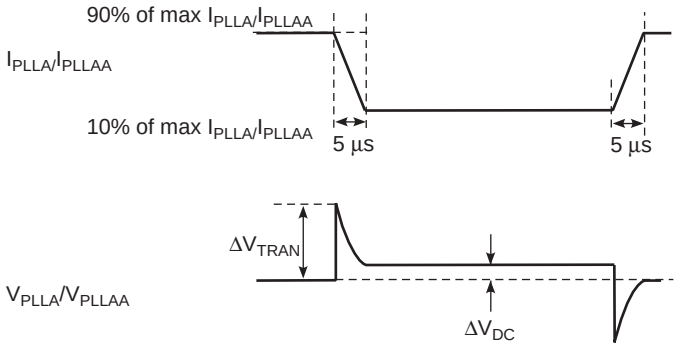
Figure 4. Line Regulation



Load Regulation

Measures the maximum transient and DC variations of the output voltage of the LDO when the load current changes between two specified values with fixed power supply; minimum rise time and fall time is 5 µs.

Figure 5. Load Regulation



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