



High-speed CMOS QuickSwitch Buffers

QS3245

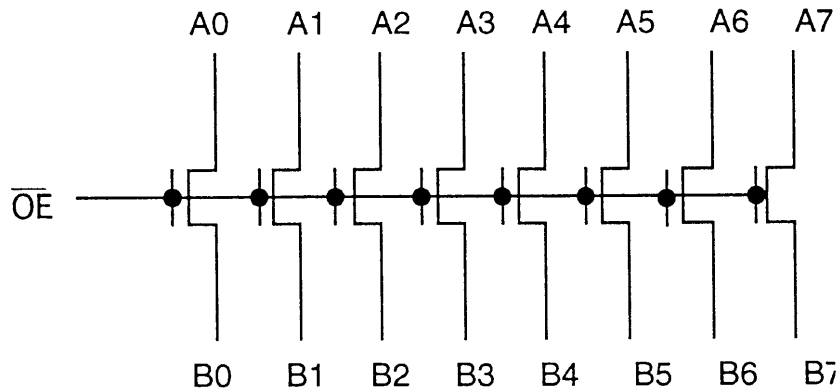
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Pin compatible to the 74F245, 74FCT245, and 74FCT245T
- Low power CMOS proprietary technology
- Zero propagation delay
- TTL-compatible control inputs
- Zero ground bounce
- Available in 20-pin DIP, SOIC, and QSOP

DESCRIPTION

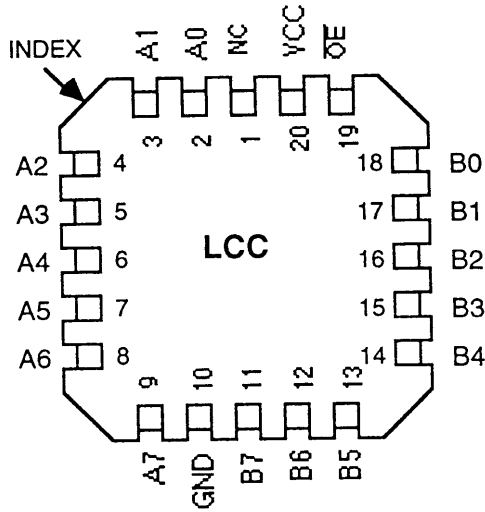
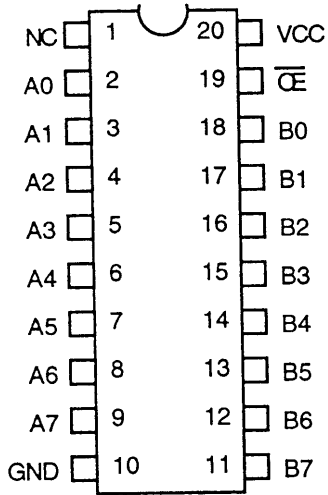
The QS3245 provides a set of eight high-speed CMOS TTL-compatible bus switches in a pinout compatible with 74FCT245, 74F245, 74ALS/AS/LS245 8-bit transceivers. The low on resistance (5 ohms) of the 3245 allows inputs to be connected outputs without adding propagation delay and without generating additional ground bounce noise. The Output enable (\overline{OE}) signal turns the switches on similar to the \overline{OE} signal of the 74'245.

FUNCTIONAL BLOCK DIAGRAM



3245 PINOUT

PDIP, SOIC, QSOP



ALL PINS TOP VIEW

3245 PIN DESCRIPTION

Name	Description
OE	Output Enable
An	Data I/O's
Bn	Data I/O's

3245 FUNCTION TABLE

OE	OUTPUTS
H	Disconnected
L	An = Bn

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Switch Voltage V_S	-0.5V to +7.0V
DC Input Voltage V_I	-0.5V to +7.0V
AC Input Voltage (for a pulse width 20 ns).....	-3.0V
DC Channel Current Max. current/pin.....	120 mA
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

2

$T_A = 25^\circ C, f = 1\text{ MHz}, V_{in} = 0V, V_{out} = 0V$

Pins	SOIC		QSOP		PDIP		Unit
	Typ	Max	Typ	Max	Typ	Max	
Controls	3	4	3	4	4	5	pF
QuickSwitch Channels	7	8	7	8	8	9	

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A = 0^\circ C$ to $70^\circ C, V_{CC} = 5.0V \pm 5\%$ Military $T_A = -55^\circ C$ to $125^\circ C, V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{ih}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	-	-	Volts
V_{il}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	-	-	0.8	Volts
I_{lin}	Input Leakage Current	$0 \leq V_{in} \leq V_{CC}$	-	-	5	μA
I_{loz}	Off State Current (Hi-Z)	$0 \leq A, B \leq V_{CC}$	-	-	5	μA
I_{los}	Short Circuit Current (2)	A (B) = 0V, B (A) = V_{CC}		300		mA
R_{on}	Switch On Resistance (Note 3)	$V_{CC} = \text{Min}, V_{in} = 0.0\text{ Volts}$ $I_{on} = 30\text{ mA}$	-	5	7	Ω
		$V_{CC} = \text{Min}, V_{in} = 2.4\text{ Volts}$ $I_{on} = 15\text{ mA}$	-	10	15	

Notes:

1. Typical values indicate $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.
2. Not more than one output should be used to test this high power condition, and the duration is 1 second.
3. Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two pins.
4. During input/output leakage testing all pins are at a High or Low state, and the OE control is High.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Typ	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, V _i = GND or V _{cc} , f = 0	-	-	2.5	mA
ΔI _{cc}	Pwr Supply Current, per Input High (2)	V _{cc} = MAX, Input = 3.4 V, f = 0 Per control input	-	-	3.5	mA
Q _{ccd}	Dynamic Pwr Supply Current per MHz (3)	V _{cc} = MAX, A & B pins open, Control input toggling @ 50% duty cycle	-	-	0.25	mA/MHz

Notes:

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_i=3.4V, control inputs only). A and B pins do not contribute to I_{cc}.
3. Guaranteed by design. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0° C to 70° C, V_{cc} = 5.0V±5% Military T_A = -55° C to 125° C, V_{cc} = 5.0V±10%
 Cload = 50 pF, Rload = 500 unless otherwise noted.

Symbol	Description	Note	Com		Mil		Unit
			Min	Max	Min	Max	
t _{AB}	Data Propagation Delay An to/from Bn	1,2,3		0.25		0.25	ns
t _{OEY}	Switch Turn On Delay OE to An/Bn	1	0.5	5.6	0.5	6.6	ns
t _{PLZ} t _{PHZ}	Switch Turn Off Delay OE to An/Bn	1,2	0.5	4.5	0.5	5.5	ns

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.