

## 2- $V_{RMS}$ DirectPath™, 112/106/100-dB Audio Stereo DAC With 32-Bit, 384-kHz PCM Interface

Check for Samples: [PCM5100-Q1 \(Preliminary\)](#), [PCM5101-Q1 \(Preliminary\)](#), [PCM5102-Q1](#)

### FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Market-Leading Low Out-of-Band Noise
- Selectable Digital-Filter Latency and Performance
- No DC Blocking Capacitors Required
- Integrated Negative Charge Pump
- Internal Pop-Free Control For Sample-Rate Changes or Clock Halts
- Intelligent Muting System; Soft Up/Down Ramp and Analog Mute For 120-dB Mute SNR With Popless Operation.
- Integrated High-Performance Audio PLL With BCK Reference to Generate SCK Internally
- Small 20-pin TSSOP Package

### Typical Performance (3.3-V Power Supply)

Parameter	PCM5102-Q1 / PCM5101-Q1 / PCM5100-Q1
SNR	112 / 106 / 100 dB
Dynamic range	112 / 106 / 100 dB
THD+N at –1 dBFS	–93 / –92 / –90 dB
Full-scale output	2.1 $V_{RMS}$ (GND center)
Normal 8× oversampling digital-filter latency: 22 / $f_S$	
Low-latency 8× oversampling digital-filter latency: 3.5 / $f_S$	
Sampling frequency	8 kHz to 384 kHz
System clock multiples ( $f_{SCK}$ ): 64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, 3072; up to 50 MHz	



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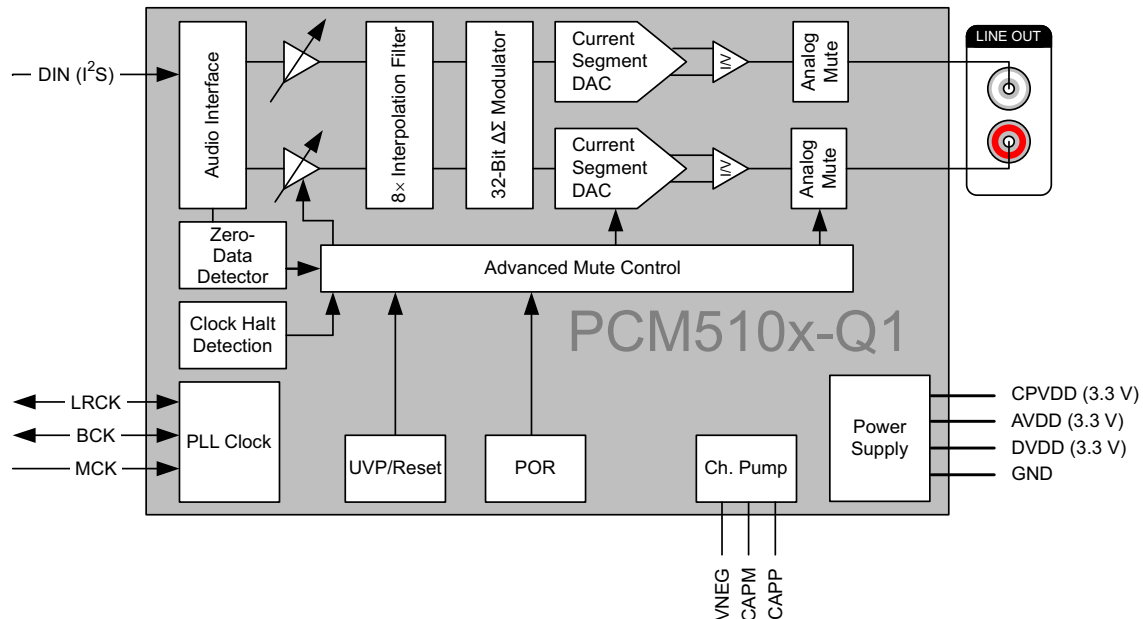


Figure 1. PCM510x-Q1 Functional Block Diagram

## OTHER KEY FEATURES

- Accepts 16-, 24-, and 32-Bit Audio Data
- PCM Data Formats: I<sup>2</sup>S, Left-Justified
- Automatic Power-Save Mode When LRCK And BCK Are Deactivated.
- 3.3-V Failsafe LVCMOS Digital Inputs
- Hardware Configuration
- Single-Supply Operation:
  - 3.3-V Analog, 3.3-V Digital
- Integrated Power-On Reset

## APPLICATIONS

- A/V Receivers
- DVD, BD Players
- HDTV Receivers
- Applications Requiring 2-V<sub>RMS</sub> Audio Output

## DESCRIPTION

The PCM510x-Q1 family is a series of monolithic CMOS integrated circuits that include a stereo digital-to-analog converter and additional support circuitry in a small TSSOP package. The PCM510x-Q1 uses the latest generation of TI's advanced segment-DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter.

The PCM510x-Q1 provides 2.1-V<sub>RMS</sub> ground centered outputs, allowing designers to eliminate not only dc blocking capacitors on the output, but also external muting circuits traditionally associated with single-supply line drivers.

The integrated line driver surpasses all other charge-pump-based line drivers by supporting loads down to 1 kΩ. By supporting loads down to 1 kΩ, the PCM510x-Q1 can essentially drive up to 10 products in parallel. (LCD TV, DVDR, AV receivers, and so on).

The integrated PLL on the device removes the requirement for a system clock (commonly known as master clock). This allows a three-wire I<sup>2</sup>S connection, along with reduced system EMI.

Intelligent clock error and PowerSense undervoltage protection uses a two-level mute system for pop-free performance. On clock error or system power failure, the device digitally attenuates the data (or last known-good data), then mutes the analog circuit

Compared with existing DAC technology, the PCM510x-Q1 offers up to 20-dB lower out-of-band noise, reducing EMI and aliasing in downstream amplifiers/ADCs. (from traditional 100-kHz OBN measurements all the way to 3 MHz)

The PCM510x-Q1 accepts industry-standard audio data formats with 16- to 32-bit data. Sample rates up to 384 kHz are supported.

**Table 1. Ordering Information**

Part Number	T <sub>A</sub>	Top-Side Symbol
PCM5100TPWRQ1 (Preview)	–40°C to 105°C	PCM5100Q
PCM5101TPWRQ1 (Preview)	–40°C to 105°C	PCM5101Q
PCM5102TPWRQ1	–40°C to 105°C	PCM5102Q

F

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage	AVDD, CPVDD, DVDD	–0.3 to 3.9	V
Digital input voltage		–0.3 to 3.9	
Analog input voltage		–0.3 to 3.9	
Operating temperature range		–25 to 85	°C
Storage temperature range		–65 to 150	
ESD rating	Human-body model (HBM) AEC-Q100 Classification Level H2	2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B	750	V

**THERMAL CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\theta_{JA}$	Theta JA	High K		91.2		°C/W
$\psi_{JT}$	Psi JT			1		
$\psi_{JB}$	Psi JB			41.5		
$\theta_{JC}$	Theta JC	Top		25.3		
$\theta_{JB}$	Theta JB			42		

**RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
<b>Power-Supply Requirements</b>						
DV <sub>DD</sub>	Digital supply voltage	Target DV <sub>DD</sub> = 3.3 V	3	3.3	3.6	VDC
AV <sub>DD</sub>	Analog supply voltage		3	3.3	3.6	VDC
CPV <sub>DD</sub>	Charge-pump supply voltage		3	3.3	3.6	VDC
I <sub>DD</sub>	DV <sub>DD</sub> supply current at 3.3 V <sup>(1)</sup>	f <sub>S</sub> = 48 kHz		7	12	mA
		f <sub>S</sub> = 96 kHz		8		
		f <sub>S</sub> = 192 kHz		9		
I <sub>DD</sub>	DV <sub>DD</sub> supply current at 3.3 V <sup>(2)</sup>	f <sub>S</sub> = 48 kHz		8	13	mA
		f <sub>S</sub> = 96 kHz		9		
		f <sub>S</sub> = 192 kHz		10		
I <sub>DD</sub>	DV <sub>DD</sub> supply current at 3.3 V <sup>(3)</sup>			0.5	0.8	mA
I <sub>CC</sub>	AV <sub>DD</sub> / CPV <sub>DD</sub> supply current <sup>(1)</sup>	f <sub>S</sub> = 48 kHz		11	16	mA
		f <sub>S</sub> = 96 kHz		11		
		f <sub>S</sub> = 192 kHz		11		

(1) Input is bipolar-zero data.

(2) Input is 1-kHz, –1-dBFS data.

(3) Power-down mode

## RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
<b>Power-Supply Requirements</b>						
I <sub>CC</sub>	AV <sub>DD</sub> / CPV <sub>DD</sub> supply current <sup>(2)</sup>	f <sub>S</sub> = 48 kHz		22	32	mA
		f <sub>S</sub> = 96 kHz		22		
		f <sub>S</sub> = 192 kHz		22		
I <sub>CC</sub>	AV <sub>DD</sub> / CPV <sub>DD</sub> supply current <sup>(3)</sup>	f <sub>S</sub> = N/A		0.2	0.4	mA
	Power dissipation, DV <sub>DD</sub> = 3.3 V <sup>(1)</sup>	f <sub>S</sub> = 48 kHz		59.4	92.4	mW
		f <sub>S</sub> = 96 kHz		62.7		
		f <sub>S</sub> = 192 kHz		66		
	Power dissipation, DV <sub>DD</sub> = 3.3 V <sup>(2)</sup>	f <sub>S</sub> = 48 kHz		99	148.5	mW
		f <sub>S</sub> = 96 kHz		102.3		
		f <sub>S</sub> = 192 kHz		105.6		
	Power dissipation, DV <sub>DD</sub> = 3.3 V <sup>(3)</sup>	f <sub>S</sub> = N/A (power-down mode)		2.3	4	mW

## ELECTRICAL CHARACTERISTICS

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$ ,  $f_S = 48\text{ kHz}$ , system clock =  $512 f_S$ , and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		16	24	32	Bits
<b>Data Format (PCM Mode)</b>						
	Audio data interface format		I <sup>2</sup> S, left justified			
	Audio data bit length		16, 24, 32-bit acceptable			
	Audio data format		MSB-first, 2s complement			
$f_S$	Sampling frequency		8		384	kHz
	System clock frequency		64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, or 3072 $f_{SCK}$ , up to 50 Mhz			
<b>Digital Input/Output</b>						
Logic family: 3.3-V LVCMOS compatible						
$V_{IH}$	Input logic level		$0.7 \times DV_{DD}$			V
$V_{IL}$			$0.3 \times DV_{DD}$			
$I_{IH}$	Input logic current	$V_{IN} = V_{DD}$			10	$\mu\text{A}$
$I_{IL}$		$V_{IN} = 0\text{ V}$			-10	
$V_{OH}$	Output logic level	$I_{OH} = -4\text{ mA}$	$0.8 \times DV_{DD}$			V
$V_{OL}$		$I_{OL} = 4\text{ mA}$	$0.22 \times DV_{DD}$			
<b>Dynamic Performance (PCM Mode)<sup>(1)(2)</sup> (Values shown for three devices PCM5102/PCM5101/PCM5100)</b>						
	THD+N at -1 dBFS <sup>(2)</sup>	$f_S = 48\text{ kHz}$	-93/-92/-90	-83/-82/-80		dB
		$f_S = 96\text{ kHz}$	-93/-92/-90			
		$f_S = 192\text{ kHz}$	-93/-92/-90			
	Dynamic range <sup>(2)</sup>	EIAJ, A-weighted, $f_S = 48\text{ kHz}$	106/ 100/ 95	112/106/100		dB
		EIAJ, A-weighted, $f_S = 96\text{ kHz}$		112/106/100		
		EIAJ, A-weighted, $f_S = 192\text{ kHz}$		112/106/100		
	Signal-to-noise ratio <sup>(2)</sup>	EIAJ, A-weighted, $f_S = 48\text{ kHz}$		112/106/100		dB
		EIAJ, A-weighted, $f_S = 96\text{ kHz}$		112/106/100		
		EIAJ, A-weighted, $f_S = 192\text{ kHz}$		112/106/100		
	Signal-to-noise ratio with analog mute <sup>(2)(3)</sup>	EIAJ, A-weighted, $f_S = 48\text{ kHz}$	113	123		dB
		EIAJ, A-weighted, $f_S = 96\text{ kHz}$		123		
		EIAJ, A-weighted, $f_S = 192\text{ kHz}$		123		
	Channel separation	$f_S = 48\text{ kHz}$	100/ 95/ 90	109/103/97		dB
		$f_S = 96\text{ kHz}$		109/103/97		
		$f_S = 192\text{ kHz}$		109/103/97		
<b>Analog Output</b>						
	Output voltage			2.1		$V_{RMS}$
	Gain error		-6	$\pm 2$	6	% of FSR
	Gain mismatch, channel-to-channel		-6	$\pm 2$	6	% of FSR
	Bipolar-zero error	At bipolar zero	-5	$\pm 1$	5	mV
	Load impedance		1			k $\Omega$
<b>Filter Characteristics–1: Normal</b>						

(1) Filter condition: THD+N: 20-Hz HPF, 20-kHz AES17 LPF; dynamic range: 20-Hz HPF, 20-kHz AES17 LPF; A-weighted signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF; A-weighted channel separation: 20-Hz HPF, 20-kHz AES17 LPF; analog performance specifications are measured using the System Two Cascade™ audio measurement system by Audio Precision™ in the rms mode.

(2) Output load is 10 k $\Omega$ , with 470- $\Omega$  output resistor and a 2.2-nF shunt capacitor (see recommended output filter).

(3) Both L-ch and R-ch are BPZ when XSMT is de-asserted.

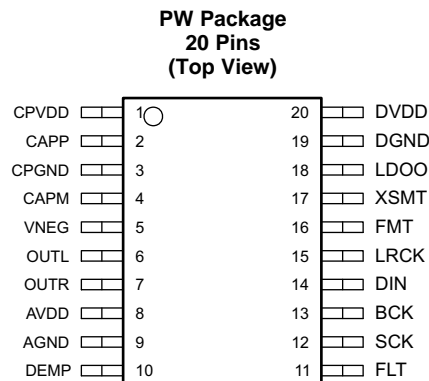
## ELECTRICAL CHARACTERISTICS (continued)

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$ ,  $f_S = 48\text{ kHz}$ , system clock =  $512 f_S$ , and 24-bit data unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass band				0.45 $f_S$	
Stop band		0.55 $f_S$			
Stop-band attenuation		-60			dB
Pass-band ripple				$\pm 0.02$	
Delay time			22 / $f_S$		s
<b>Filter Characteristics–2: Low Latency</b>					
Pass band				0.47 $f_S$	
Stop band		0.55 $f_S$			
Stop-band attenuation		-52			dB
Pass-band ripple				$\pm 0.0001$	
Delay time			3.5 / $f_S$		s

## DEVICE INFORMATION

### TERMINAL FUNCTIONS, PCM510x-Q1



**Table 2. PIN FUNCTIONS, PCM510x-Q1**

PIN		I/O	DESCRIPTION
NAME	NO.		
CPVDD	1	—	Charge-pump power supply, 3.3 V
CAPP	2	O	Charge-pump flying-capacitor terminal for positive rail
CPGND	3	—	Charge-pump ground
CAPM	4	O	Charge-pump flying-capacitor terminal for negative rail
VNEG	5	O	Negative charge-pump rail terminal for decoupling, -3.3 V
OUTL	6	O	Analog output from DAC left channel
OUTR	7	O	Analog output from DAC right channel
AVDD	8	—	Analog power supply, 3.3 V
AGND	9	—	Analog ground
DEMP	10	I	De-emphasis control for 44.1-kHz sampling rate <sup>(1)</sup> : Off (Low), On (High)
FLT	11	I	Filter select : Normal latency (Low) / Low latency (High)
SCK	12	I	System clock input <sup>(1)</sup>
BCK	13	I	Audio-data bit-clock input <sup>(1)</sup>

(1) Failsafe LVCMOS Schmitt trigger input

**Table 2. PIN FUNCTIONS, PCM510x-Q1 (continued)**

PIN		I/O	DESCRIPTION
NAME	NO.		
DIN	14	I	Audio-data input <sup>(1)</sup>
LRCK	15	I	Audio-data word-clock input <sup>(1)</sup>
FMT	16	I	Audio format selection : I <sup>2</sup> S (Low) / Left-justified (High)
XSMT	17	I	Soft-mute control <sup>(1)</sup> : Soft mute (Low), Soft un-mute (High)
LDOO	18	—	Internal-logic supply-rail terminal for decoupling
DGND	19	—	Digital ground
DVDD	20	—	Digital power supply, 3.3 V

### TYPICAL CHARACTERISTICS

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$ ,  $f_s = 48\text{ kHz}$ , system clock =  $512 f_s$ , and 24-bit data unless otherwise noted.

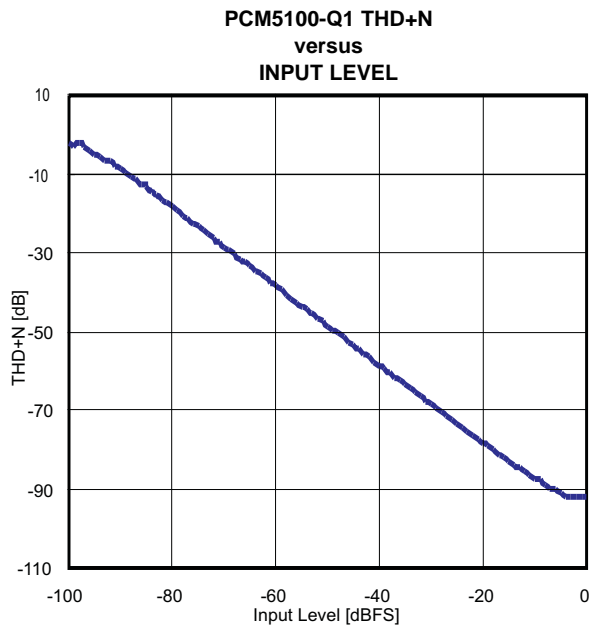


Figure 2.

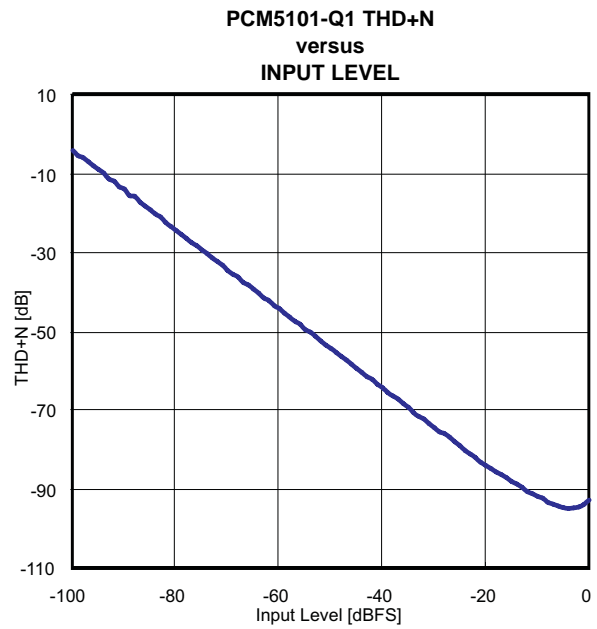


Figure 3.

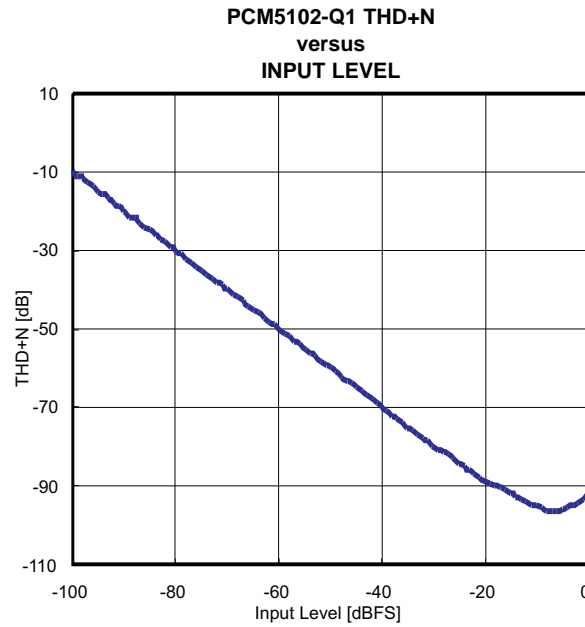


Figure 4.



### TYPICAL CHARACTERISTICS (continued)

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$ ,  $f_S = 48\text{ kHz}$ , system clock =  $512 f_S$ , and 24-bit data unless otherwise noted.

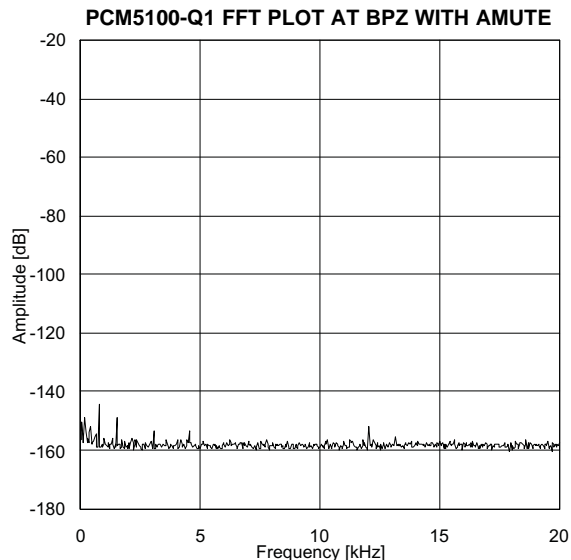


Figure 5.

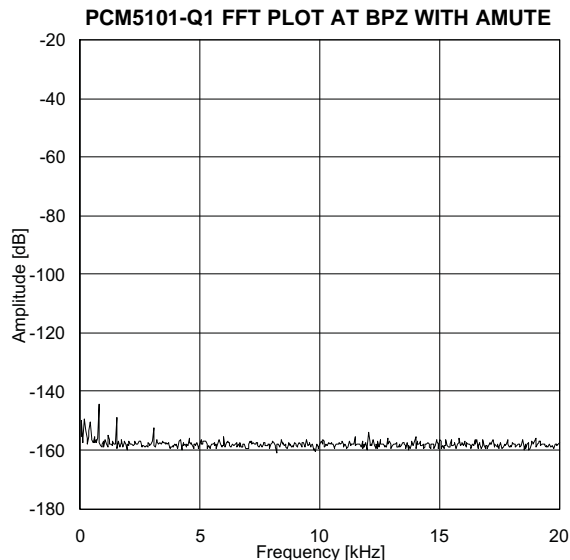


Figure 6.

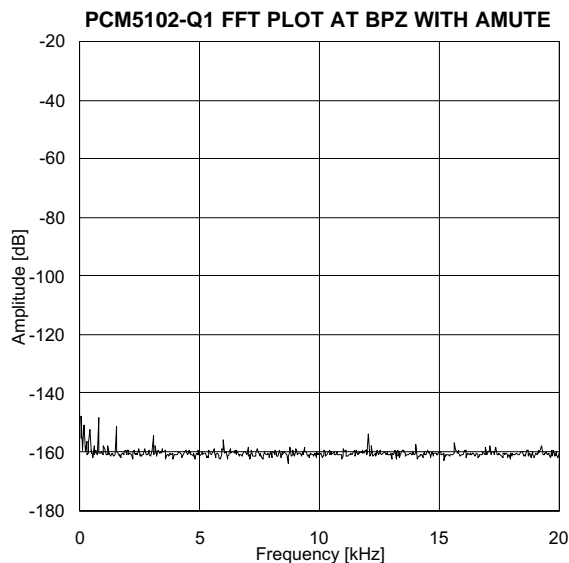
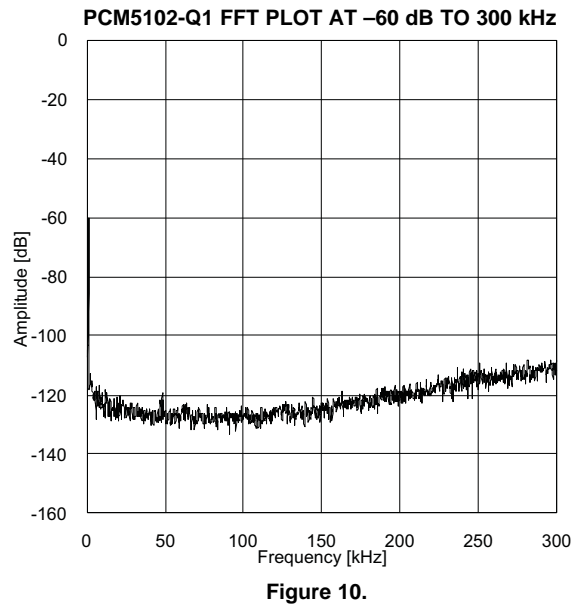
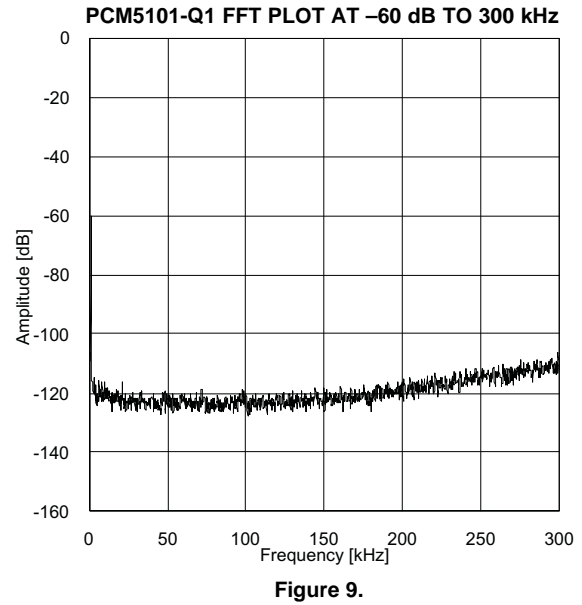
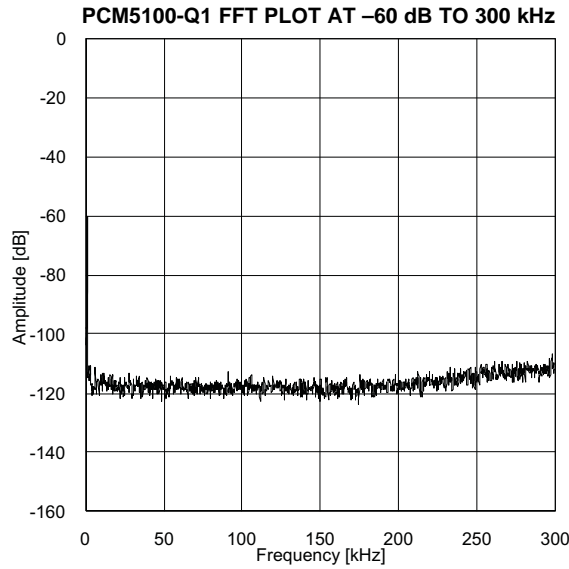


Figure 7.

### TYPICAL CHARACTERISTICS (continued)

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$ ,  $f_S = 48\text{ kHz}$ , system clock =  $512 f_S$ , and 24-bit data unless otherwise noted.



## APPLICATION INFORMATION

### Reset and System Clock Functions

#### Power-On Reset Function

The PCM510x-Q1 includes a power-on-reset function shown in [Figure 11](#). Having  $V_{DD} > 2.8$  V enables the power-on reset function. After the initialization period, the PCM510x-Q1 enters its default reset state.

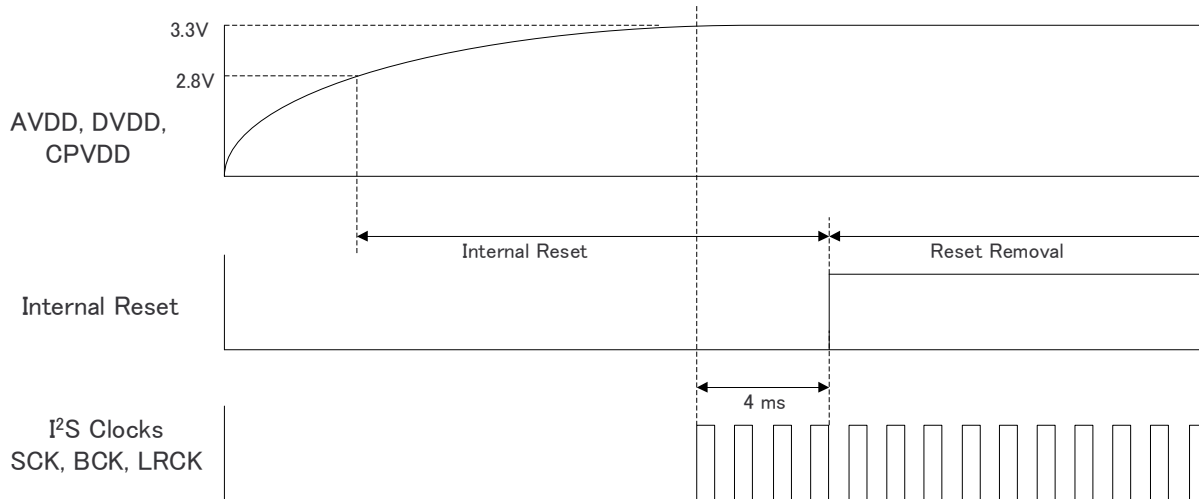


Figure 11. Power-On Reset Timing, DVDD = 3.3V

## System-Clock Input

The PCM510x-Q1 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock, applied at the SCK input (pin 12), supports up to 50 MHz. The PCM510x-Q1 has a system-clock detection circuit that automatically senses the system-clock frequency. Common audio sampling frequencies of 8 kHz, 16 kHz, 32 kHz–44.1 kHz and 48 kHz, 88.2 kHz–96 kHz, 176.4 kHz–192 kHz, and 384 kHz with  $\pm 4\%$  tolerance are supported. The sampling-frequency detector sets the clock for the digital filter, delta-sigma modulator (DSM) and the negative charge pump (NCP) automatically. Table 3 shows examples of system clock frequencies for common audio sampling rates.

### NOTE

The sampling frequency detector only detects six sampling frequency options. Any sampling frequency between the range of 32 kHz–44.1 kHz (or if it is 48 kHz) is detected as one option. The same case applies for the range from 88.2 kHz–96 kHz and 176.4 kHz–192 kHz.

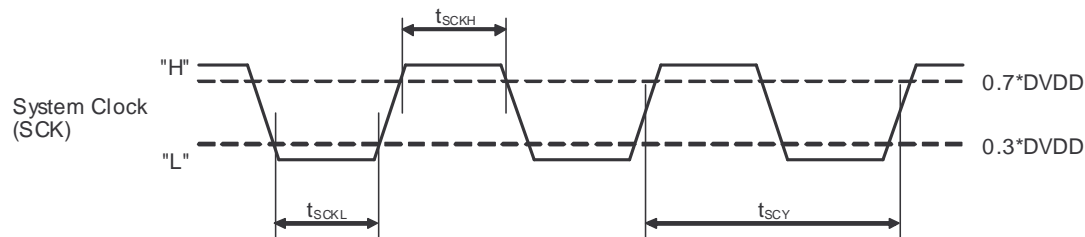
The device supports SCK rates between 1 MHz and 50 MHz that are not common to standard audio clocks by configuring various PLL and clock-divider registers. This allows the device to become a clock master and drive the host serial port with LRCK and BCK, from a non-audio related clock (for example, using 12 MHz to generate 44.1 kHz (LRCK) and 2.8224 MHz (BCK)).

Figure 12 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise.

**Table 3. System Master Clock Inputs for Audio-Related Clocks**

Sampling Frequency	System Clock Frequency ( $f_{SCK}$ ) (MHz)											
	64 $f_S$	128 $f_S$	192 $f_S$	256 $f_S$	384 $f_S$	512 $f_S$	768 $f_S$	1024 $f_S$	1152 $f_S$	1536 $f_S$	2048 $f_S$	3072 $f_S$
8 kHz	– <sup>(1)</sup>	1.0240 <sup>(2)</sup>	1.5360 <sup>(2)</sup>	2.0480	3.0720	4.0960	6.1440	8.1920	9.2160	12.2880	16.3840	24.5760
16 kHz	– <sup>(1)</sup>	2.0480 <sup>(2)</sup>	3.0720 <sup>(2)</sup>	4.0960	6.1440	8.1920	12.2880	16.3840	18.4320	24.5760	36.8640	49.1520
32 kHz	– <sup>(1)</sup>	4.0960 <sup>(2)</sup>	6.1440 <sup>(2)</sup>	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	49.1520	– <sup>(1)</sup>	– <sup>(1)</sup>
44.1 kHz	– <sup>(1)</sup>	5.6488 <sup>(2)</sup>	8.4672 <sup>(2)</sup>	11.2896	16.9344	22.5792	33.8688	45.1584	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>
48 kHz	– <sup>(1)</sup>	6.1440 <sup>(2)</sup>	9.2160 <sup>(2)</sup>	12.2880	18.4320	24.5760	36.8640	49.1520	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>
88.2 kHz	– <sup>(1)</sup>	11.2896 <sup>(2)</sup>	16.9344	22.5792	33.8688	45.1584	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>
96 kHz	– <sup>(1)</sup>	12.2880 <sup>(2)</sup>	18.4320	24.5760	36.8640	49.1520	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>
176.4 kHz	– <sup>(1)</sup>	22.5792	33.8688	45.1584	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>
192 kHz	– <sup>(1)</sup>	24.5760	36.8640	49.1520	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>
384 kHz	24.5760	49.1520	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>

- (1) The device does not support this system clock rate for the given sampling frequency.  
 (2) PLL mode supports this system clock rate.



**Figure 12. Timing Requirements for SCK Input**

**Table 4. Timing Requirements for SCK Input**

	Parameters	Min	Max	Unit
$t_{SCY}$	System clock-pulse cycle time	20	1000	ns
$t_{SCKH}$	System clock-pulse duration, High	9		ns
$t_{SCKL}$	System clock-pulse duration, Low	9		ns

## System Clock PLL Mode

The system clock PLL mode allows designers to use a simple three-wire I<sup>2</sup>S audio source when driving the DAC, thereby reducing the need for a high-frequency SCK, making PCB layout easier, and reducing high-frequency electromagnetic interference.

The device starts up expecting an external SCK input, but if BCK and LRCK start correctly while SCK remains at ground level for 16 successive LRCK periods, then the internal PLL starts, automatically generating an internal SCK from the BCK reference. In the PCM510x-Q1, supplying an external SCK disables the internal PLL; the device requires specific BCK rates to generate an appropriate master clock. Table 5 describes the minimum and maximum BCK per LRCK for the integrated PLL to automatically generate an internal SCK.

**Table 5. BCK Rates (MHz) by LRCK Sample Rate for PCM510x-Q1 PLL Operation**

Sample f (kHz)	BCK (f <sub>s</sub> )	
	32	64
8	–	–
16	–	1.024
32	1.024	2.048
44.1	1.4112	2.8224
48	1.536	3.072
96	3.072	6.144
192	6.144	12.288
384	12.288	24.576

## Audio Data Interface

### Audio Serial Interface

The audio interface port is a 3-wire serial port. It includes LRCK (pin 15), BCK (pin 13), and DIN (pin 14). BCK is the serial audio bit clock, and it is used to clock the serial data present on DIN into the serial shift register of the audio interface. Serial data is clocked into the PCM510x-Q1 on the rising edge of BCK. LRCK is the serial audio left/right word clock.

**Table 6. PCM510x-Q1 Audio Data Formats, Bit Depths and Clock Rates**

CONTROL MODE	FORMAT	DATA BITS	MAX LRCK FREQUENCY [f <sub>s</sub> ]	SCK RATE [× f <sub>s</sub> ]	BCK RATE [× f <sub>s</sub> ]
Hardware control	I <sup>2</sup> S or LJ	32, 24, 20, 16	Up to 192 kHz	128–3072 (≤50 MHz)	64, 48, 32
			384 kHz	64, 128	64, 48, 32

The PCM510x-Q1 requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than ±5 SCK, the device initializes internal operation within one sample period and forces analog outputs to the bipolar-zero level until the completion of resynchronization between LRCK and the system clock.

If the relationship between LRCK and BCK is invalid for more than 4 LRCK periods, the device initializes internal operation within one sample period and forces analog outputs to the bipolar-zero level until the completion of resynchronization between LRCK and BCK.

## PCM Audio Data Formats and Timing

The PCM510x-Q1 supports industry-standard audio data formats, including standard I<sup>2</sup>S and left-justified. Data formats are selected using the FMT (pin 16), Low for I<sup>2</sup>S, and High for left-justified.

All formats require binary 2s complement, MSB-first audio data. Figure 13 shows a detailed timing diagram for the serial audio interface.

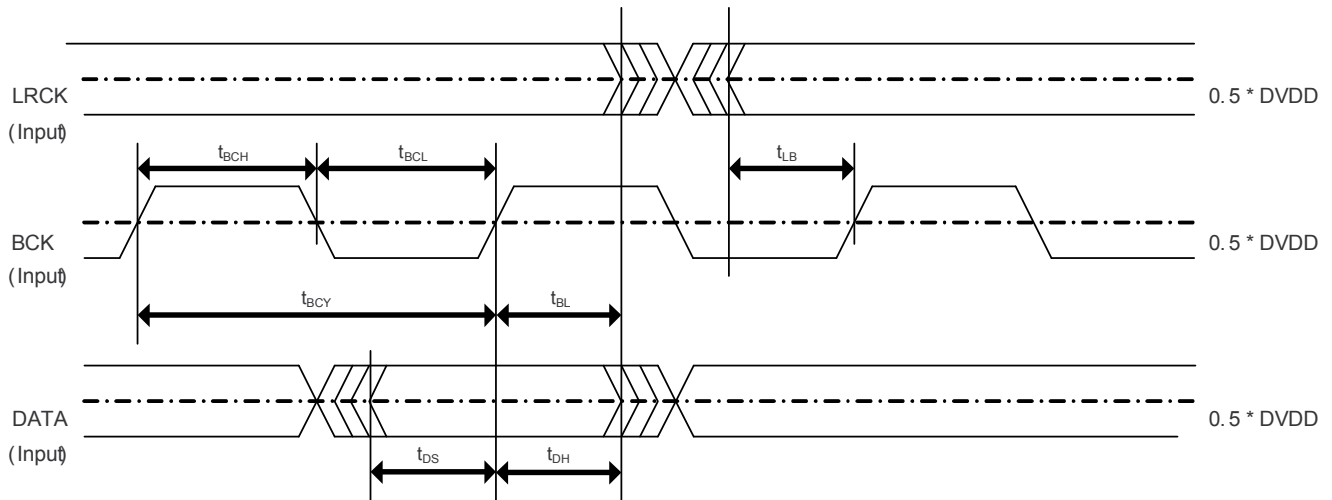


Figure 13. PCM510x-Q1 Serial Audio Timing - Slave

Table 7. Audio Interface Slave Timing

	Parameters	Min	Max	Unit
$t_{BCY}$	BCK pulse cycle time	40		ns
$t_{BCL}$	BCK pulse duration LOW	16		ns
$t_{BCH}$	BCK pulse duration HIGH	16		ns
$t_{BL}$	BCK rising edge to LRCK edge	8		ns
$t_{LB}$	LRCK edge to BCK rising edge	8		ns
$t_{DS}$	DATA setup time	8		ns
$t_{DH}$	DATA hold time	8		ns
$f_{BCK}$	BCK frequency at DVDD = 3.3 V		24.576	MHz

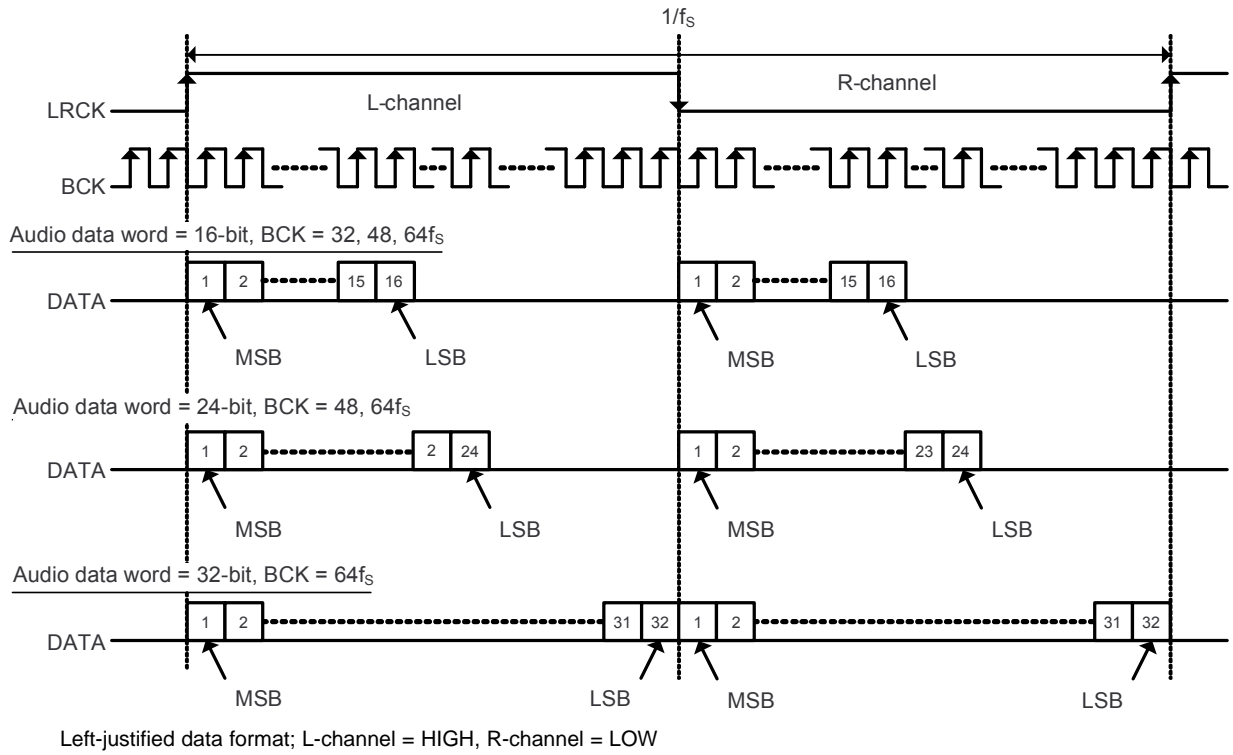


Figure 14. Left-Justified Audio Data Format

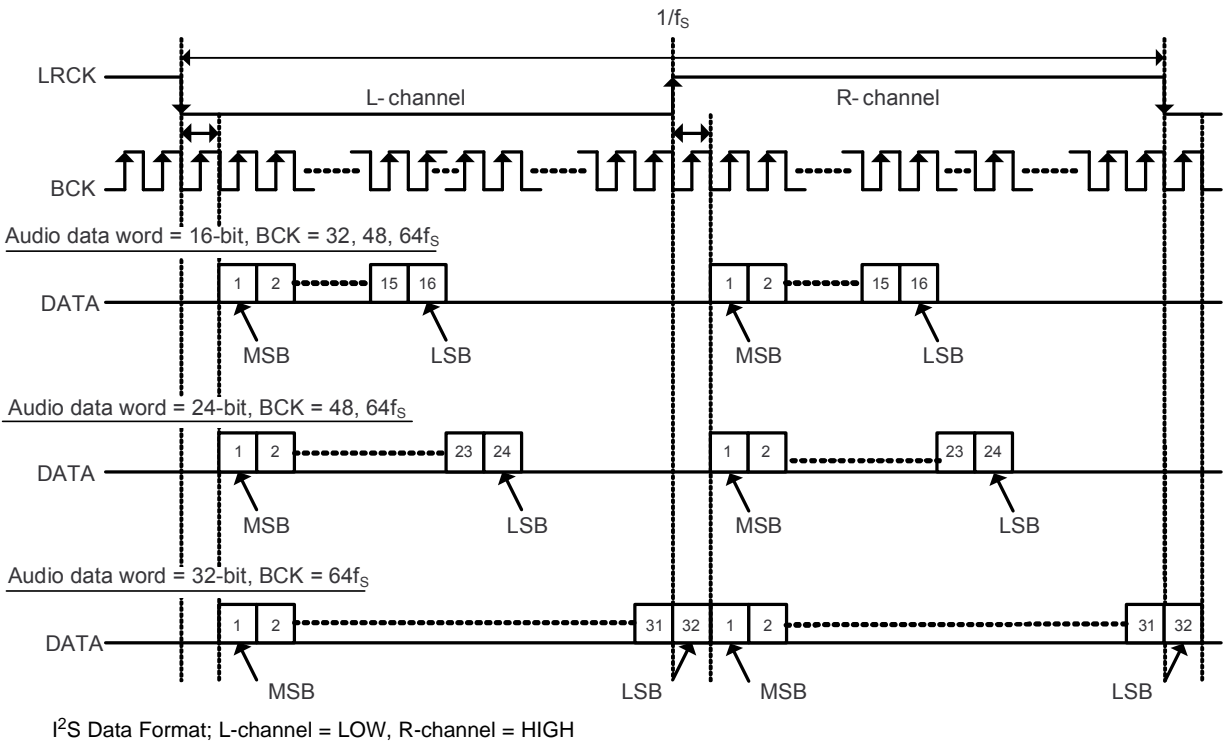


Figure 15. I<sup>2</sup>S Audio Data Format

## Function Descriptions

### Interpolation Filter

The PCM510x-Q1 provides two types of interpolation filter. Users can select which filter to use by using the FLT pin (pin11).

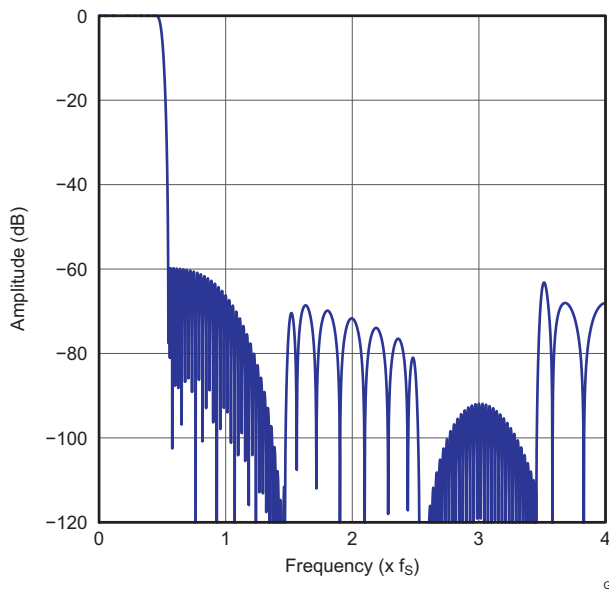
**Table 8. Digital Interpolation Filter Options**

FLT Pin	Description
0	FIR normal x8, x4, x2, and x1 interpolation filters
1	IIR low-latency x8, x4, x2, and x1 interpolation filters

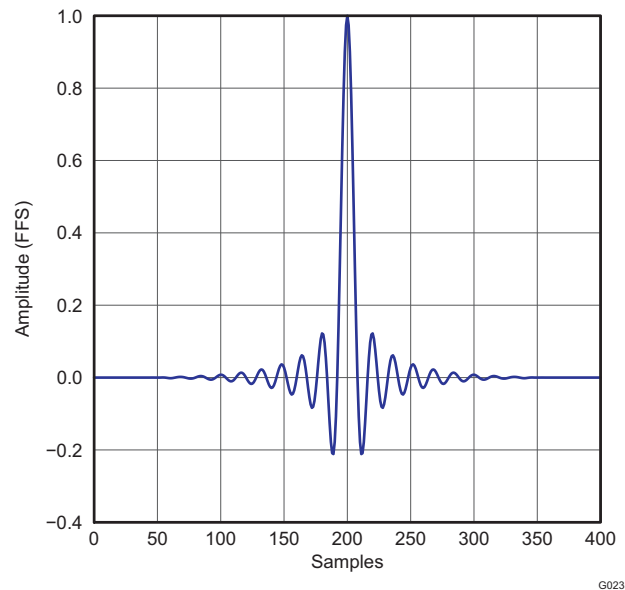
The normal x8, x4, x2, or x1 (bypass) interpolation filter is programmed in 256 cycles in 1 sampling frequency ( $f_s$ ) for from 8 kHz to 384 kHz.

**Table 9. Normal x8 Interpolation Filter**

Parameter	Condition	Value (Typ)	Value (Max)	Unit
Filter-gain pass band	$0-0.45 f_s$		$\pm 0.02$	dB
Filter-gain stop band	$0.55 f_s-7.455 f_s$	-60		dB
Filter-group delay		$22 / f_s$		s

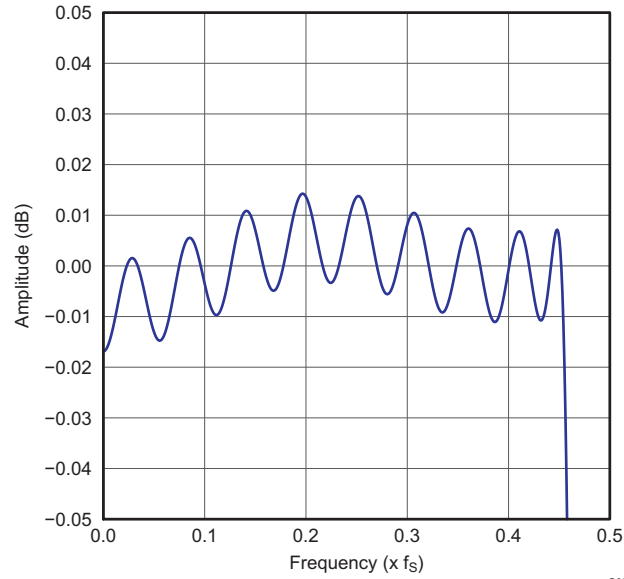


**Figure 16. Normal x8 Interpolation-Filter Frequency Response**



**Figure 17. Normal x8 Interpolation-Filter Impulse Response**



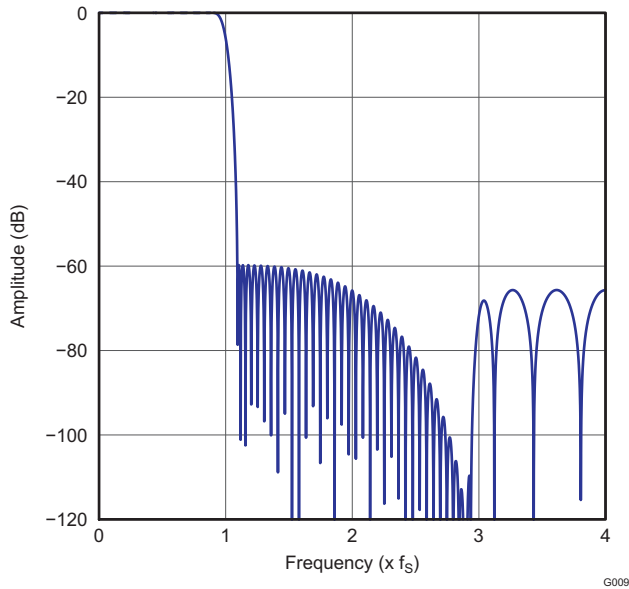


**Figure 18. Normal x8 Interpolation-Filter Pass-Band Ripple**

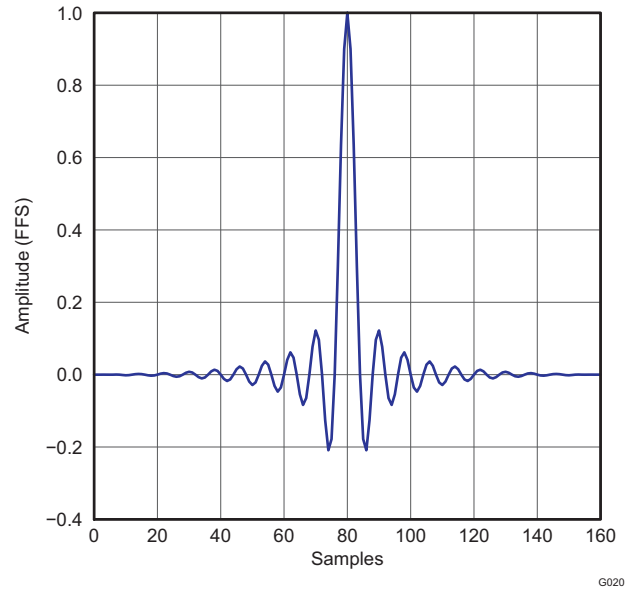
The normal  $\times 4$ ,  $\times 2$ , or  $\times 1$  (bypass) interpolation filter is programmed in 256 cycles in 1 sampling frequency ( $f_S$ ) for from 8 kHz to 384 kHz.

**Table 10. Normal  $\times 4$  Interpolation Filter**

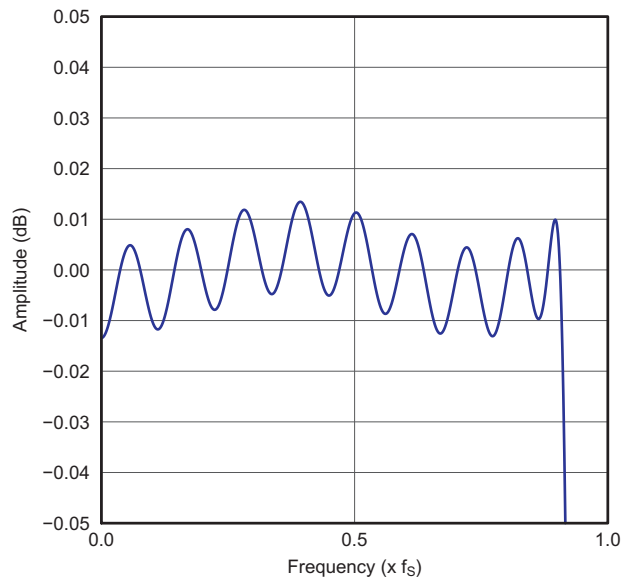
Parameter	Condition	Value (Typ)	Value (Max)	Unit
Filter-gain pass Band	$0-0.45 f_S$		$\pm 0.02$	dB
Filter-gain stop band	$0.55 f_S-7.455 f_S$	-60		dB
Filter-group delay		$22 / f_S$		s



**Figure 19. Normal  $\times 4$  Interpolation-Filter Frequency Response**



**Figure 20. Normal  $\times 4$  Interpolation-Filter Impulse Response**

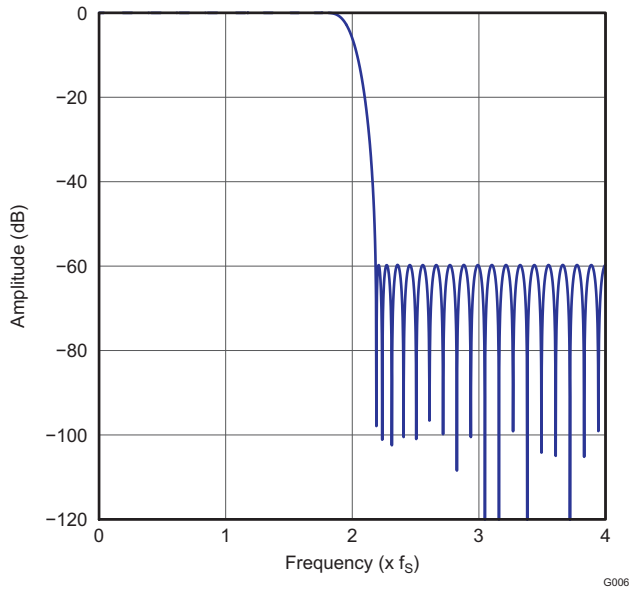


**Figure 21. Normal  $\times 4$  Interpolation-Filter Pass-Band Ripple**

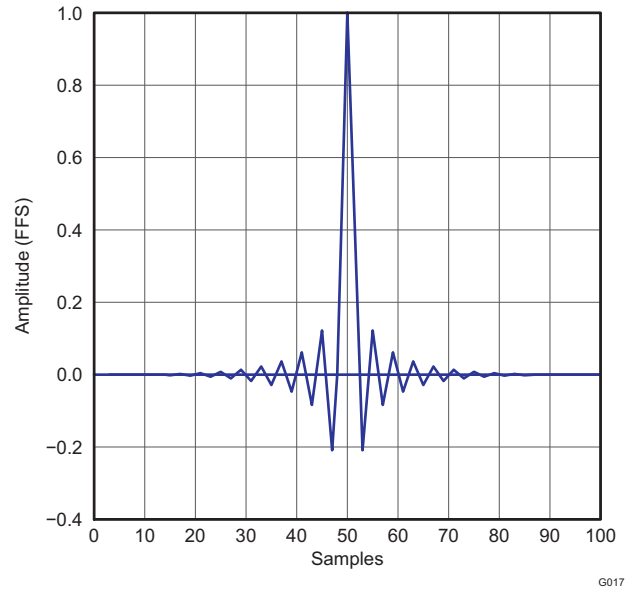
Normal  $\times 2$  or  $\times 1$  (bypass) interpolation filter is programmed in 256 cycles in 1 sampling frequency ( $f_s$ ) for from 8 kHz to 384 kHz.

**Table 11. Normal  $\times 2$  Interpolation Filter**

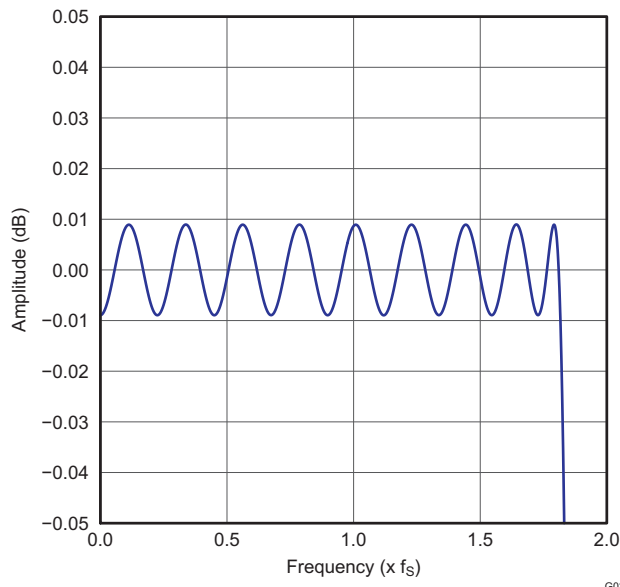
Parameter	Condition	Value (Typ)	Value (Max)	Unit
Filter-gain pass band	$0-0.45 f_s$		$\pm 0.02$	dB
Filter-gain stop band	$0.55 f_s-7.455 f_s$	-60		dB
Filter-group delay		$22 / f_s$		s



**Figure 22. Normal  $\times 2$  Interpolation-Filter Frequency Response**



**Figure 23. Normal  $\times 2$  Interpolation-Filter Impulse Response**

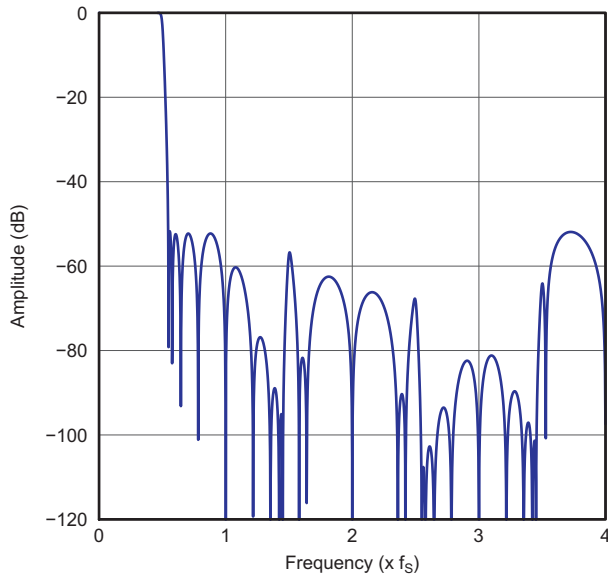


**Figure 24. Normal  $\times 2$  Interpolation-Filter Pass-Band Ripple**

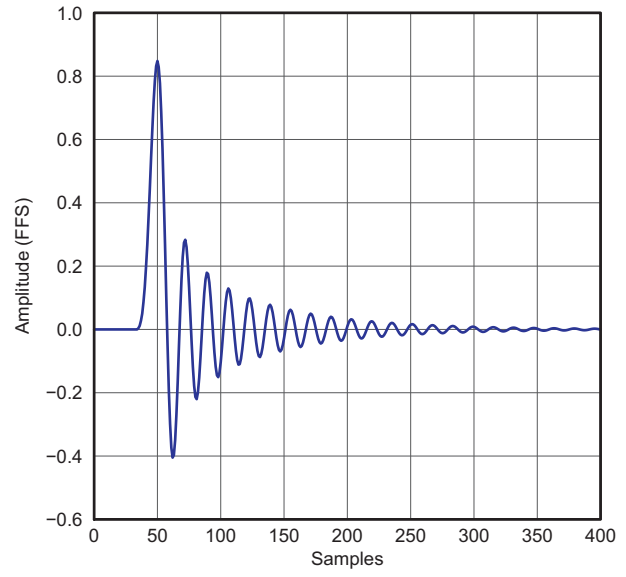
The low-latency  $\times 8$ ,  $\times 4$ ,  $\times 2$ , or  $\times 1$  (bypass) interpolation filter is programmed in 256 cycles in  $1 f_s$  for from 8 kHz to 384 kHz.

**Table 12. Low-Latency  $\times 8$  Interpolation Filter**

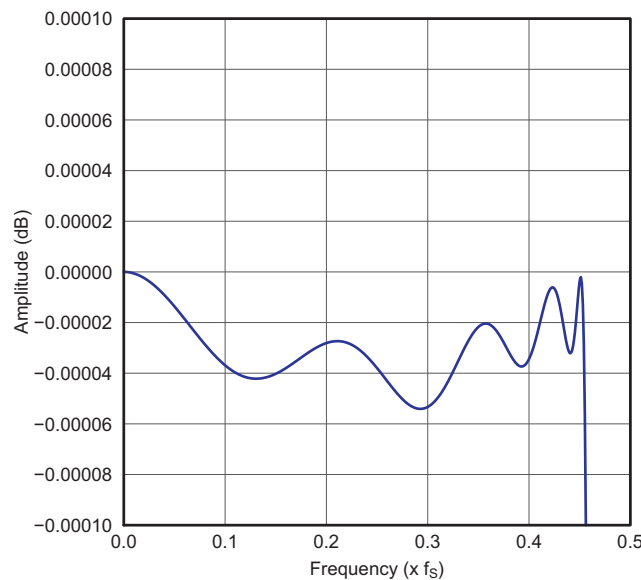
Parameter	Condition	Value (Typ)	Unit
Filter-gain pass band	$0-0.45 f_s$	$\pm 0.0001$	dB
Filter-gain stop band	$0.55 f_s-7.455 f_s$	-52	dB
Filter-group delay		$3.5 / f_s$	s



**Figure 25.  $\times 8$  Interpolation-Filter Frequency Response**



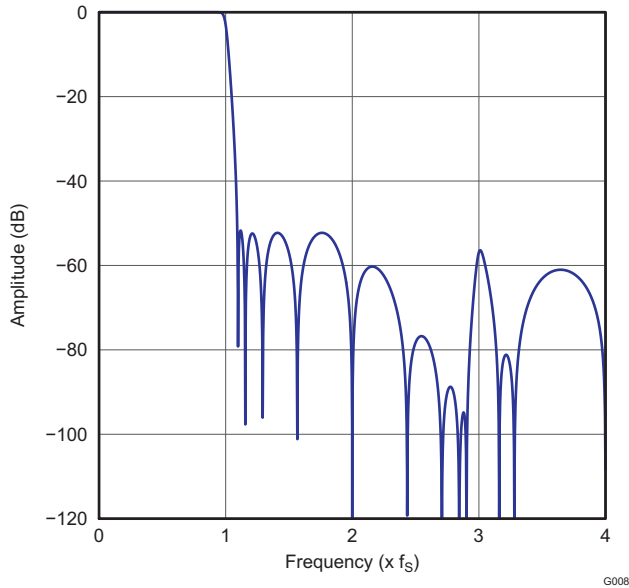
**Figure 26. Low-Latency  $\times 8$  Interpolation-Filter Impulse Response**



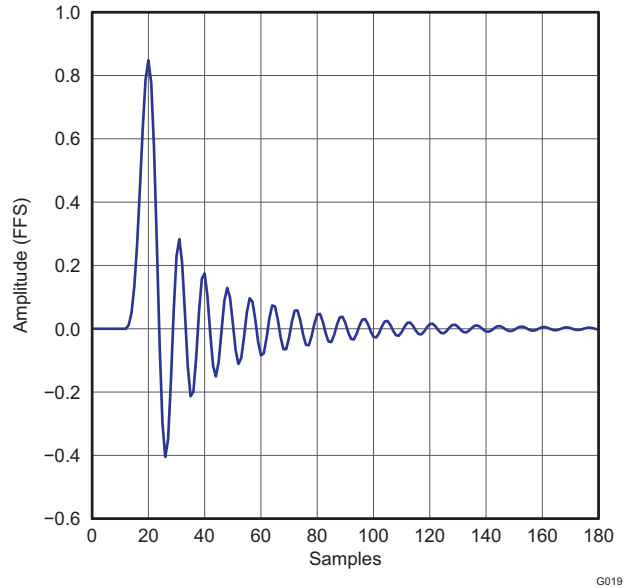
**Figure 27. Low-Latency  $\times 8$  Interpolation-Filter Pass-Band Ripple**

**Table 13. Low-Latency x4 Interpolation Filter**

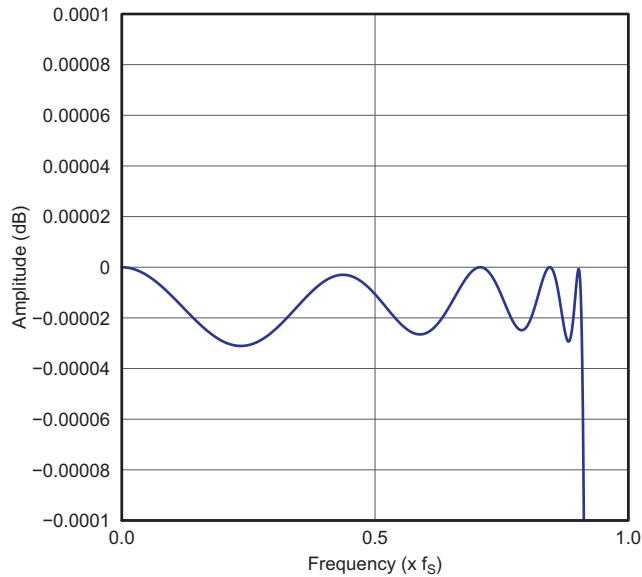
Parameter	Condition	Value (Typ)	Unit
Filter-gain pass band	$0-0.45 f_s$	$\pm 0.0001$	dB
Filter-gain stop band	$0.55 f_s-3.455 f_s$	-52	dB
Filter-group delay		$3.5 / f_s$	s



**Figure 28. Low-Latency x4 Interpolation-Filter Frequency Response**



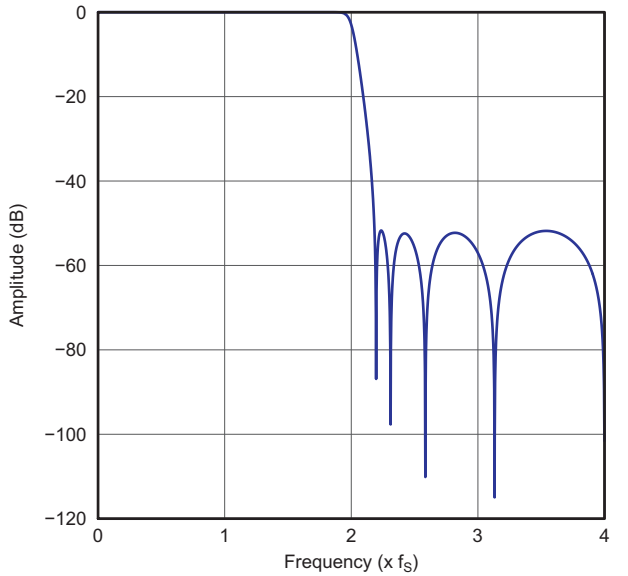
**Figure 29. Low-Latency x4 Interpolation-Filter Impulse Response**



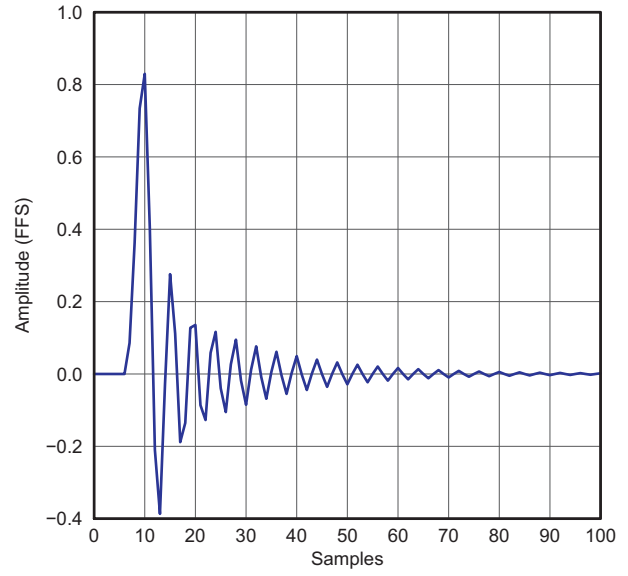
**Figure 30. Low latency x4 Interpolation-Filter Pass-Band Ripple**

**Table 14. Low-Latency  $\times 2$  Interpolation Filter**

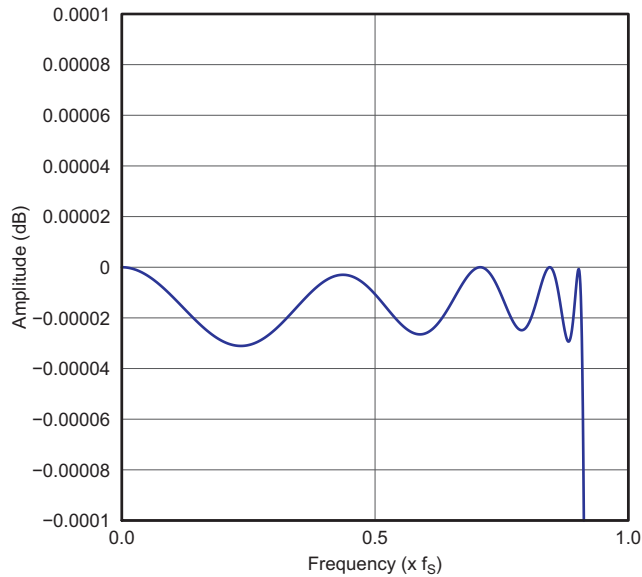
Parameter	Condition	Value (Typ)	Unit
Filter-gain pass band	$0-0.45 f_s$	$\pm 0.0001$	dB
Filter-gain stop band	$0.55 f_s-1.455 f_s$	-52	dB
Filter-group delay		$3.5 / f_s$	s



**Figure 31. Low-Latency  $\times 2$  Interpolation-Filter Frequency Response**



**Figure 32. Low-Latency  $\times 2$  Interpolation-Filter Impulse Response**



**Figure 33. Low-Latency  $\times 2$  Interpolation-Filter Pass-Band Ripple**

## Zero-Data Detect

The PCM510x-Q1 has a zero-data detect function. When the device detects continuous zero data, it enters a full analog-mute condition.

The PCM510x-Q1 counts zero data over 1024 LRCKs (21 ms at 48 kHz) before setting analog mute.

## Power-Save Mode

On detection of any kind of clock error (SCK, BCK, and LRCK) or clock halt, the PCM510x-Q1 enters standby mode automatically and powers down the current-segment DAC and line driver.

When BCK and LRCK halt to a low level for more than 1 second, the PCM510x-Q1 enters the power-down mode automatically. Power-down mode includes the negative charge pump and reference circuit power-down in addition to standby.

On application of expected audio clocks (SCK, BCK, LRCK) to the PCM510x-Q1, the device starts its power-up sequence automatically.

## XSMT Pin (Soft Mute and Soft Un-Mute)

For external digital control of the PCM510x-Q1, an external digital host must drive the XSMT pin with a specific minimum rise time ( $t_r$ ) and fall time ( $t_f$ ) for soft mute and soft un-mute. The PCM510x-Q1 requires  $t_r$  and  $t_f$  times of less than 20 ns. In the majority of applications, this should not be a problem; however, traces with high capacitance may have issues.

When shifting the XSMT pin from high to low (3.3 V to 0 V), a soft digital attenuation ramp starts.  $-1$ -dB gain occurs every  $1 / f_s$  from 0 dBFS to  $-\infty$ . This takes 104 sample periods.

When the XSMT pin is shifted from low to high (0 V to 3.3V), a soft digital un-mute starts. 1-dB gain steps occur every  $1 / f_s$  from  $-\infty$  to 0 dBFS. This takes 104 sample periods.

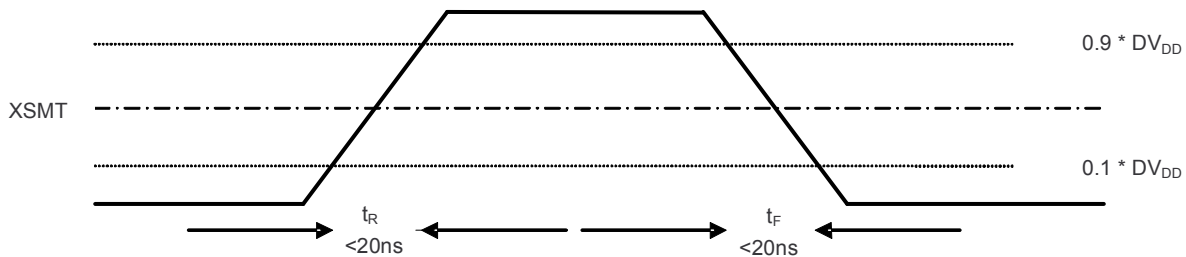


Figure 34. XSMT Timing for Soft Mute and Soft Un-Mute

Table 15. XSMT Timing Parameters

Parameters	Min	Max	Unit
Rise time ( $t_r$ )		20	ns
Fall time ( $t_f$ )		20	ns

## External Power Sense Undervoltage Protection mode

The XSMT pin can alternatively monitor a system voltage, such as the 24-VDC LCD TV backlight, or 12-VDC system supply, using a potential divider created with two resistors. (See [Figure 35](#) )

- If the XSMT pin makes a transition from 1 to 0 over 6 ms or more, the device switches into external undervoltage-protection mode. In this mode, two trigger levels are used.
- When the XSMT pin level reaches 2 V, the soft-mute process begins.
- When the XSMT pin level reaches 1.2 V, analog mute engages, regardless of digital audio level, and analog shutdown begins (for example, DAC circuitry powers down, and so forth).

A timing diagram to show this is shown in [Figure 36](#).

### NOTE

The XSMT input-pin voltage range is from  $-0.3\text{ V}$  to  $\text{DVDD} + 0.3\text{ V}$ . Consider the ratio of external resistors within this input range. Any increase in power supply (such as power-supply positive noise or ripple) can pull the XSMT pin higher than  $\text{DVDD} + 0.3\text{ V}$ .

For example, if the PCM510x-Q1 is monitoring a 12-V input and dividing the voltage by 4, then the voltage at XSMT during ideal power supply conditions is 3 V. If the voltage spikes any higher than 14.4 V, then the voltage on XSMT exceeds 3.6 V ( $\text{DVDD} + 0.3$ ), potentially damaging the device.

Appropriate setting of the divider allows monitoring of any dc voltage.

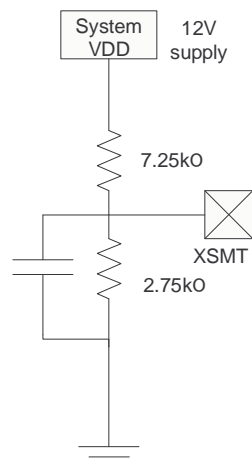


Figure 35. XSMT in External UVP Mode

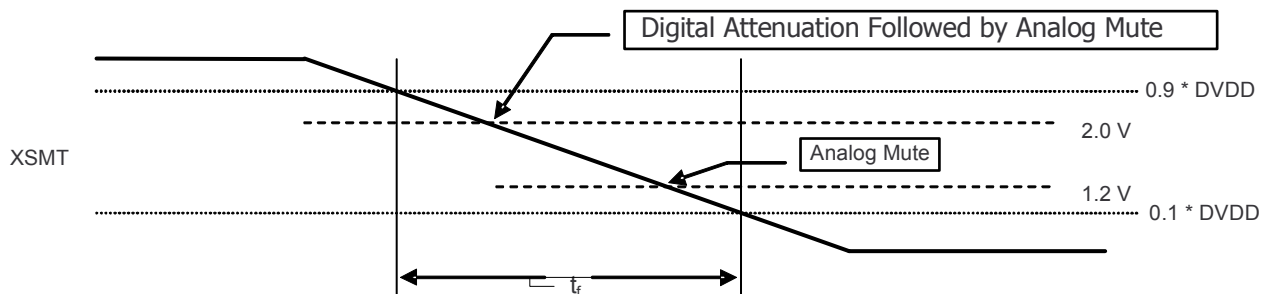


Figure 36. XSMT Timing for Undervoltage Protection



Typical Application Circuits

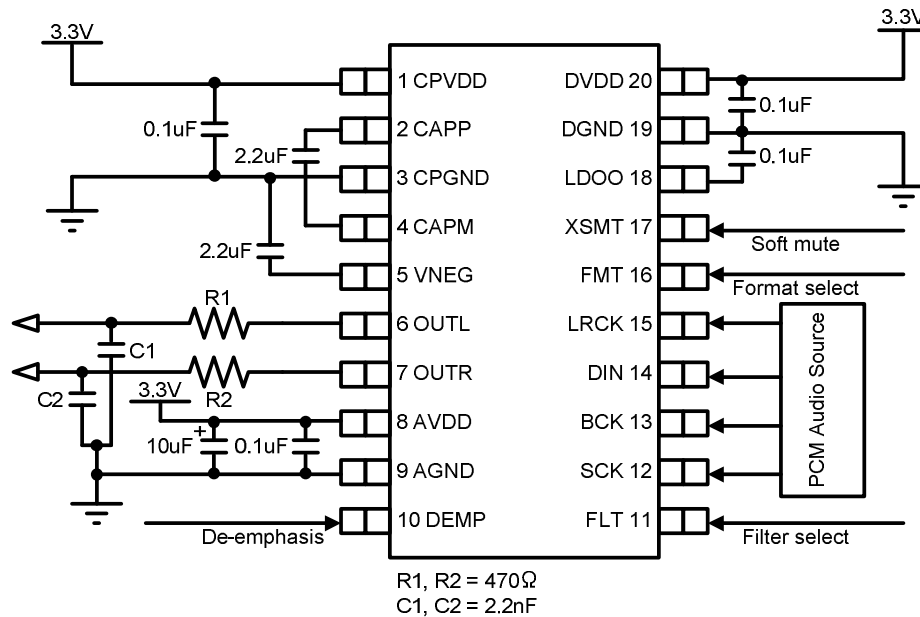


Figure 37. PCM510x-Q1 Standard PCM Audio Operation, 3.3 V

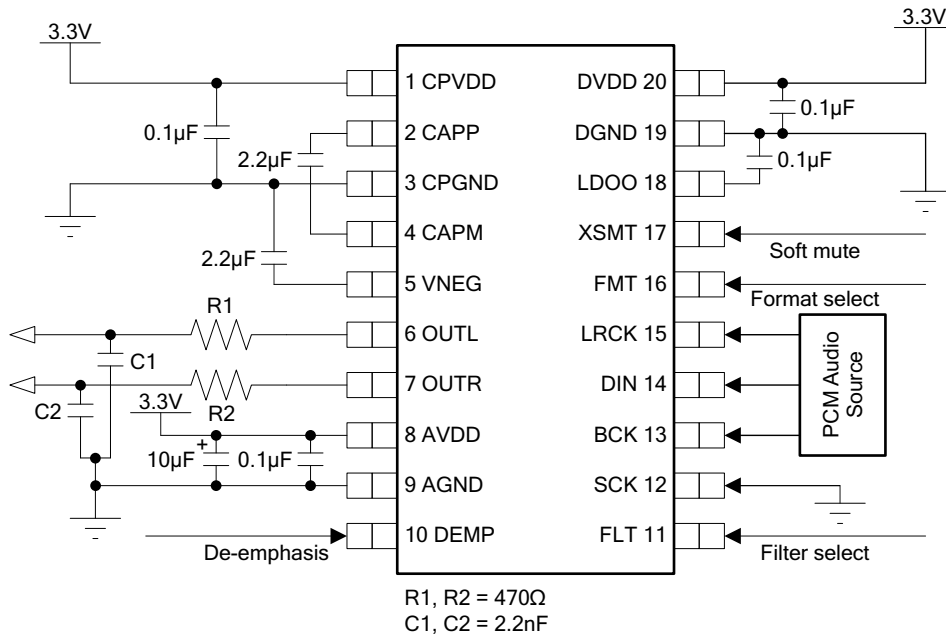
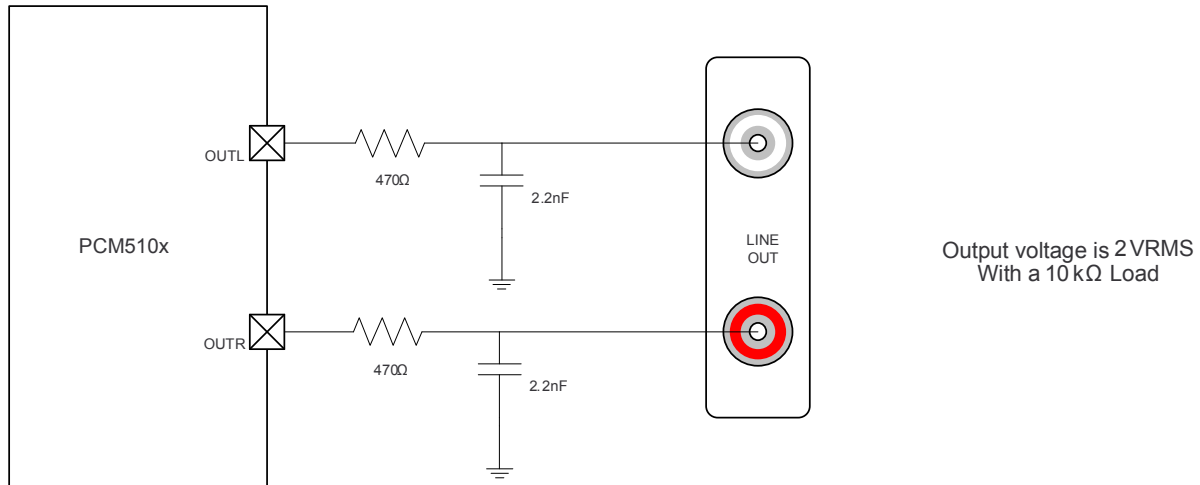


Figure 38. PCM510x-Q1 PLL Operation

### Recommended Output Filter for the PCM510x-Q1

The diagram in [Figure 39](#) shows the recommended output filter for the PCM510x-Q1. The new PCM510x-Q1 next-generation current-segment architecture offers excellent out-of-band noise, making a traditional 20-kHz low-pass filter a thing of the past.

The RC settings below offer a  $-3$ -dB filter point at 153 kHz (approximately), giving the DAC the ability to reproduce virtually all frequencies through to its maximum sampling rate of 384 kHz.



**Figure 39. Recommended Low-Pass Output Filter for 10-kΩ Operation**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
PCM5102TPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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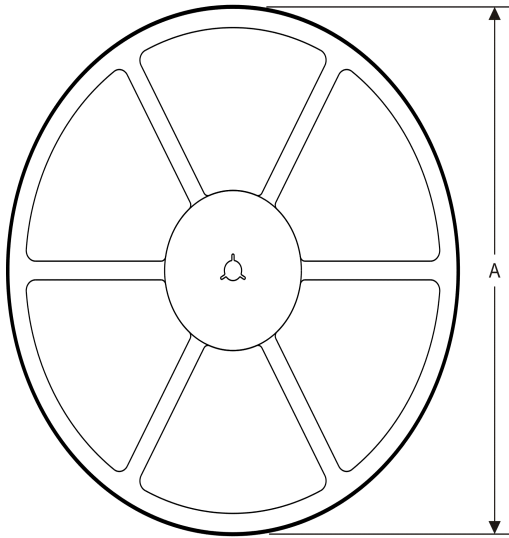
- Catalog: [PCM5102](#)

NOTE: Qualified Version Definitions:

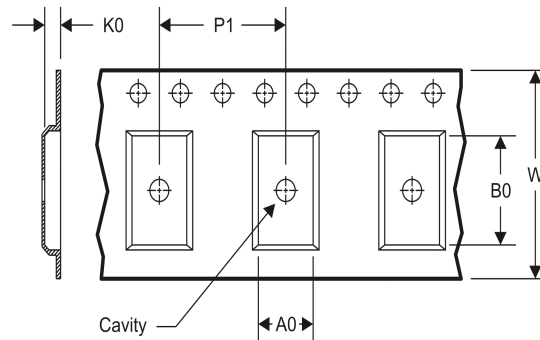
- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM5102TPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



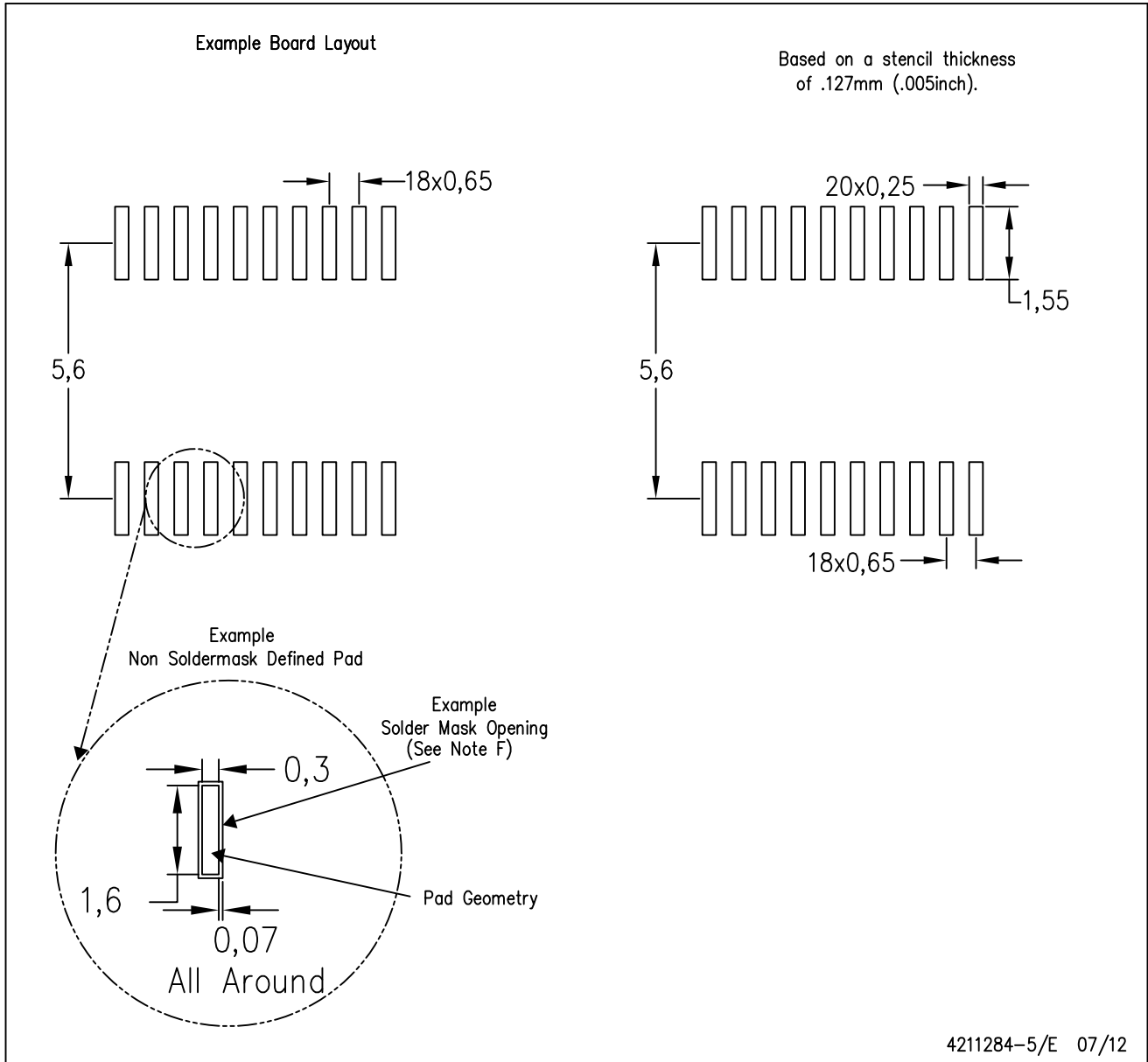
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM5102TPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
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