DATA SHEET

PCF84C21A; PCF84C41A; PCF84C81A

Telecom microcontrollers

Product specification
Supersedes data of 1995 Jul 14
File under Integrated Circuits, IC14

1996 Nov 20

Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Manufactured in silicon gate CMOS process
- 8-bit CPU, ROM, RAM, I/O in a 28-lead package
- 2 kbyte ROM, 64 byte RAM (PCF84C21A)
- 4 kbyte ROM, 128 byte RAM (PCF84C41A)
- 8 kbyte ROM, 256 byte RAM (PCF84C81A)
- I^2C-bus interface with multi-master capability
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O Port lines
- High sink current capability on the 8 lines of Port 1
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts:
  - external
  - 8-bit programmable timer/event counter 1
  - I^2C-bus
- Two test inputs, one of which also serves as the external interrupt input
- Stop and Idle modes
- Supply voltage: 2.5 to 5.5 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: –40 to +85 °C.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C21A, PCF84C41A and PCF84C81A. The shared properties of the PCF84CxxxA family of microcontrollers are described in the *"PCF84CxxxA family"* data sheet which should be read in conjunction with this publication.

The PCF84C21A, PCF84C41A and PCF84C81A are general purpose CMOS microcontrollers with 2 kbytes, 4 kbytes and 8 kbytes of program memory and 64,128 and 256 bytes of RAM, respectively. In addition to 20 I/O port lines, the microcontrollers provide an on-chip I^2C-bus interface. This two-line serial bus extends the microcontroller capabilities when implemented with the powerful I^2C-bus peripherals. These include LCD drivers, I/O expanders, telecom circuits, ADC and DAC converters, clock/calendar circuits, EEPROM and RAM and are listed in *"Data Handbook IC12, I^2C Peripherals".*

The instruction set is based on that of the MAB8048 and is a sub-set of that listed in the *"PCF84CxxxA family"* data sheet.

3 ORDERING INFORMATION (see note 1)

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF84C21AP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCF84C41AP			
PCF84C81AP			
PCF84C21AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCF84C41AT			
PCF84C81AT			

Note

1. Please refer to the Order Entry Form (OEF) for these devices for the full type number to use when ordering. This type number will also specify the required program and the ROM mask options.

4 BLOCK DIAGRAM

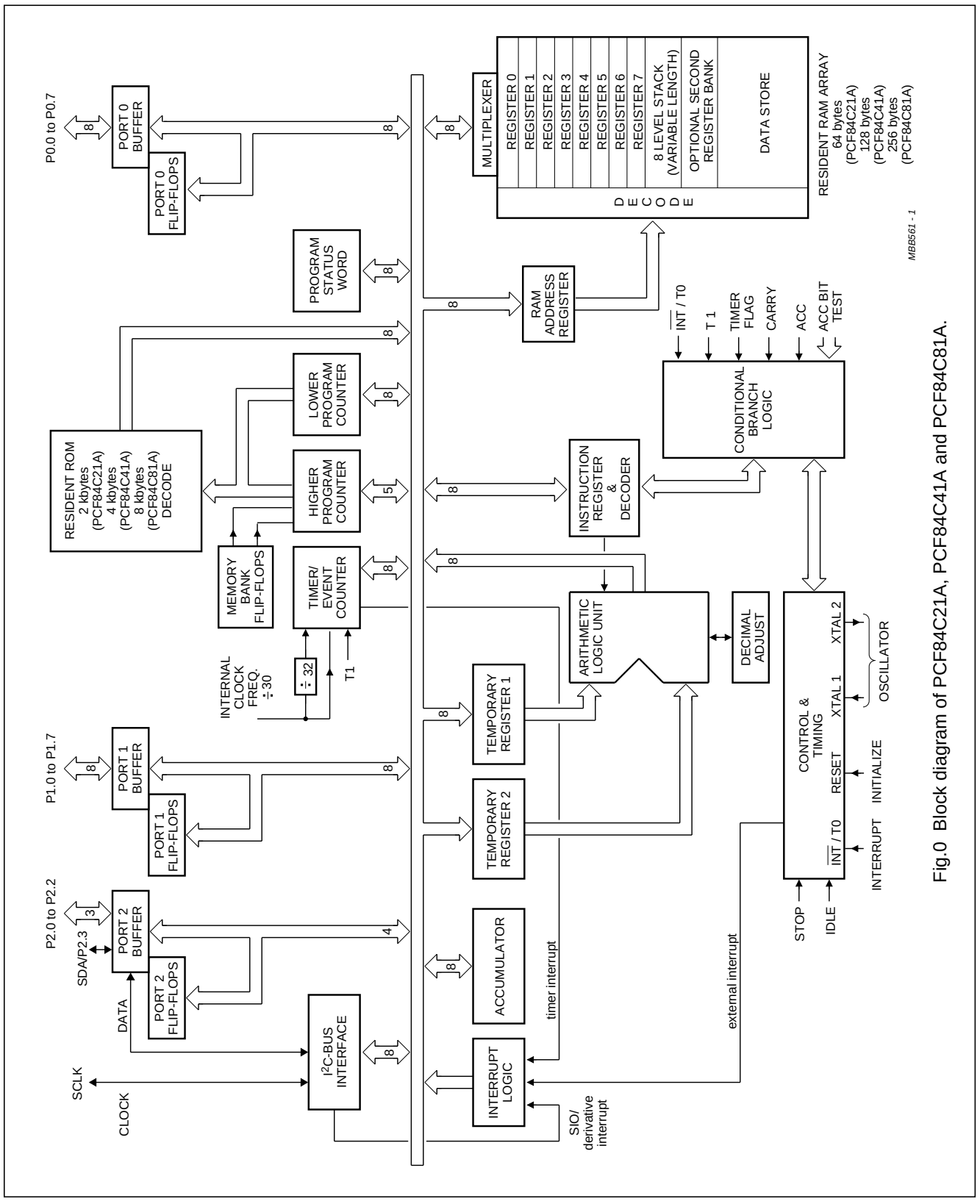


Fig.0 Block diagram of PCF84C21A, PCF84C41A and PCF84C81A.

5 PINNING INFORMATION

5.1 Pinning

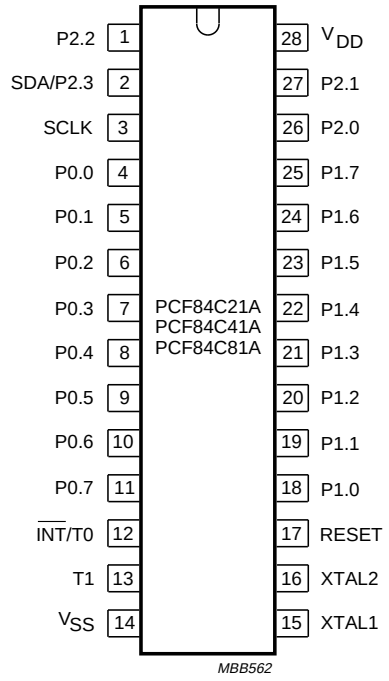


Fig.2 Pin configuration.

5.2 Pin description

Table 1 DIP28 and SO28 packages

SYMBOL	PIN	FUNCTION
P2.2	1	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
SDA/P2.3	2	bidirectional data line of the I^2C-bus interface, or 1 bit of Port 2: 4-bit quasi-bidirectional I/O port
SCLK	3	bidirectional clock line of the I^2C-bus interface
P0.0 to P0.7	4 to 11	8 bits of Port 0: 8-bit quasi-bidirectional I/O port
$\overline{INT}$/T0	12	Interrupt/Test 0
T1	13	Test 1/count input of 8-bit timer/event counter 1
V_{SS}	14	ground
XTAL1	15	crystal oscillator input or external clock input
XTAL2	16	crystal oscillator output
RESET	17	Reset input
P1.0 to P1.7	18 to 25	8 bits of Port 1: 8-bit quasi-bidirectional I/O port
P2.0 to P2.1	26 to 27	2 bits of Port 2: 4-bit quasi-bidirectional I/O port
V_{DD}	28	positive supply

6 INSTRUCTION SET

ROM is restricted to 2 kbytes for the PCF84C21A and 4 kbytes for the PCF84C41A. Therefore, the instructions SEL MB1/2/3 for the PCF84C21A, and the instructions SEL MB2/3 for the PCF84C41A should be avoided, as they would define non-existing program memory banks.

As RAM is limited to 64 bytes for the PCF84C21A and to 128 bytes for the PCF84C41A, care should be taken to avoid accesses to non-existing RAM locations.

See the "*PCF84CxxxA family*" data sheet for a complete description of the instruction set.

7 HIGH SINK OUTPUT CURRENTS

The Port 1 outputs of these devices are designed for high current drive in the logic 0 state. They are capable of driving 10 mA loads and higher. Applications include drive for small relays and light-emitting diodes (LEDs).

To avoid overload, care should be taken that the total Port 1 current averages less than 80 mA, i.e. an average of 10 mA per Port 1 line. Refer to Chapter "Limiting values" which specifies an upper limit of 100 mA for I_{SS}.

8 ROM MASK OPTIONS

ROM CODE	OPTION		
Program/data	Any mix of instructions and data up to ROM size of 2 kbytes for the PCF84C21A, 4 kbytes for the PCF84C41A and 8 kbytes for the PCF84C81A.		
Port Output			
P0.0 to P0.7	standard	open-drain	push-pull
P1.0 to P1.7	standard	open-drain	push-pull
P2.0 to P2.2	standard	open-drain	push-pull
SDA/P2.3	–	open-drain	–
Port State after reset			
P0.0 to P0.7	set	reset	–
P1.0 to P1.7	set	reset	–
P2.0 to P2.2	set	reset	–
SDA/P2.3	set	–	–
Oscillator			
Transconductance	LOW (g_{mL})	MEDIUM (g_{mM})	HIGH (g_{mH})

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices. See *"Data Handbook IC14, Section: Handling MOS devices"*.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+7	V
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current except Port 1 output LOW	–10	+10	mA
I_O	DC output current, Port 1 output LOW	–10	+20	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{DD}	supply current	–50	+50	mA
I_{SS}	ground supply current	–100	+50	mA
T_{stg}	storage temperature range	–55	+150	°C
T_j	operating junction temperature	–	90	°C

11 DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage	see Fig.3	2.5	–	5.5	V
I_{DD}	operating supply current	note 1; see Figs 4 and 5				
		V_{DD} = 3 V; f_{xtal} = 3.58 MHz (g_{mL})	–	0.3	0.6	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	–	1.1	3.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	–	1.7	5.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	–	2.5	6.0	mA
$I_{DD(idle)}$	supply current (Idle mode)	note 1; see Figs 6 and 7				
		V_{DD} = 3 V; f_{xtal} = 3.58 MHz (g_{mL})	–	0.2	0.4	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	–	0.8	1.6	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	–	1.2	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	–	1.7	5.0	mA
$I_{DD(stp)}$	supply current (Stop mode)	V_{DD} = 2.5 V; notes 1 and 2; see Fig.8	–	1.2	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	µA
Outputs						
I_{OL}	LOW level output sink current [except Port 1; SDA/P2.3 and SCLK]	V_{DD} = 5 V; V_O = 0.4 V; see Fig.9				
		PCF84C21A; PCF84C41A	1.6	12	–	mA
		PCF84C81A	1.6	5	–	mA
I_{OL1}	LOW level output sink current; Port 1	V_{DD} = 5 V; V_O = 1.2 V; see Fig.10				
		PCF84C21A; PCF84C41A	10	30	–	mA
		PCF84C81A	10	19	–	mA
I_{OL2}	LOW level output sink current; SDA/P2.3 and SCLK	V_{DD} = 5 V; V_O = 0.4 V; see Fig.11				
		PCF84C21A; PCF84C41A	3	12	–	mA
		PCF84C81A	3	6.5	–	mA
I_{OH}	HIGH level pull-up output source current	V_{DD} = 5 V; V_O = 3.5 V; see Fig.12	40	100	–	µA
		V_{DD} = 5 V; V_O = 0 V; see Fig.12	–	–140	–400	µA
I_{OH1}	HIGH level push-pull output source current	V_{DD} = 5 V; V_O = 4.6 V; see Fig.13	–1.6	–7	–	mA
Oscillator (see Fig.14)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance	V_{DD} = 5 V	0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance	V_{DD} = 5 V	3.0	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

Notes

1. V_{IL} = V_{SS}; V_{IH} = V_{DD}; open drain outputs connected to V_{SS}; all other outputs, including XTAL2, open (typical values at 25 °C with crystal connected between XTAL1 and XTAL2).
2. V_{IL} = V_{SS}; V_{IH} = V_{DD}; RESET and T1 at V_{SS}; $\overline{INT}$/T0 at V_{DD}; crystal connected between XTAL1 and XTAL2; open drain outputs connected to V_{SS}; all other outputs open.

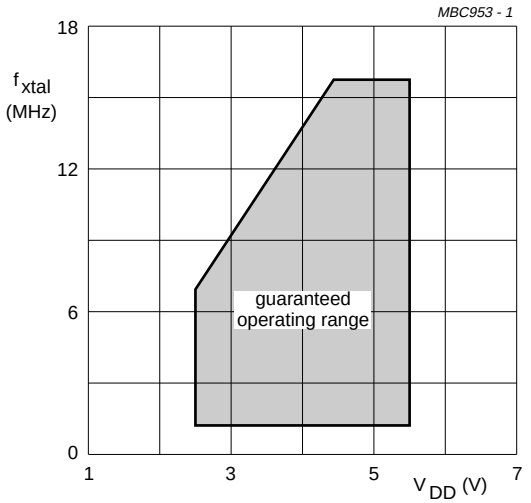
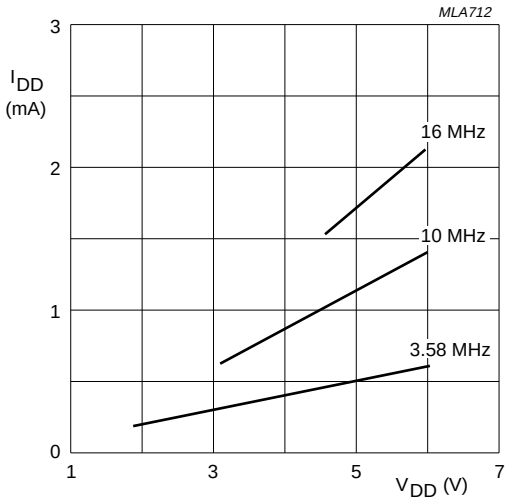
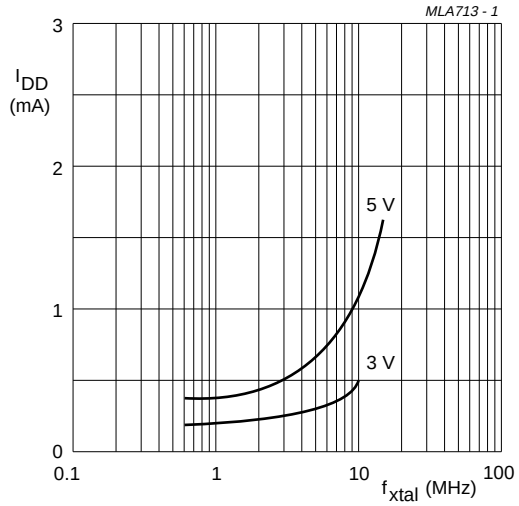


Fig.3 Maximum clock frequency as a function of operating supply voltage (V_{DD}).



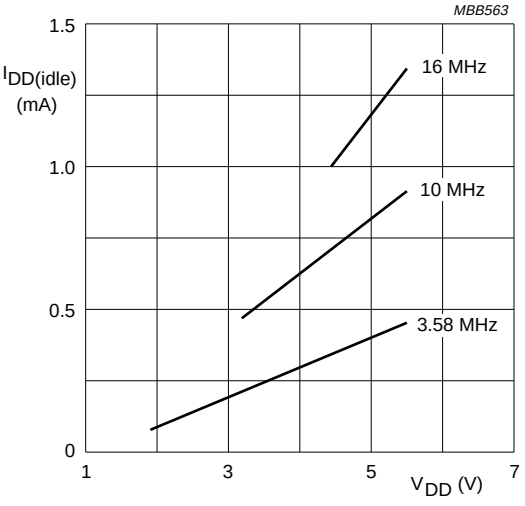
Supply current based on optimal oscillator selection.

Fig.4 Typical operating supply current (I_{DD}) as a function of operating supply voltage (V_{DD}).



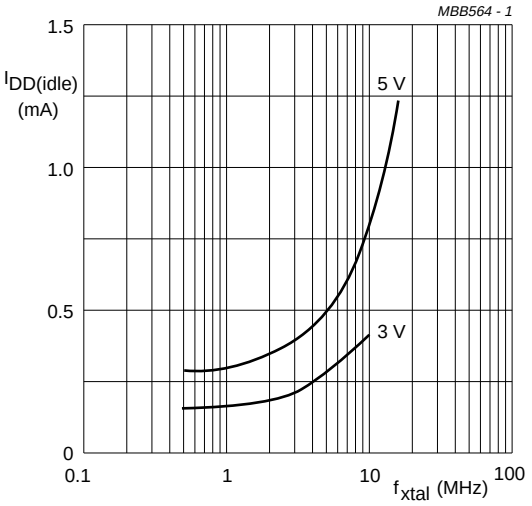
Supply current based on optimal oscillator selection.

Fig.5 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



Supply current based on optimal oscillator selection.

Fig.6 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of operating supply voltage (V_{DD}).



Supply current based on optimal oscillator selection.

Fig.7 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of clock frequency (f_{xtal}).

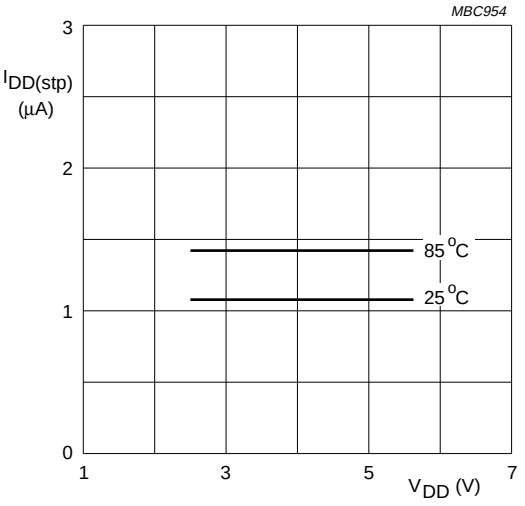
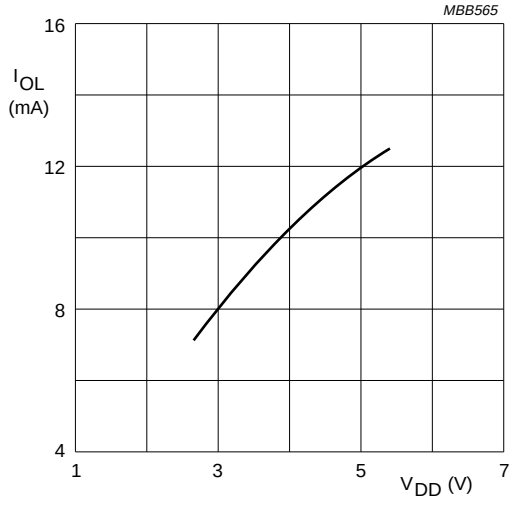
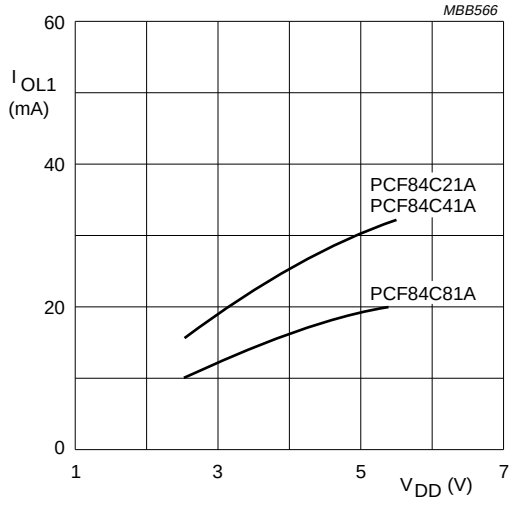


Fig.8 Typical supply current in Stop mode ($I_{DD(stp)}$) as a function of operating supply voltage (V_{DD}).



V_O = 0.4 V.

Fig.9 Typical LOW level output sink current (I_{OL}) as a function of operating supply voltage (V_{DD}).



V_O = 1.2 V.

Fig.10 Typical LOW level output sink current for Port 1 (I_{OL1}) as a function of operating supply voltage (V_{DD}).

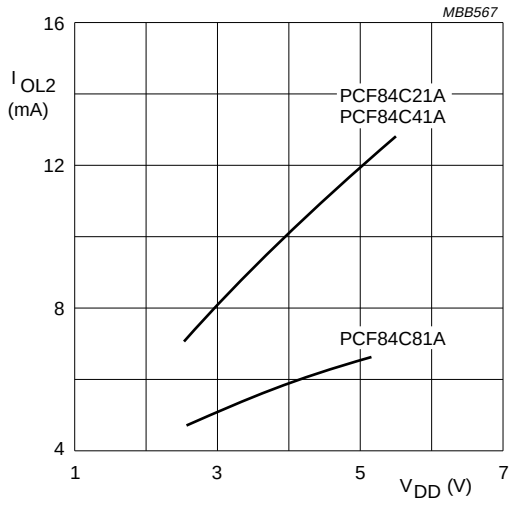


Fig.11 Typical LOW level output sink current for SDA/P2.3 or SCLK (I_{OL2}) as a function of operating supply voltage (V_{DD}).

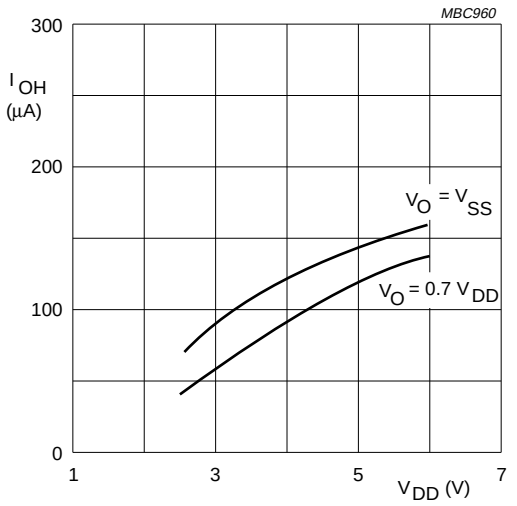
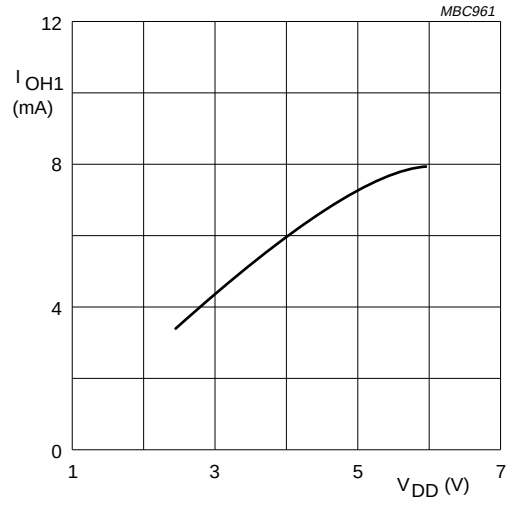


Fig.12 Typical HIGH level pull-up output source current (I_{OH}) as a function of operating supply voltage (V_{DD}).



$V_{OL} = V_{DD} - 0.4$ V.

Fig.13 Typical HIGH level push-pull output source current (I_{OH1}) as a function of operating supply voltage (V_{DD}).

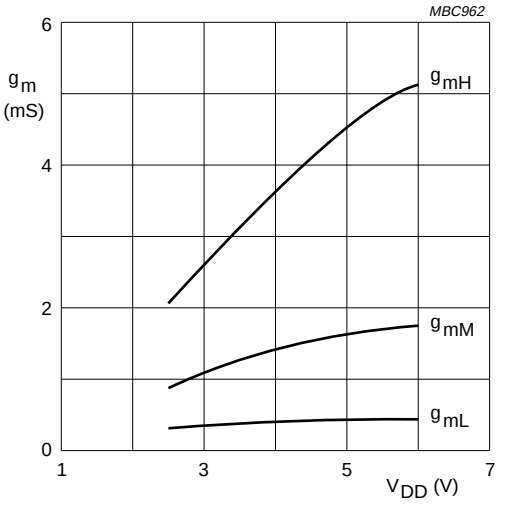


Fig.14 Typical transconductance values (g_m) as a function of operating supply voltage (V_{DD}) for the options g_{mL}, g_{mM} and g_{mH}.

12 AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
f_{xtal}	clock frequency	see Fig.3	1	–	16	MHz

Table 2 I^2C-bus timing (see Figs 15 and 16)

SYMBOL	PARAMETER	INPUT (see Fig.14)	OUTPUT (see Fig.15; note 1)
SCLK			
$t_{HD;STA}$	START condition hold time	$\geq \frac{14}{f_{xtal}}$	$\frac{DF + 9}{2 \times f_{xtal}}$
t_{LOW}	SCLK LOW time	$\geq \frac{17}{f_{xtal}}$	$\frac{DF - 3}{2 \times f_{xtal}}$; note 2
t_{HIGH}	SCLK HIGH time	$\geq \frac{17}{f_{xtal}}$	$\frac{DF + 3}{2 \times f_{xtal}}$; note 2
t_{RC}	SCLK rise time	≤1 µs	≤1 µs; note 3
t_{FC}	SCLK fall time	≤0.3 µs	≤0.1 µs; note 4
SDA			
t_{BUF}	bus free time	$\geq \frac{14}{f_{xtal}}$	≥ 4.7 µs; note 5
$t_{SU;DAT}$	data set-up time	≥ 250 ns	$\geq \frac{15}{f_{xtal}}$; note 6
$t_{HD;DAT}$	data hold time	≥ 0	$\geq \frac{9}{f_{xtal}}$
t_{RD}	SDA/P2.3 rise time	≤1 µs	≤1 µs; note 3
t_{FD}	SDA/P2.3 fall time	≤0.3 µs	≤0.1 µs; note 4
$t_{SU;STO}$	STOP condition set-up time	$\geq \frac{14}{f_{xtal}}$	$\frac{DF - 3}{2 \times f_{xtal}}$

Notes

1. DF stands for Division Factor: the divisor of f_{xtal} (see the *"PCF84CxxxA family"* data sheet).
2. Values given for ASC = 0; for ASC = 1: $t_{HIGH} = \frac{3\,(DF + 1)}{4 \times f_{xtal}}$; $t_{LOW} = \frac{DF - 3}{4 \times f_{xtal}}$
3. Determined by I^2C-bus capacitance (C_b) and external pull-up resistor.
4. At maximum allowed I^2C-bus capacitance C_b = 400 pF.
5. Determined by program.
6. If $t_{LOW} < \frac{24}{f_{xtal}}$, $t_{SU:DAT} \geq \frac{t_{LOW} - 9}{f_{xtal}}$, independent of ASC.

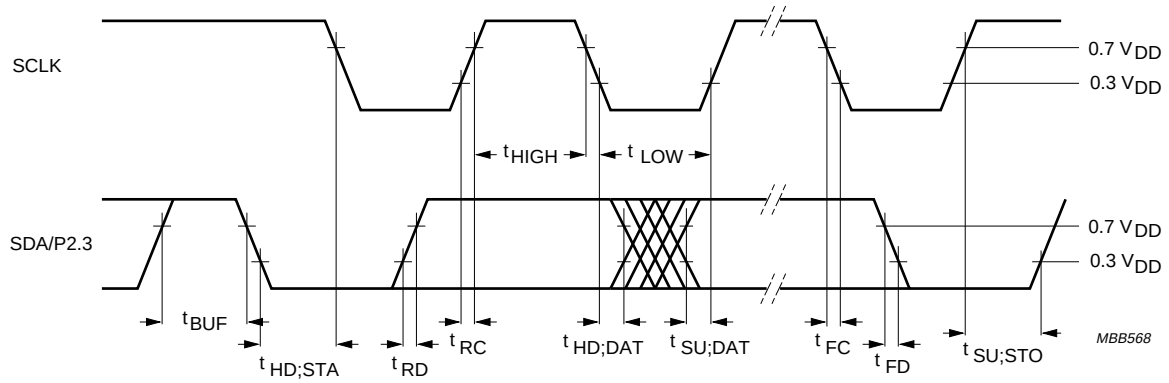


Fig.15 Slave SCLK receiver SDA/P2.3 timing (SCLK and SDA/P2.3 are inputs).

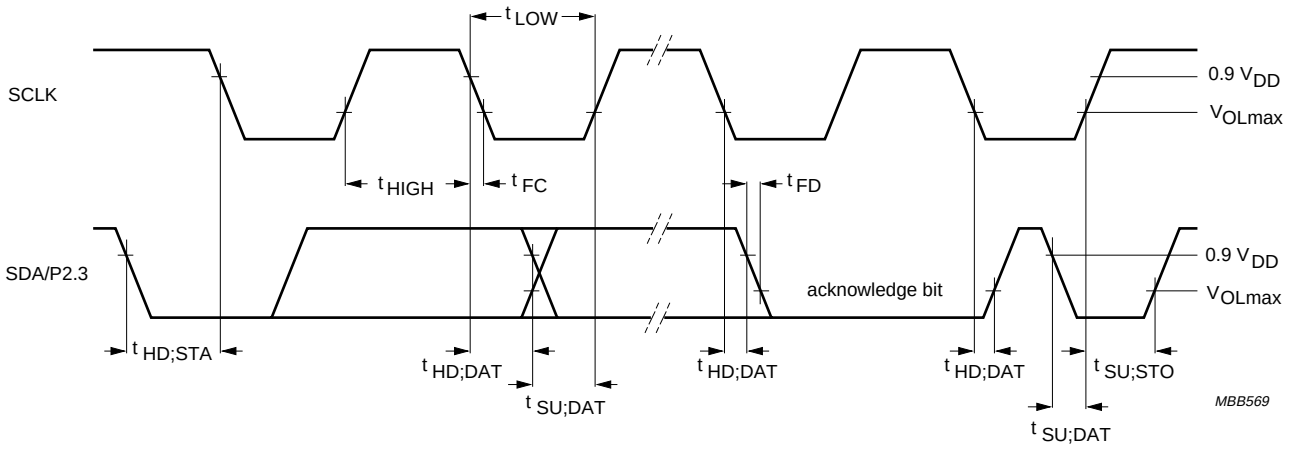
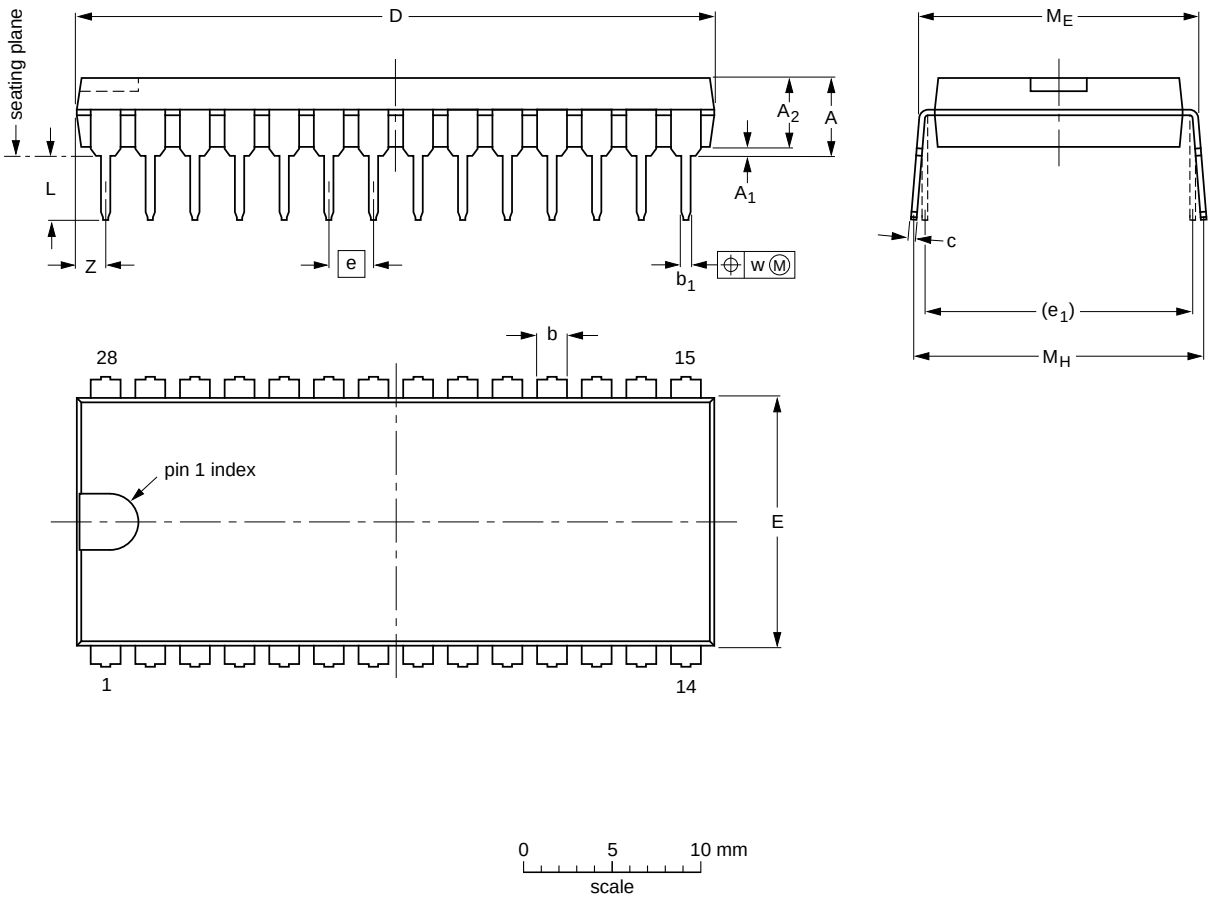


Fig.16 Master SCLK and transmitter SDA/P2,3 timing (SCLK and SDA/P2.3 are outputs).

13 PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

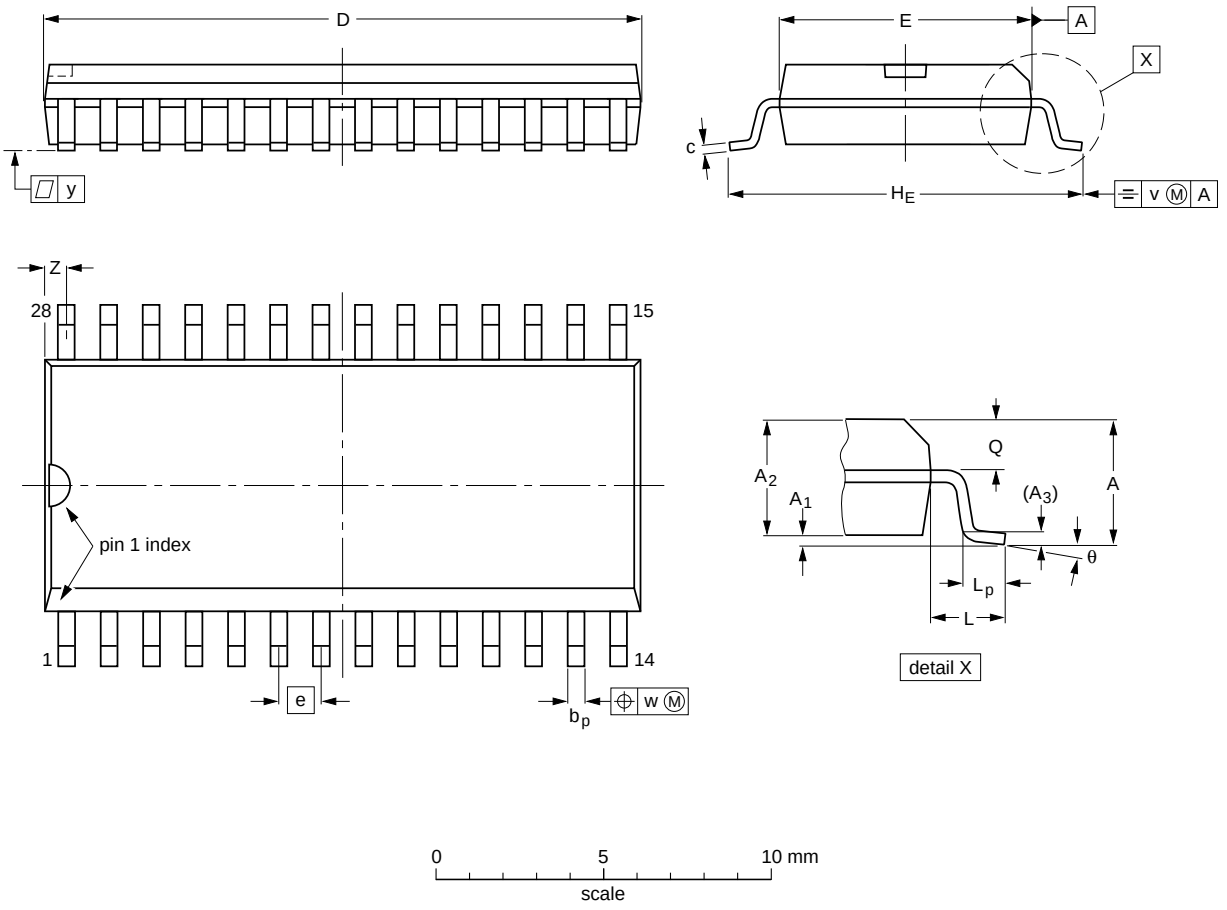
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

14 SOLDERING

14.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

14.2 DIP

14.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

14.3 SO

14.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

14.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

17 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.