PA41DIE

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous	60mA
INPUT VOLTAGE, differential	±16V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, junction	150°C

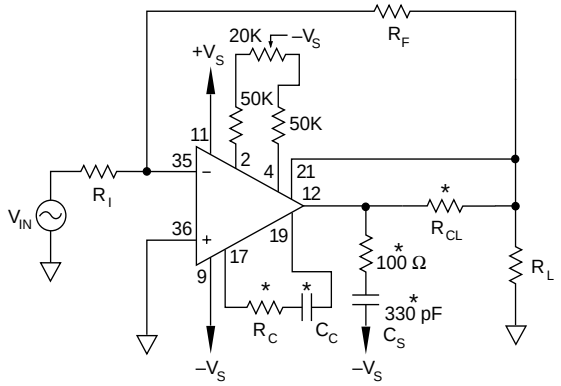
NOTE: Refer to parent product data sheet PA41 for typical AC electrical characteristics, precautions, applications and other test parameters.

DC WAFER PROBED SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE, initial			15	30	mV
OFFSET VOLTAGE, vs. supply	V_S = ±50 V to ±175 V		20	32	µV/V
OFFSET VOLTAGE, vs. temperature[2]	T_A = 25-85°C		50	130	µV/°C
BIAS CURRENT, initial			10	50	pA
COMMON MODE REJECTION	V_{CM} = ±90 V DC	84	94		dB
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–9		V
SUPPLY CURRENT, quiescent		.9	1.4	2.0	mA

NOTES: 1. Unless otherwise stated V_S = ±150 V, T_A = 25°C, DC input specification ± value given.
2. Sample tested by wafer to 95%.

TYPICAL EXTERNAL CONNECTIONS

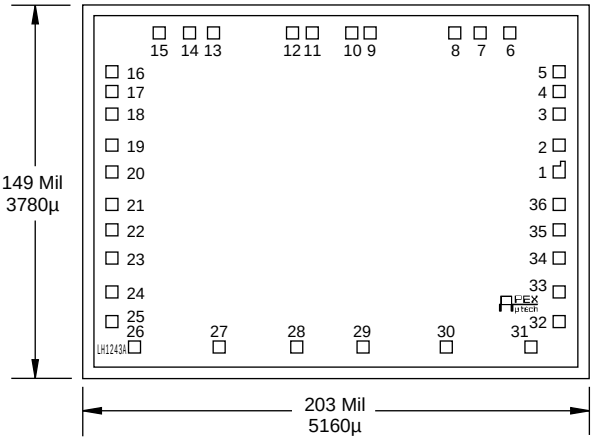


* Required component and value if given.
Optional balance components are recommended values.
C_S, C_C are NPO, rated for full supply voltage $-V_S$ to $+V_S$.

NOTE: Diagram for connection illustration only.
All op amp configurations are possible.

Pad	Function	Pad	Function
2	Balance	17	Compensation
4	Balance	19	Compensation
9	– Supply	21	Current Limit
11	+ Supply	35	– Input
12	Output	36	+ Input

DIE LAYOUT



Thickness: 20 Mil (508µ)
Backside: Ti (500Å) Au (3000Å)
Bond pad: 4.9 Mil sq (125µ) Al
Bond pads 17 and 10 are connected
Make no connection to bond pads not listed by function

NOTE: Backside at $-V_S$ potential.
Make no connection.

CAUTION PA41DIE is a MOSFET amplifier. ESD handling procedures must be observed.

