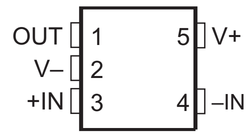
1.8-V MICROPOWER CMOS OPERATIONAL AMPLIFIER ZERO-DRIFT SERIES

Check for Samples: OPA333-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Low Offset Voltage: 10 μV (Max)**
- **0.01-Hz to 10-Hz Noise: 1.1 μV_{PP}**
- **Quiescent Current: 17 μA**
- **Single-Supply Operation**
- **Supply Voltage: 1.8 V to 5.5 V**
- **Rail-to-Rail Input/Output**
- **MicroSize SOT23 (DBV) Package**

DBV PACKAGE
(TOP VIEW)

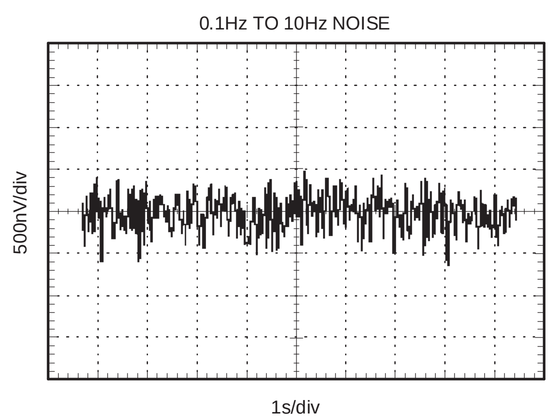


DESCRIPTION/ORDERING INFORMATION

The OPA333 series of CMOS operational amplifiers uses a proprietary auto-calibration technique to simultaneously provide very low offset voltage (10 μV max) and near-zero drift over time and temperature. These miniature, high-precision, low-quiescent-current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 50 mV of the rails. Single or dual supplies as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V) may be used. They are optimized for low-voltage single-supply operation.

The OPA333 family offers excellent common-mode rejection ratio (CMRR) without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

The OPA333 (single version) is available in the SOT23-5 package.



ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOT23 – DBV	Reel of 2500	OPA333QDBVRQ1	QCNQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage		7	V
Signal input terminals, voltage(2)	–0.3	(V+) + 0.3	V
Output short circuit(3)		Continuous	
Operating temperature range	–40	125	°C
Storage temperature range	–65	150(4)	°C
Junction temperature		150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short circuit to ground, one amplifier per package
(4) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

ELECTRICAL CHARACTERISTICS: V_S = 1.8 V to 5.5 V

Boldface limits apply over the specified temperature range, **T_A = –40°C to 125°C**.
At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}	V_S = 5 V		2	10	µV
vs temperature	**dV_{OS}/d_T**	**V_S = 5 V**		**0.5**		**µV/°C**
vs power supply	**PSRR**	**V_S = 1.8 V to 5.5 V**		**1**	**6**	**µV/V**
Long-term stability(1)				(1)		
Channel separation, dc				0.1		µV/V
INPUT BIAS CURRENT						
Input bias current	I_B			±70	±200	pA
over Temperature				**±200**		**pA**
Input offset current	I_{OS}			±140	±400	pA
NOISE						
Input voltage noise, f = 0.01 Hz to 1 Hz				0.3		$µV_{PP}$
Input voltage noise, f = 0.1 Hz to 10 Hz				1.1		$µV_{PP}$
Input current noise, f = 10 Hz	i_n			100		fA/√Hz
INPUT VOLTAGE RANGE						
Common mode voltage range	V_{CM}		(V–) – 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	**(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V**	**106**	**130**		**dB**
INPUT CAPACITANCE						
Differential				2		pF
Common mode				4		pF
OPEN-LOOP GAIN						
Open-loop voltage gain	**A_{OL}**	**(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ**	**106**	**130**		**dB**
FREQUENCY RESPONSE						
Gain-bandwidth product	GBW	C_L = 100 pF		350		kHz
Slew rate	SR	G = 1		0.16		V/µs
OUTPUT						
Voltage output swing from rail		R_L = 10 kΩ		30	50	mV
over temperature		**R_L = 10 kΩ**			**85**	**mV**
Short-circuit current	ISC			±5		mA
Capacitive load drive	CL					
(2)Open-loop output impedance		f = 350 kHz, I_O = 0		2		kΩ
POWER SUPPLY						
Specified voltage range	V_S		1.8		5.5	V
Quiescent current per amplifier	I_Q	I_O = 0		17	25	µA
over temperature					**30**	**µA**
Turn-on time		V_S = 5 V		100		µs

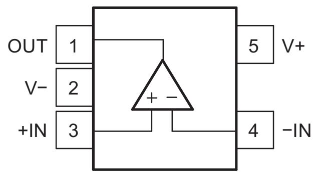
(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.
(2) See Typical Characteristics

ELECTRICAL CHARACTERISTICS: V_S = 1.8 V to 5.5 V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to 125°C**.
At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE						
Specified range			–40		125	°C
Operating range			–40		125	°C
Storage range			–65		150	°C
Thermal resistance	θ_{JA}					
SOT23-5				200		°C/W

PIN CONFIGURATION

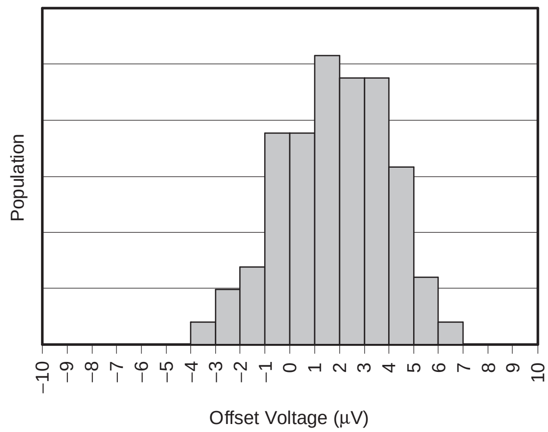


SOT23-5

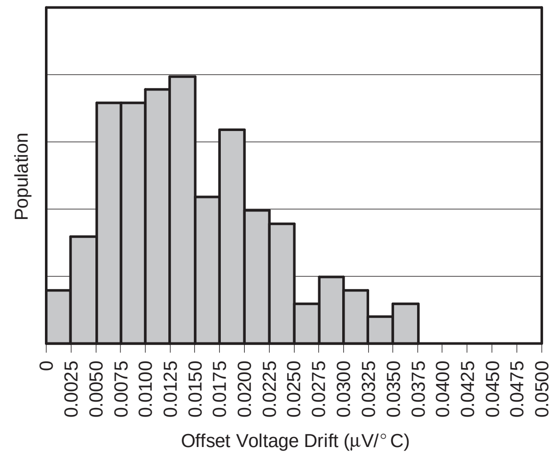
TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted)

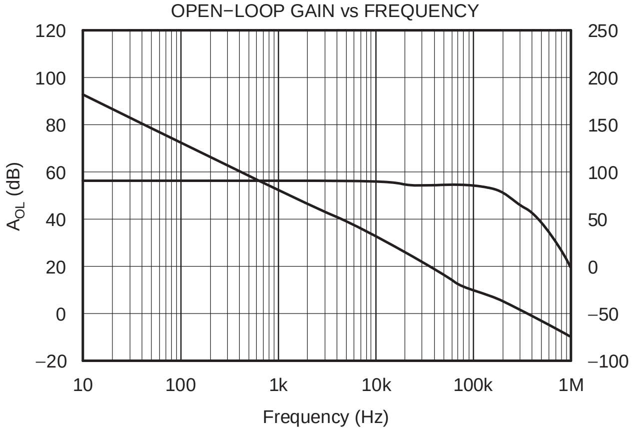
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



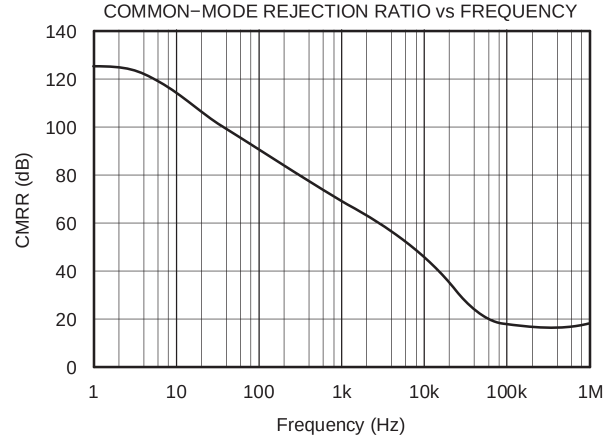
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



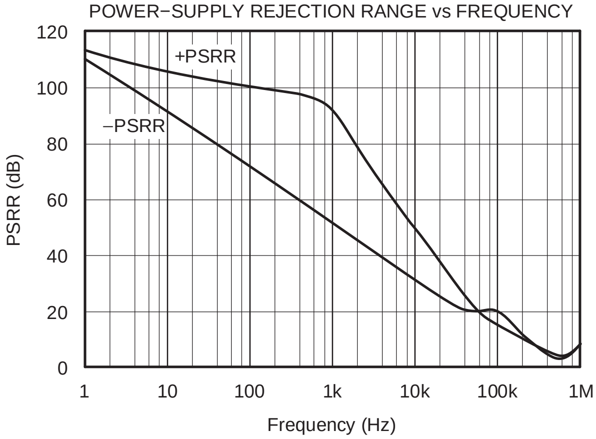
OPEN−LOOP GAIN vs FREQUENCY



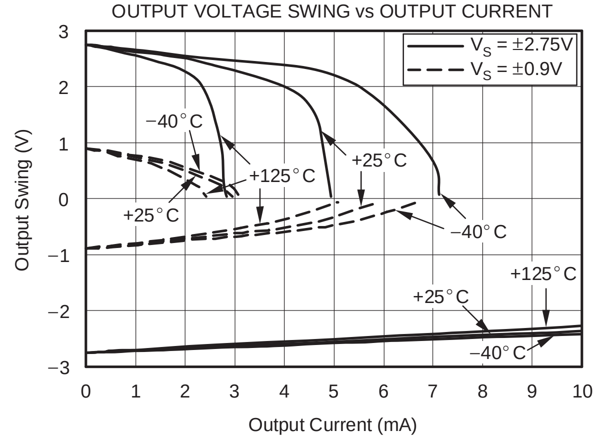
COMMON−MODE REJECTION RATIO vs FREQUENCY



POWER−SUPPLY REJECTION RANGE vs FREQUENCY

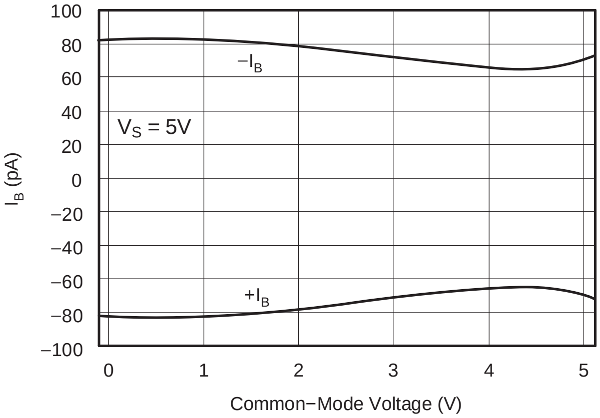


OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

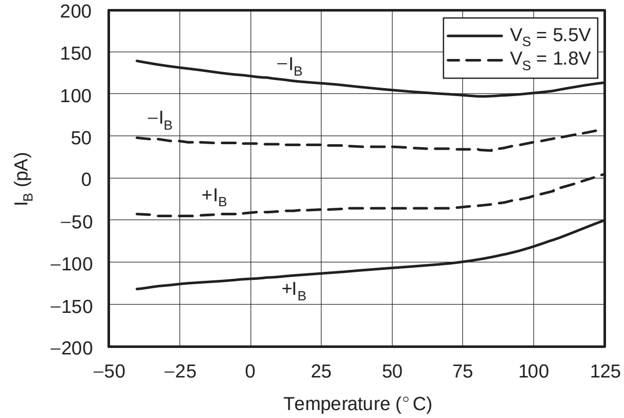


TYPICAL CHARACTERISTICS (continued)

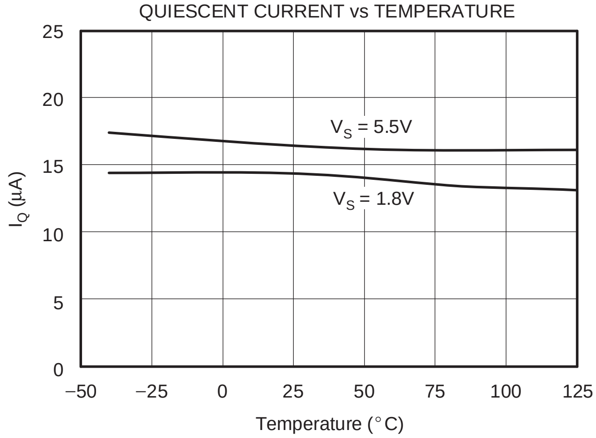
INPUT BIAS CURRENT vs COMMON−MODE VOLTAGE



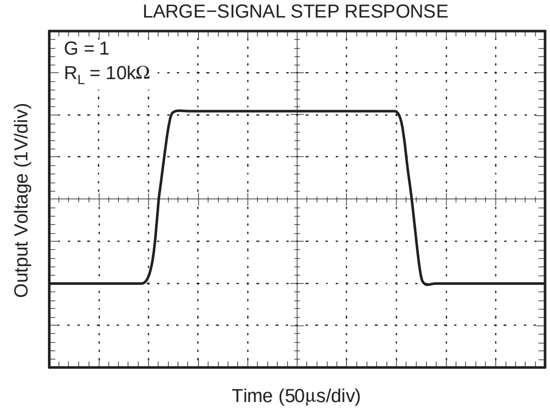
INPUT BIAS CURRENT vs TEMPERATURE



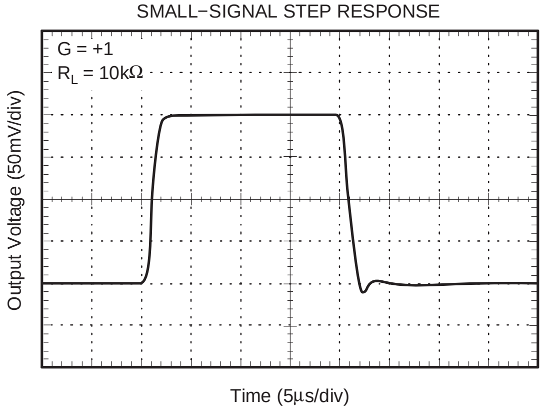
QUIESCENT CURRENT vs TEMPERATURE



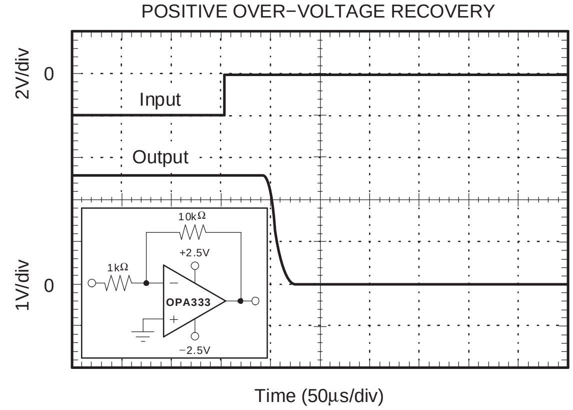
LARGE−SIGNAL STEP RESPONSE



SMALL−SIGNAL STEP RESPONSE

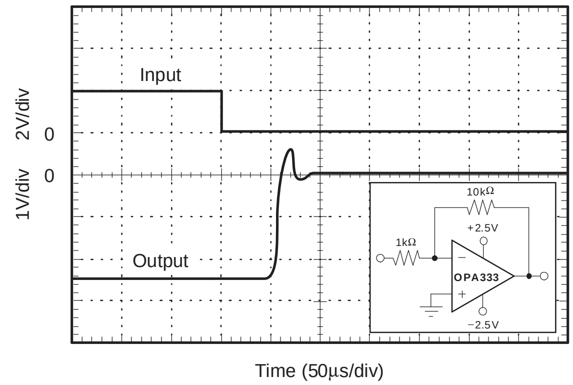


POSITIVE OVER−VOLTAGE RECOVERY

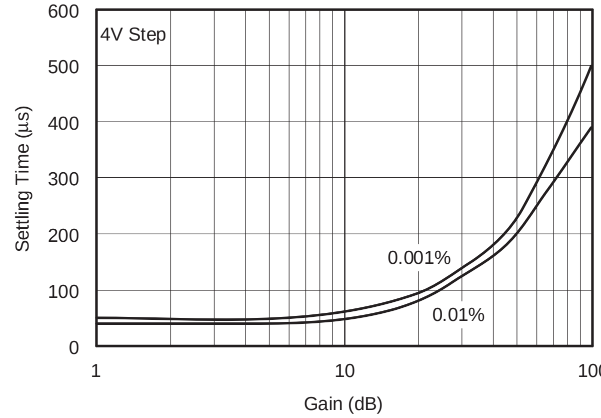


TYPICAL CHARACTERISTICS (continued)

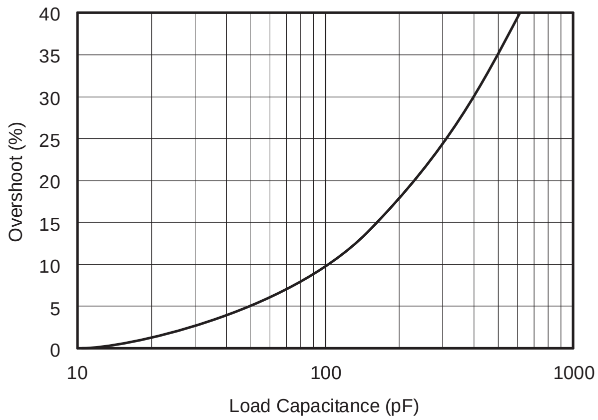
NEGATIVE OVER−VOLTAGE RECOVERY



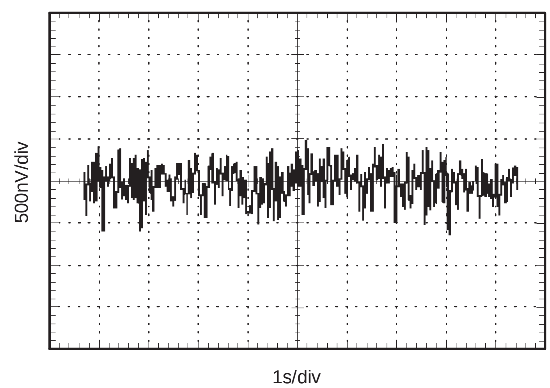
SETTLING TIME vs CLOSED−LOOP GAIN



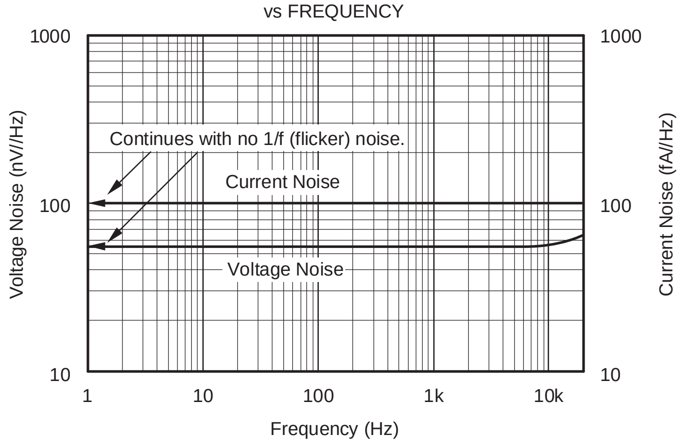
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



0.1Hz TO 10Hz NOISE



CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY



APPLICATION INFORMATION

The OPA333 is unity-gain stable and free from unexpected output phase reversal. They use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by ensuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals)
- Thermally isolate components from power supplies or other heat sources
- Shield op amp and input circuitry from air currents, such as cooling fans

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

Operating Voltage

The OPA333 op amp operates over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

Input Voltage

The OPA333 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Normally, input bias current is about 70 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor(see Figure 1).

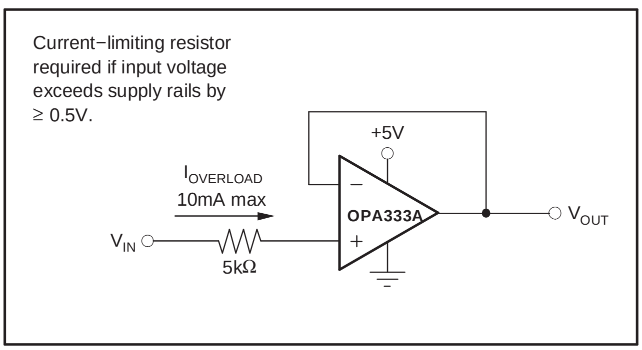


Figure 1. Input Current Protection

Internal Offset Correction

The OPA333 op amp uses an auto-calibration technique with a time-continuous 350-kHz op amp in the signal path. This amplifier is zero corrected every 8 μs using a proprietary technique. Upon power up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA333 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve (see Figure 2).

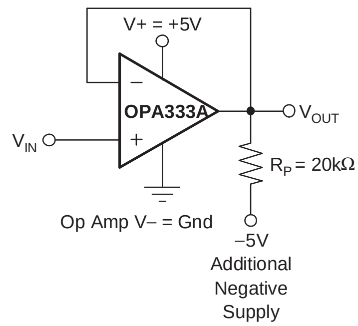


Figure 2. V_{OUT} Range to Ground

The OPA333 has an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA333 has been characterized to perform with this technique; however, the recommended resistor value is approximately 20 kΩ. Note that this configuration will increase the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occurs below –2 mV, but excellent accuracy returns as the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the op amp to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

General Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in their susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The OPA333 has been specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous-generation devices. Strong RF fields may still cause varying offset levels.

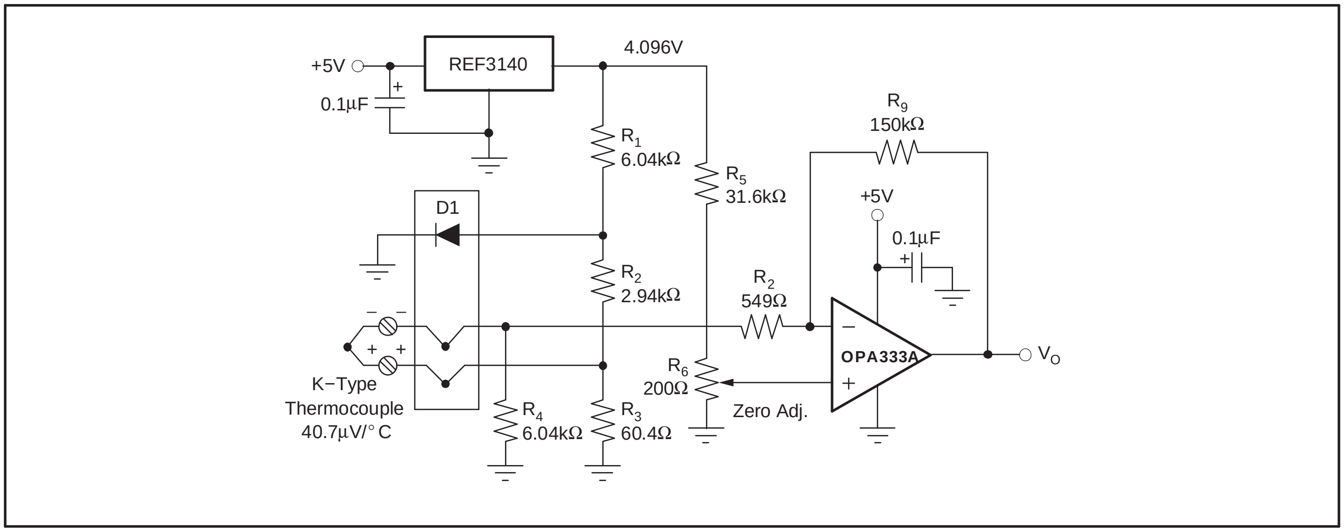


Figure 3. Temperature Measurement

Figure 4 shows the basic configuration for a bridge amplifier.

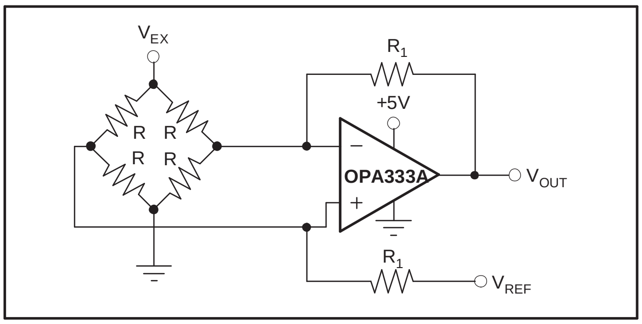


Figure 4. Single Op-Amp Bridge Amplifier

A low-side current shunt monitor is shown in Figure 5. R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. Since the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5-V power supply is sufficiently stable, the REF3130 may be omitted.

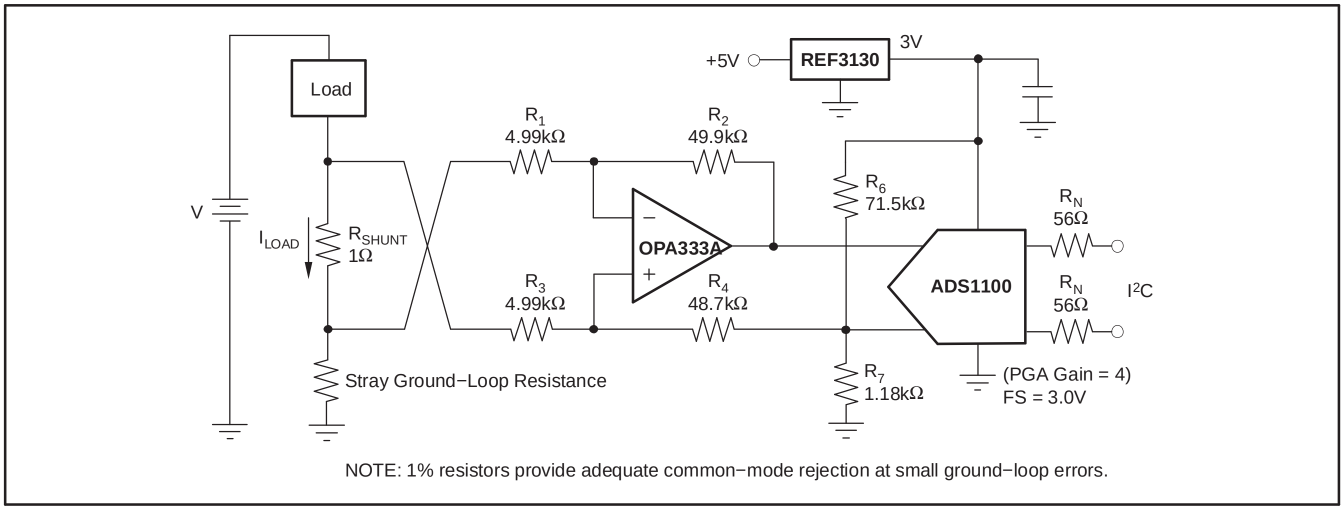


Figure 5. Low-Side Current Monitor

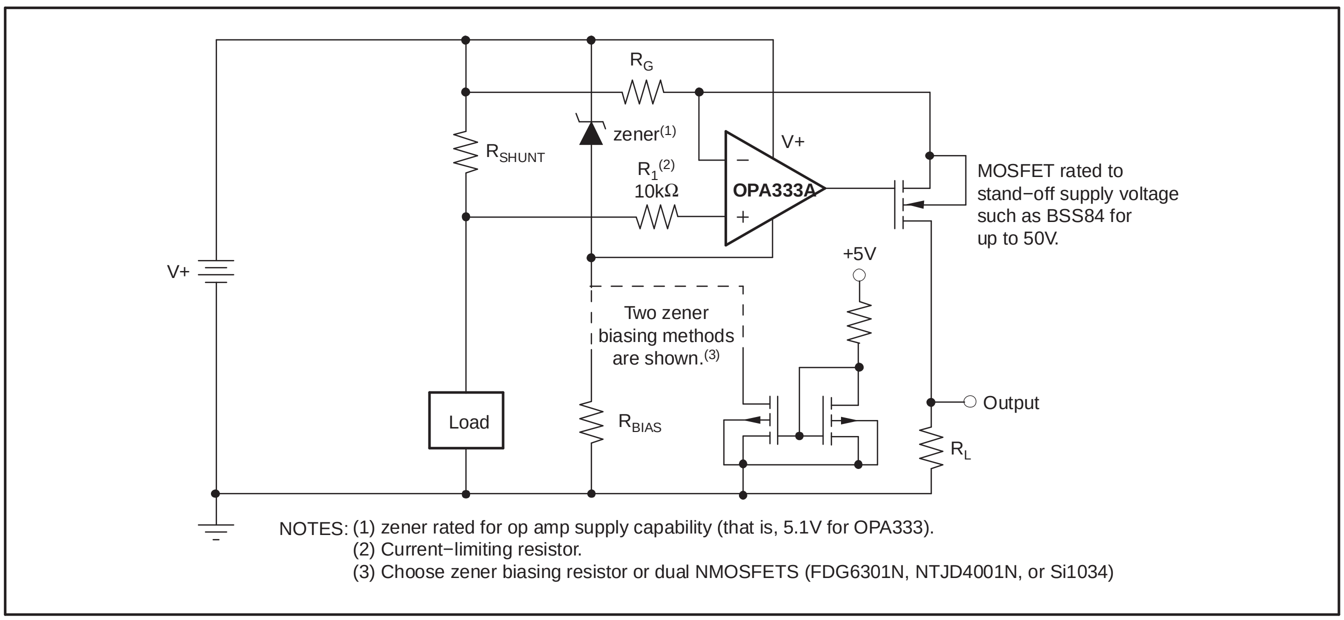


Figure 6. High-Side Current Monitor

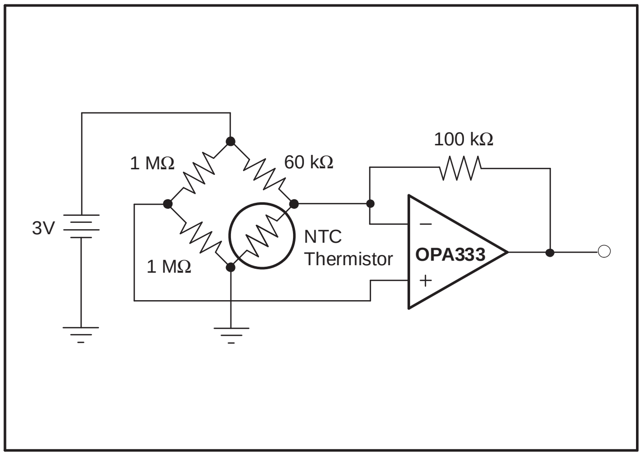


Figure 7. Thermistor Measurement

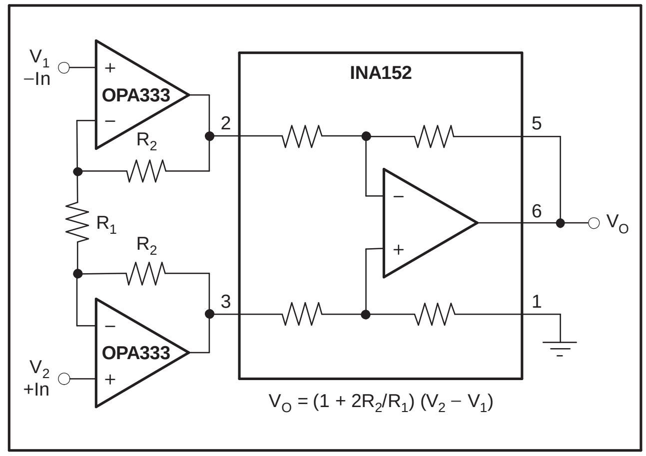


Figure 8. Precision Instrumentation Amplifier

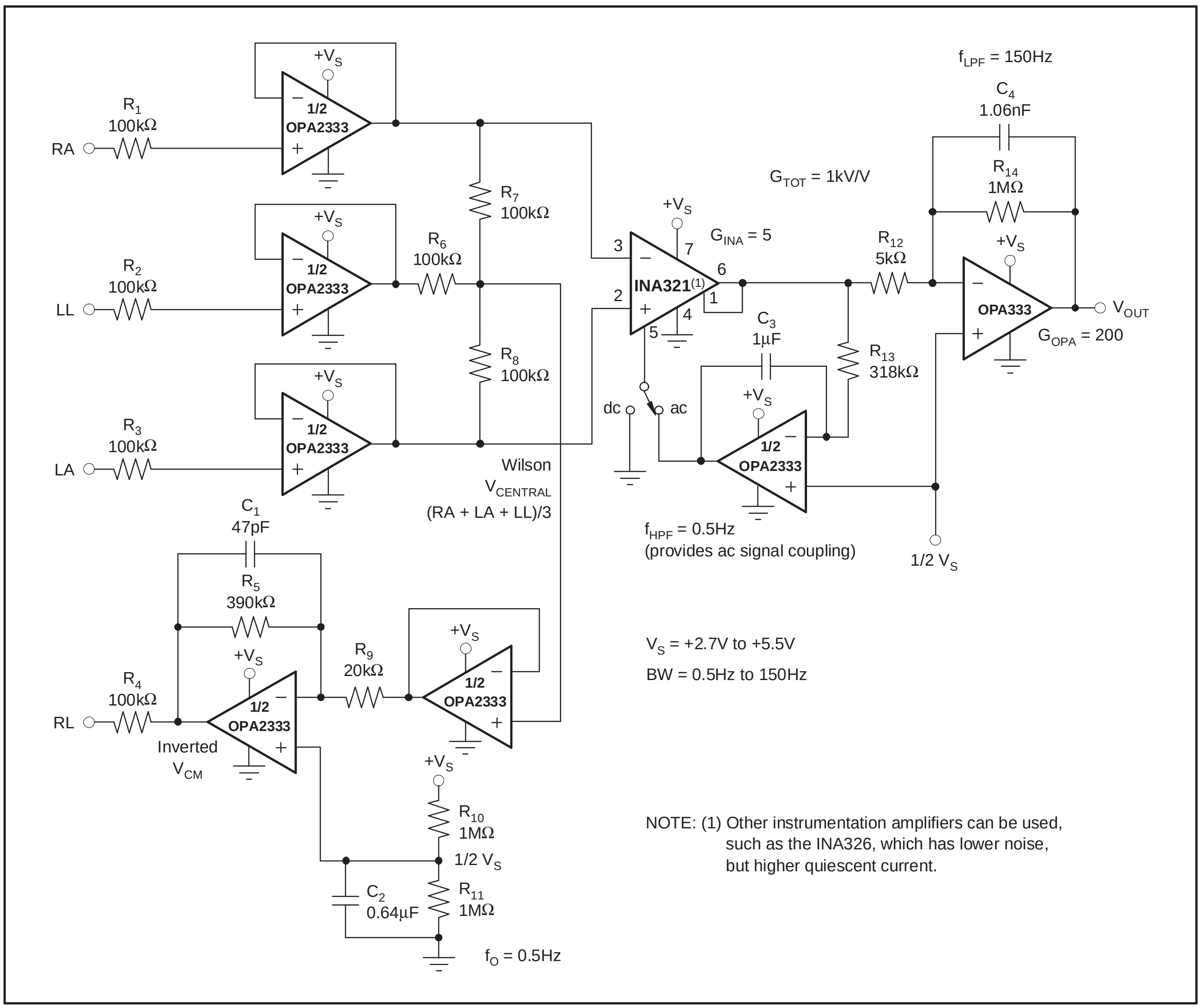


Figure 9. Single-Supply, Very-Low-Power ECG Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA333AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA333-Q1 :

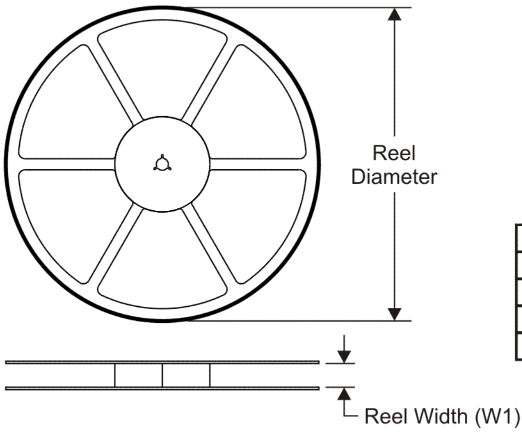
- Catalog: OPA333

NOTE: Qualified Version Definitions:

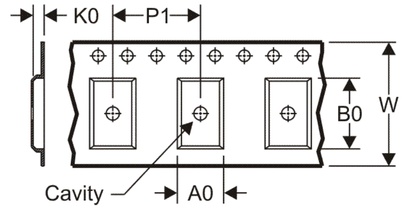
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

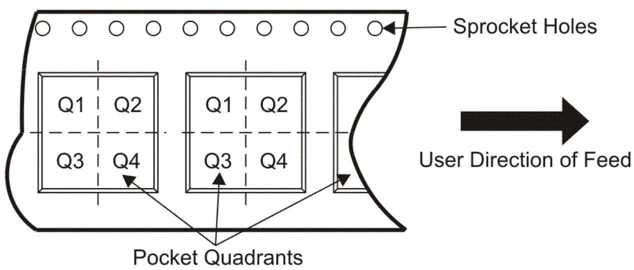


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

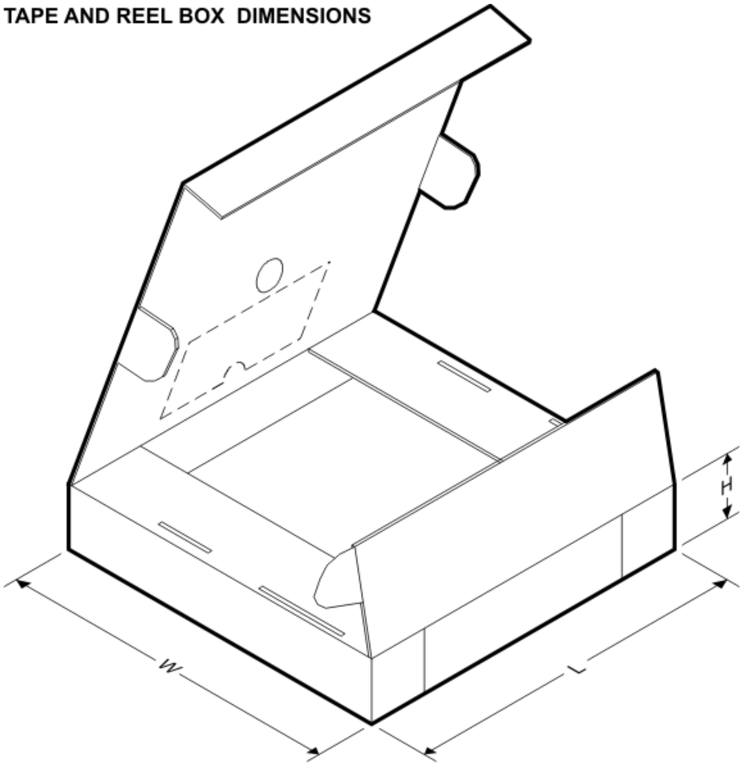
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA333AQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

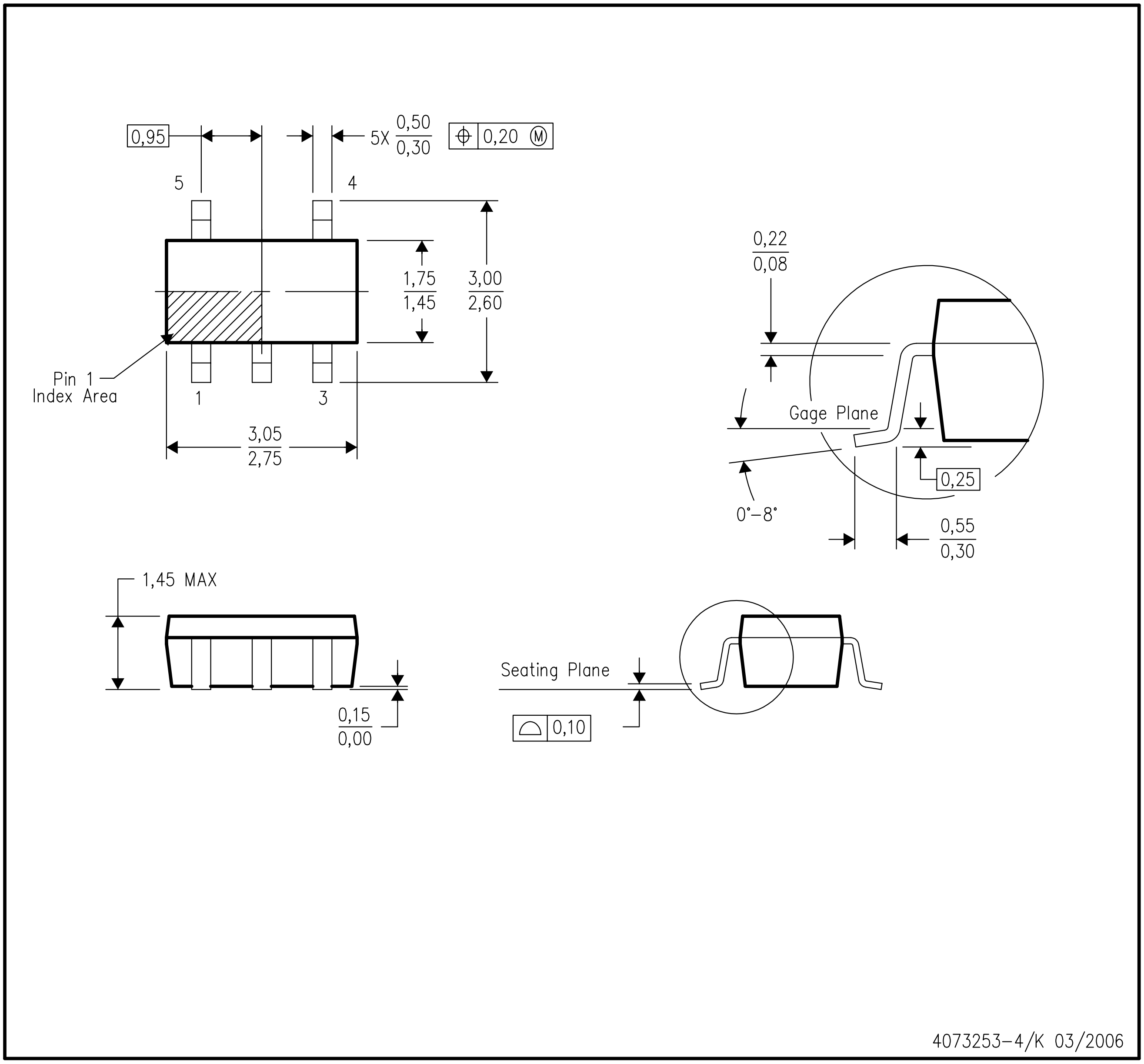
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

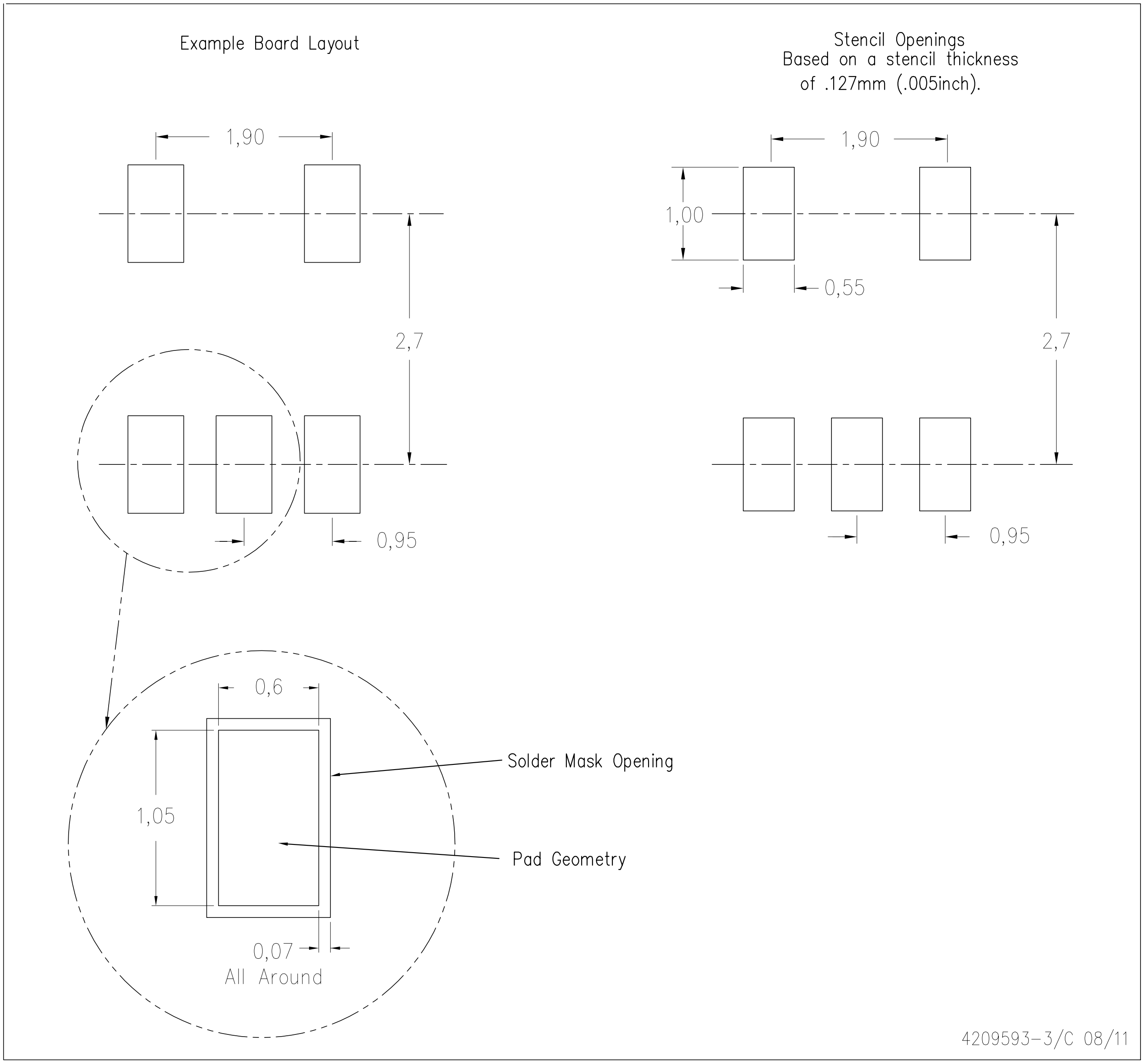
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA333AQDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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